EEC 118 Spring 2011 Lab #4 Part 1: Simulating D Flip-Flops

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Reading: Rabaey 7.1-7.3 [1].
Reference: Kang and Leblebici Chapters 4, 5, and 8 [2].

I OBJECTIVE

The objective of this lab is to use Cadence and your design library (inverters, logic gates, etc. from Lab 3) to build and simulate CMOS circuits for sequential elements.

II PRELAB

There is no prelab for this lab (basically, Lab 3 was the prelab).

III MODIFIED VTC

Part 1 (20 points) Simulate the Voltage Transfer Characteristic for modified inverters you design based on the previous lab, using a DC (slow) sweep analysis for v_{in}, the inverter input voltage. Resize the transistors in the inverter you designed in Lab 3 Part 1 to achieve $V_M = 0.4V_{DD}$ and $V_M = 0.6V_{DD}$. Record the device W/L ratios for your lab report. Turn in a plot of the two additional VTCs from your simulation, with V_M labeled.

IV DYNAMIC MOS FLIP-FLOP

Part 2 (10 points) The dynamic D Flip-Flop configuration shown in Figure 1 is often used in high speed digital circuits to store data. Implement the circuit in Cadence using the inverter with $V_M = V_{DD}/2$ designed previously in Lab 3. Create a cell called `pDFF_dyn` with a schematic view and a symbol view. Use the 180nm transistors from Lab 3, $V_{DD} = 1.8$V, and $C_0 = C_1 = 1.5$ fF for the capacitors. Try to minimize the total area of the transmission gate transistors in your implementation.

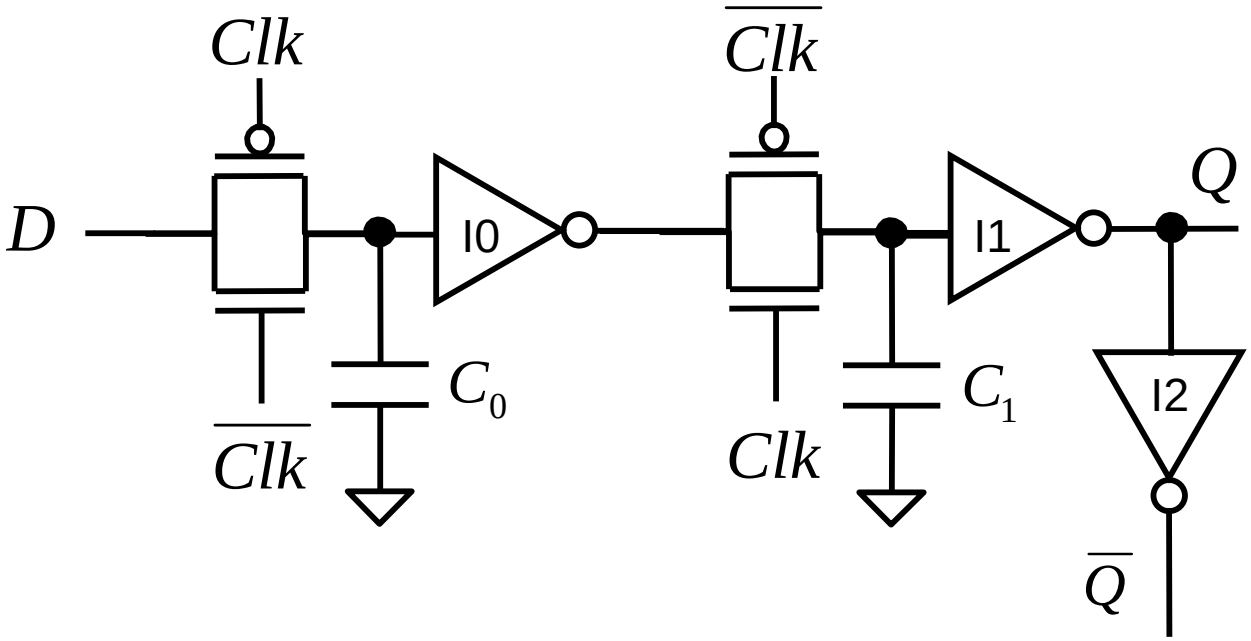

Figure 1: Dynamic D Flip-Flop with Complementary Outputs.

Part 3 (20 points) Create a testbench schematic `pDFF_dyn_tb` and instantiate one of your `pDFF_dyn` cells. Verify the operation of the flip-flop by wiring the $\overline{Q}$ output to the input D. In this configuration, the flip-flop acts as a T flip-flop, and the output Q will be the clock divided by 2. To accurately simulate the flip-flop under realistic loading conditions, connect the inputs of 4 inverters to each of the Q and $\overline{Q}$ flip-flop outputs. This loading condition is called a **fanout** of four (**FO4**) and is often used as a standard load to measure transient parameters such as rise and fall times. Also, make sure that both the Clk and $\overline{Clk}$ inputs are driven by inverters instead of voltage sources (you can use the `vpulse` source to create a periodic square wave for the clock), to accurately reflect the output impedance of a realistic clock buffer. Simulate the flip-flop with a clock frequency of 500 MHz. Turn in a plot of 10 clock cycles showing your flip-flop operating correctly. along with your flip-flop and testbench schematics.

Part 4 (20 points) Increase the size of the internal load capacitances from 1 fF to 10 fF and 25 fF. How does increasing the capacitances affect the output voltage levels and timing? What are the advantages and disadvantages of increasing the capacitance? Turn in a plot of 10 clock cycles showing the flip-flop operation for these two values of capacitance.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.