EEC 118 Spring 2011 Lab #3 Part 1: Schematic Capture Tutorial

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Reading: Rabaey Chapters 1, 5, Section 6.2 [1].
Reference: Kang and Leblebici Chapters 1, 6, 7.3-4 [2], Brunvand Chapters 1-3 [3].

1 OBJECTIVE

The objective of this lab is to set up Cadence, your design library, and start to familiarize yourself with a full custom IC design flow.

2 TOOL SETUP

To get started, you first need to set up the Cadence tools. Cadence creates a bunch of random text files which set all kinds of configuration information. It is best to keep these in a single directory for the purposes of the labs. Log in to one of the lab workstations and at the prompt type:

```
eec118-setup
```

This should create a directory which you should `cd` to before starting up Cadence:

```
cd ~/eec118
```

Type `ls -a` and take a look at some of the configuration files, just to familiarize yourself with their contents. Now you are ready to start Cadence. Type

```
virtuoso &
```

at the prompt, and you should see a window labeled "Virtuoso 6.1.4" open up. This window is part of Cadence's Design Framework interface (GUI). A "What's New" window and the **Library Manager** window should open up, too. The first window is the **Command Interpreter Window** or **CIW**. Scroll through it to look at the messages displayed as the tool loads. Ignore any warnings for now. Get in the habit of scanning these messages whenever you launch the tool, keeping an eye out for any that are out of the ordinary. This will be very helpful if you encounter any tool-related problems.

You will store your design information in a *library*. The Library Manager is the interface which allows you to manipulate your design information as well as other components from other libraries, which may be shared with other users. Although the library information is

stored as Unix files, don't try to move or rename them using shell commands. This can lead to inconsistent behavior and will likely break your libraries.

Familiarize yourself with the Library Manager and the corresponding `cds.lib` file in your `eec118` directory. You should be able to see some basic utility libraries, two libraries specific to UC Davis (`UCD_Analog_Parts` and `UCD_Digital_Parts`) and a technology library from the NCSU Cadence Design Kit (CDK) called `NCSU_TechLib_tsmc02d`. This technology library provides the physical design data and verification rules for the MOSIS Scalable CMOS 0.18μm process using DEEP design rules. This will be the example process we use in EEC 118 and EEC 119AB. The File menu allows you to create new libraries and cells within a library, while the Edit menu lets you copy, rename, delete, and update the access permissions.

Create a new library by invoking File→New→Library... in the Library Manager. Name the library `EEC118_<xx>` where `<xx>` is your username. Leave the path alone and the new library will be created in your current working directory (∼`/eec118`). Hit OK and a new window called "Technology File for New Library" should appear. Choose "Attach to an existing technology library" and accept the default, `NCSU_TechLib_tsmc02d`.

2.1 Project Directory

Although it won't be used for this lab, you should have a directory with a greatly expanded capacity for storing design information, simulation results, etc. `cd` to `/project/<username>` and make sure you can create, edit, and save files to that directory using `cat` or a text editor.

2.2 Remote Access

You should be able to access Cadence tools and the `/project` directory tree by using `ssh` to log in to `snake.ece.ucdavis.edu`. You are free to work on any aspects of labs or projects remotely, but if you need questions answered in real-time then you should attend the lab sections or the instructor or TA office hours.

3 SCHEMATIC CAPTURE

Part 1 Inverter Schematic First, we will create a new *cell* which represents a CMOS inverter. Cells have multiple views, including schematic, symbol, layout, etc. The circuit schematic view for a cell will be called `schematic`. In the second part of the lab, you will create a physical design (or layout) view of the cell called `layout`.

In the Library Manager, choose File→New→Cell View... In your `EEC118_<xx>`, enter a cell name of `inv_1x` and a view name of `schematic`. The Type field should also say schematic. The `_1x` designation indicates that this is a minimum size inverter (i.e., the PMOS and NMOS transistors are as small as we are allowing in our design). There are times when you will want bigger inverters, for example, to drive long wires or other large capacitive loads.

Click OK. You may get a window asking you to confirm the association of the schematic view with a particular tool. An empty schematic window should open. Our goal is to create an inverter schematic identical to the one shown in Figure 1. We are working in a 0.18μm

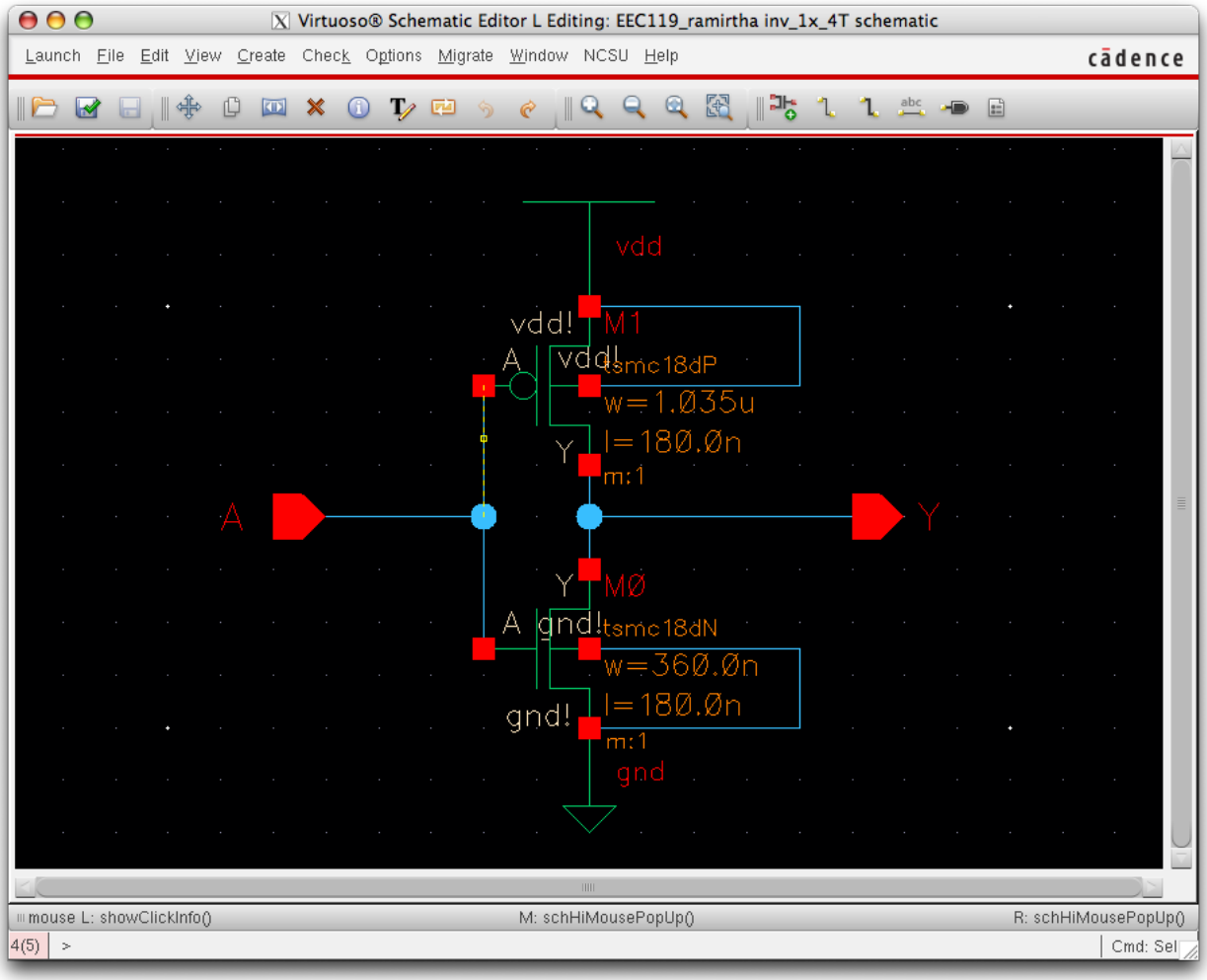

Figure 1: CMOS 1X inverter schematic.

minimum feature size technology, meaning the smallest transistor gate length is 0.18μm. Scalable CMOS design rules require that all dimensions (for transistors, wires, resistors, capacitors, etc.) must be integer multiples of a fundamental unit called λ, typically equal to half the minimum feature size (0.09μm or 90nm in our case). However, the tool uses a grid of $\lambda/2$ (corresponding to 45nm). Take care when you are instantiating devices in a schematic or layout that you set dimensions as integer multiples of the λ unit to save yourself headaches later on.

Choose Create→Instance to open a **Component Browser** window. The menu lists keyboard shortcuts (for example, *i* for Instance) for various commands. You'll want to memorize the shortcuts you use most often. We will use the four terminal devices (`pmos4` and `nmos4`) from the `UCD_Analog_Parts` library. Choose `pmos4`. The Add Instance dialog window will appear. Look over the parameters to become familiar with them, and then set the Width property to 1.035u ("u" corresponds to microns). Click in the schematic window to place the device. Go back to the Component Browser and select and place the NMOS transistor (be sure to set its Width as well, "n" corresponds to nanometers). If you ever need to modify a devices properties, you can invoke the Edit→Properties→Objects... from the menu and then select the component to modify. Many times when you invoke a command from the menu or a hotkey, the command will remain in effect. Hit Esc to get out of that particular command mode. Many other useful commands are under the Edit menu tab (Undo, Redo, Move, Copy, Rotate, Delete). Familiarize yourself with these. Pay some attention to how the transistors are placed - neatness is very important. Move the elements around until it looks nice. You can look at the bottom line of the schematic editor window to keep track of which command mode you're in. I prefer placing series devices in a pullup or pulldown network in a line with a gap of at least one grid unit and two or more grid units between the NMOS and PMOS devices. Place the vdd and gnd (power and ground, respectively) components after the transistors are placed.

Next, choose Create→Pin to bring up the Add Pin dialog. Enter A, make sure the pin direction is set to "input", and place the pin. The tools are case sensitive so make sure the pin name is uppercase. Place an output pin named Y.

Now wire the elements together by invoking Create→Wire (narrow). Click on the various elements and terminals until all the connections are completed as shown in Figure 1.

Choose File→Check and Save to verify and save your schematic. It is a good to do this frequently to catch errors early and save your work in case of a crash. If you have any errors or warnings, fix them and run Check and Save again. A common mistake is wires that look like they might touch but don't actually connect. Delete the wire and redraw it.

Part 2 Inverter Symbol The next step is to create a symbol for the inverter. Rather than creating this from scratch, we are going to copy it from another library. Go to the Library Manager window and select the `symbol` view of the `inv` cell from the `UCD_Digital_Parts` library. Right-clicking on the view should bring up a dropdown menu. Select Copy... and fill in the dialog boxes with your library `EEC118_<xx>` in the To Library field and `inv_1x` in the To Cell field. Click OK. If any warnings appear, click OK again to dismiss the warning window. You can also invoke the Copy command by going to Edit→Copy... from the Library Manager menu bar after selecting the view.

Now, you can edit the new `symbol` view for your inverter cell by double-clicking on it in the Library Manager. Modify the symbol by selecting the "inv" label and editing its properties. Change the label to "inv_1x" to match the name of your cell. Then choose File→Check and Save to verify and save your symbol. Fix any warnings or errors and run Check and Save again if necessary.

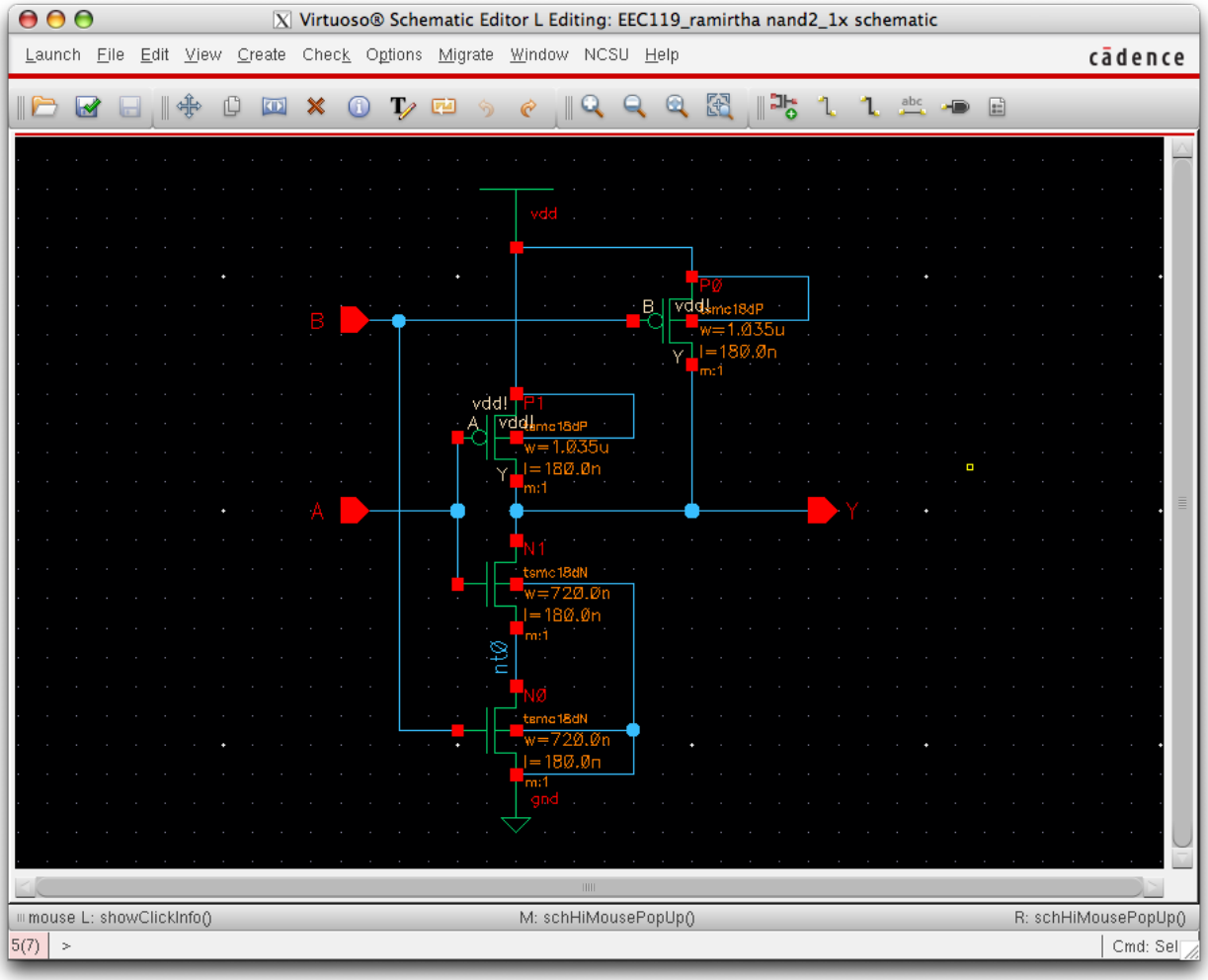

Figure 2: NAND2 gate schematic.

Part 3 NAND Gate Schematic Create a schematic for a two-input nand gate in a cell called `nand2_1x` in your 118 library. The final schematic should look similar to Figure 2. Note that the NMOS transistors have larger device sizes than for the inverter (i.e., the NAND gate is sized for approximately equal rise and fall times). Although pin order doesn't matter logically, it does matter physically and electrically, so you will get errors if you reverse the order. Place the input B pin as shown in the figure. In this class, we will use the convention that inputs which occur earlier in the alphabet appear closer to the output node in a series connection of devices, hence input A connects to the top NMOS.

It is a good idea to make sure every net (wire) in a design has a name. Otherwise, you'll have a tough time tracking down a problem later on one of the unnamed nets. Every net in

your schematic is connected to a named pin or to power or ground except the net between the two series NMOS transistors. Choose Create→Wire name... Enter `nt0` and click on the wire to name it.

Check and Save your schematic, fixing any warnings and errors which may appear.

Part 4 NAND Gate Symbol Create a symbol view for your NAND gate like you did for the inverter in Part 2. Change the label to "nand2_1x" to match the name of your cell. Then choose File→Check and Save to verify and save your symbol. Fix any warnings or errors and run Check and Save again if necessary.

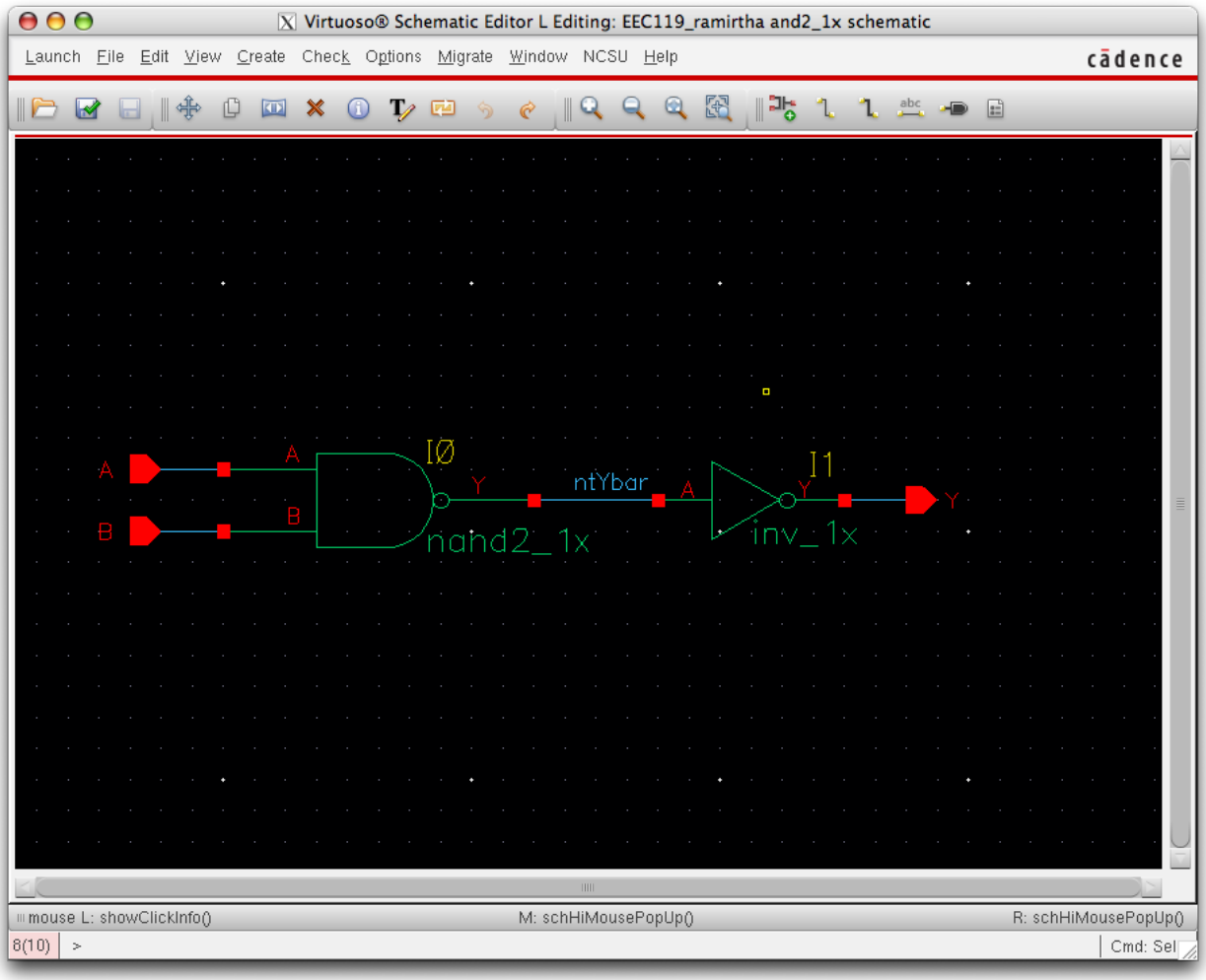

Figure 3: AND2 gate schematic.

Part 5 Design Hierarchy: AND Gate Create a new schematic cell view in your library named `and2_1x`. A CMOS AND gate is a NAND gate followed by an inverter, and you will create a schematic for it by placing instances of the NAND gate and inverter you created above. This is an example of *hierarchical design* in which more complicated cells are composed of simpler cells. Add pins and wire labels. Your final schematic should look like Figure 3. Create a symbol view for your AND gate, modify any labels to be consistent, and Check and Save both the schematic and the symbol.

Part 6 NOR Gate Cell Design Create a new cell in your library called `nor2_1x`. Generate schematic and symbol views following the procedures you used for the previous sections of this lab. You must also choose the transistor sizes for the PMOS and NMOS devices. Make these consistent with the widths and lengths already used for the inverter and NAND gate.

Checkoff

Show your final completed cell views for all three cells to the TA or instructor for checkoff.

Acknowledgments

Parts of this lab were inspired by lab exercises developed by Prof. David Money Harris and others at Harvey Mudd College for the class E158: Introduction to CMOS VLSI Design.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.

[3] E. Brunvand, *Digital VLSI Chip Design with Cadence and Synopsys CAD Tools*, 1st ed. San Francisco: Addison-Wesley, Inc., 2010.

EEC 118 Spring 2011 Lab #3 Part 1 Summary

Name:

Grading:

Part	Checkoff	TA Initials	Date
1 CMOS Inverter Schematic			
2 CMOS Inverter Symbol			
3 NAND Gate Schematic			
4 NAND Gate Symbol			
5 AND Gate Schematic			
5 AND Gate Symbol			
6 NOR Gate Schematic			
6 NOR Gate Symbol			