# EEC 118 Spring 2011 Lab #1:
# NMOS and PMOS Transistor Parameters

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**Reading:** Rabaey Chapter 3 [1].
**Reference:** Kang and Leblebici Chapter 3 [2].

## I OBJECTIVE

The objective of this experiment is to determine the electrical parameters of NMOS and PMOS transistors made with a standard metal-gate CMOS process. These parameters will be used for hand calculations of circuit characteristics in later experiments.

## II PRELAB

Before coming to the laboratory, study Section 3.3 of Rabaey (for more background, see Sections 3.3 and 3.4 of Kang and Leblebici) to learn the definitions of threshold voltage $V_T$, device transconductance parameter or gain factor $k$, body effect coefficient $\gamma$, and output conductance parameter $\lambda$. Also read "Input Protection of MOS Gates" at the end of Lab #1.
Assume the following data:
gate oxide capacitance $C_{ox} = 35$ nF/cm$^2$
$2|\Phi_F| = 0.6$ V
electron mobility $\mu_n = 580$ cm$^2$/V·s
hole mobility $\mu_p = 232$ cm$^2$/V·s
source-drain pn junctions are abrupt junctions

**Problem 1 (20 points)** Compute the I-V curves for NMOS and PMOS transistors using the parameters assumed above. Also, assume that $|V_T| = 1$V, $\lambda = 0$, and the transistor W/L ratio is 10. Plot $I_D$ vs. $|V_{DS}|$ assuming $V_{BS} = 0$V and $|V_{GS}| = 2.5$V for $|V_{DS}| = 3$, 3.5, 4, 4.5, 5, 5.5, 6, and 6.5 Volts (i.e., plot one curve for the NMOS with appropriate polarities for the bias voltages, and a second curve for the PMOS with appropriate polarities for the bias voltages).

# III TRANSISTOR PARAMETERS: MEASUREMENT AND CALCULATION

**Part 1 (10 points)** Use the connections shown in Figure 1 to measure drain current $I_D$ as a function of $V_{DS} = V_{GS}$ for $V_{DS} = 3$, 3.5 4, 4.5, 5, 5.5, 6, and 6.5 Volts for NMOS devices. Make these measurements at $V_{SB} = 0$, 2, and 5 V, making sure that the body is *negative* with respect to the source.

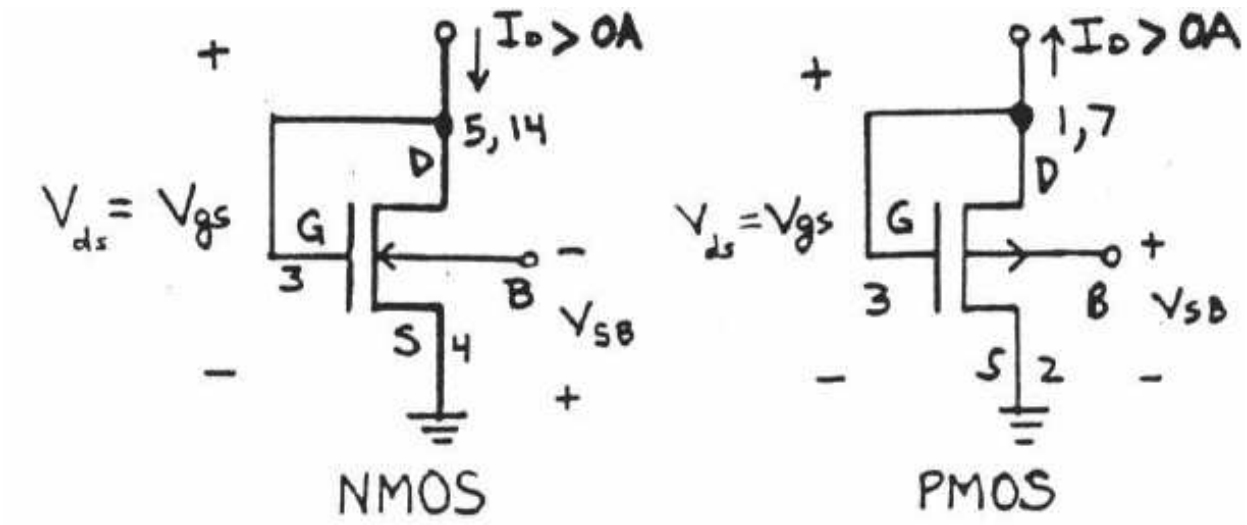


Figure 1: Connections for measuring drain current $I_D$ as a function of $V_{DS} = V_{GS}$.

**Part 2 (10 points)** Repeat Step 1 for a PMOS device. Note that *all polarities are reversed!* The body is *positive* with respect to the source, $V_{DS}$ should be negative for all measurements.

**Part 3 (10 points)** Plot $\sqrt{I_D}$ vs. $V_{GS} = V_{DS}$ for both devices at three values of body bias. Figure 2 shows sample plots. Draw the best fit straight line through your data points. From intercepts, determine $V_T$ for $|V_{BS}| = 0$, 2, and 5 V for each device. From the $V_{BS} = 0$V plot, determine the transconductance parameter $k = k'W/L$. Estimate W/L for both transistors.

**Part 4 (20 points)** With $V_{BS} = 0$ V and $V_{GS} = 2.5$ V, measure drain current $I_D$ at $V_{DS} = 2$, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, and 6 Volts using the connections shown in Figure 3 for both NMOS and PMOS devices.

**Part 5 (10 points)** Using the data from parts 1 and 2, plot $V_T$ vs. $\sqrt{|2\Phi_F| + |V_{BS}|} - \sqrt{|2\Phi_F|}$. Assuming $|2\Phi_F| = 0.6$V for both transistors, estimate $\gamma_P$ and $\gamma_N$.

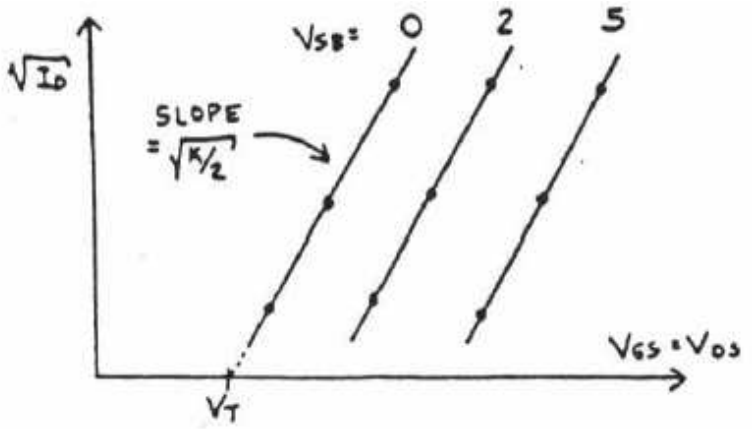


Figure 2: Sample plot of $\sqrt{I_D}$ as a function of $V_{DS} = V_{GS}$ for various $V_{SB}$.

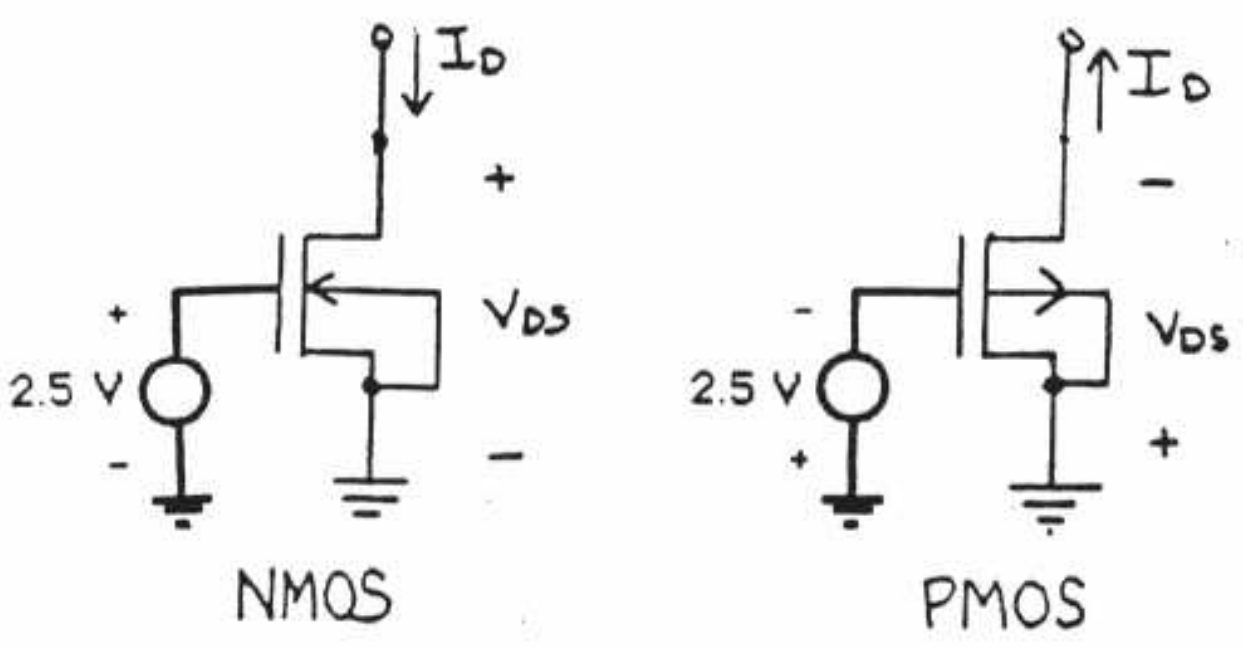


Figure 3: Connections to measure $I_D$ for $V_{BS} = 0$V.

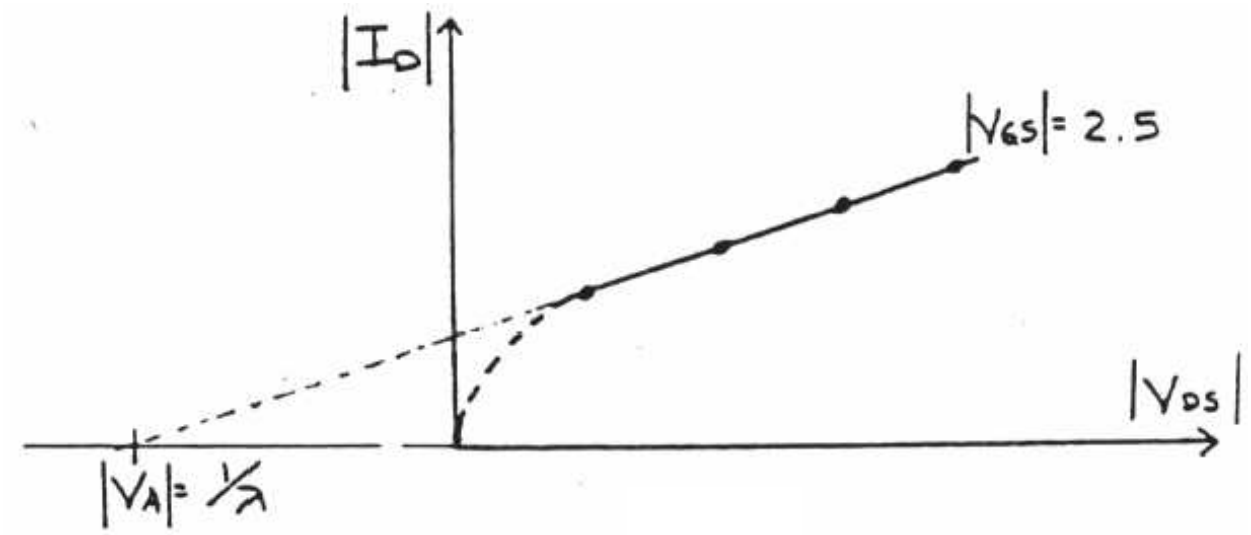


Figure 4: Determining $\lambda$ from the $I_D$ vs. $V_{DS}$ plot.

**Part 6 (10 points)** Using your data from part 4, plot $I_D$ vs. $V_{DS}$ with $V_{BS} = 0$ V for both devices and determine the channel length modulation factor, $\lambda$, from the slopes as shown in Figure 4.

**Part 7 (5 points)** Use the curve tracer to plot $I_D$ vs. $V_{DS}$ for the NMOS transistor with $V_{BS} = 0$V. Sketch at least three curves in your lab notebook for the region $0 \leq V_{GS} \leq 10$V and $0 \leq V_{DS} \leq 10$V. **If the curve tracer isn't working, use a multimeter to measure the appropriate voltages and currents at several bias points to sketch your curves.**

**Part 8 (5 points)** Use the curve tracer to plot $I_D$ vs. $V_{GS}$ for the "diode-connected" NMOS transistor as shown in Figure 5. Sketch at least three curves in your notebook for $0 < V_{GS} < 10$V with $V_{BS} = 0$V. **If the curve tracer isn't working, use a multimeter to measure the appropriate voltages and currents at several bias points to sketch your curves.**

# References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.

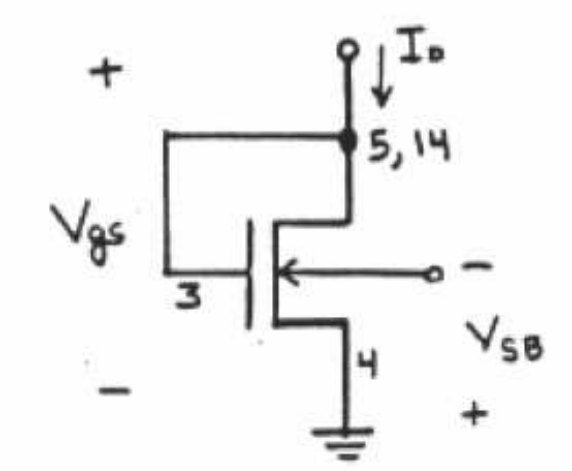


Figure 5: Diode-connected NMOS transistor.

## Input Protection of MOS Gates

Any integrated circuit designed with MOS transistors must be protected against damage due to excessive electrostatic discharges which can sometimes occur during handling and assembly procedures. If no protection were provided, large static voltages appearing across any two pins of a MOS IC could cause oxide rupture.

*Figure 1* shows a schematic of a typical input protection network employed. The network consists of three elements: a resistor, a diode connected to $V_{CC}$, and a diode connected to ground. The resistor will slow down incoming transients and dissipate some of their energy. Connected to the resistor are the two diodes which clamp the input voltage spike and prevent large voltages from appearing across the transistor's gate oxide.

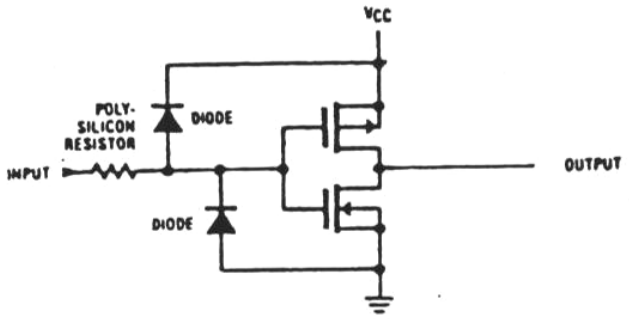


Figure 1. Schematic Diagram of MOS Input Protection Structure

All CMOS ICs have such protection diodes. The 4007 transistor array includes these diodes connected to pin 14 (VCC) and pin 7 (GND or VSS), see Figure 2. To assure these protection diodes are always off, pin 14 must be at or above the most positive supply and pin 7 must be at or below the most negative supply. If necessary, you may keep these protection diodes from interferring with your circuit by floating pin 14 and pin 7.

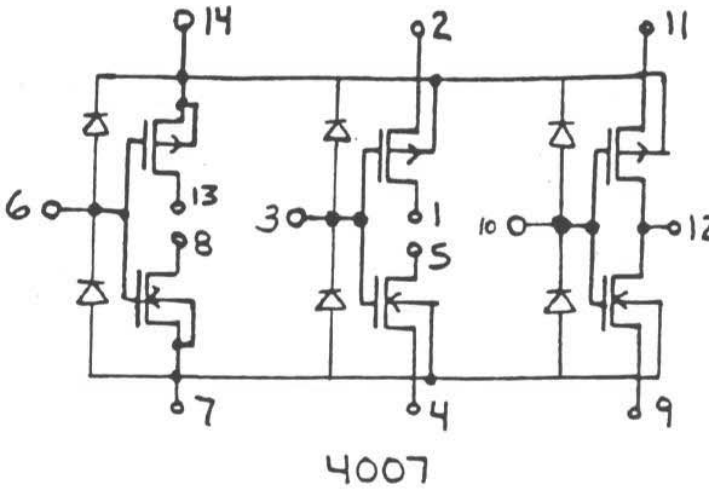


Figure 2.