EEC 118 Spring 2011 Homework #3

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Reading: Rabaey Chapter 5 [1].

Reference: Kang and Leblebici Chapters 5 and 6 [2].

1 CMOS Inverter

Consider a CMOS inverter with the following device parameters for the transistors:

- NMOS: $V_{T0} = 0.8$V, $L = 1.0\mu$m, $\lambda = 0.0$V^{-1}, $\mu C_{ox} = 50\mu$A/V^2

- PMOS: $V_{T0} = -1.0$V, $L = 1.0\mu$m, $\lambda = 0.0$V^{-1}, $\mu C_{ox} = 20\mu$A/V^2

and assume the power supply voltage V_{DD} is 5.0V. The total output load capacitance of this circuit is $C_{out} = 2$pF, which is independent of transistor dimensions.

Problem 1.1 Sizing. Determine the channel width of the NMOS and PMOS transistors such that the switching threshold voltage V_M is equal to 2.2V and the output rise time $t_r = 5$ns.

Problem 1.2 Delay. Calculate the average propagation delay time t_{pd} for the circuit designed in Problem 1.1.

Problem 1.3 V_{DD} Variation. How do the switching threshold V_M and the delay times change if the power supply voltage is dropped from 5V to 3.3V? Provide an interpretation of the results.

2 CMOS Inverter

Consider a CMOS inverter with the same process parameters as in Problem 1. The switching threshold is designed to be equal to 2.4V. A simplified expression of the total output load capacitance is given as:

$$C_{out} = 500 + C_{db,n} + C_{db,p}$$
$$C_{db,n} = (100 + 9W_n)$$
$$C_{db,p} = (80 + 7W_p)$$

where C_{out}, $C_{db,n}$, and $C_{db,p}$ all have units of fF and W_n and W_p are expressed in microns.

Problem 2.1 Sizing. Determine the width of both transistors such that the propagation delay t_{pHL} is smaller than 0.825ns.

Problem 2.2 Rise and Fall Times. Assume now that the CMOS inverter has been designed with dimensions $(W/L)_n = 6$ and $(W/L)_p = 15$, and that the total output load capacitance is 250fF. Calculate the output rise and fall time by computing the average current.

3 CMOS Inverter

Consider a CMOS inverter with the following device parameters for the transistors:

- NMOS: $V_{T0} = 1.0$V, $W/L = 10$, $\lambda = 0.0$V^{-1}, $\mu C_{ox} = 45\mu$A/V^2

- PMOS: $V_{T0} = -1.2$V, $W/L = 20$, $\lambda = 0.0$V^{-1}, $\mu C_{ox} = 25\mu$A/V^2

and assume the power supply voltage V_{DD} is 5.0V with a total output load capacitance of this circuit $C_{out} = 1.5$pF.

Problem 3.1 Rise and Fall Times. Calculate the rise and fall time of the output signal using (1) an exact method (differential equations) and (2) an approximate method (average current).

Problem 3.2 Frequency. Determine the maximum frequency of a periodic square-wave input signal so that the output voltage can still exhibit a full logic swing from 0V to 5V in each cycle.

Problem 3.3 Power. Calculate the dynamic power dissipation at this frequency.

Problem 3.4 Redesign. Assume the output load capacitance is mainly dominated by fixed fan-out components (which are independent of W_n and W_p). We want to re-design the inverter so that the propagation delay times are reduced by 25%. Determine the required channel dimensions of the NMOS and PMOS transistors. How does this re-design influence the switching (inversion) threshold V_M?
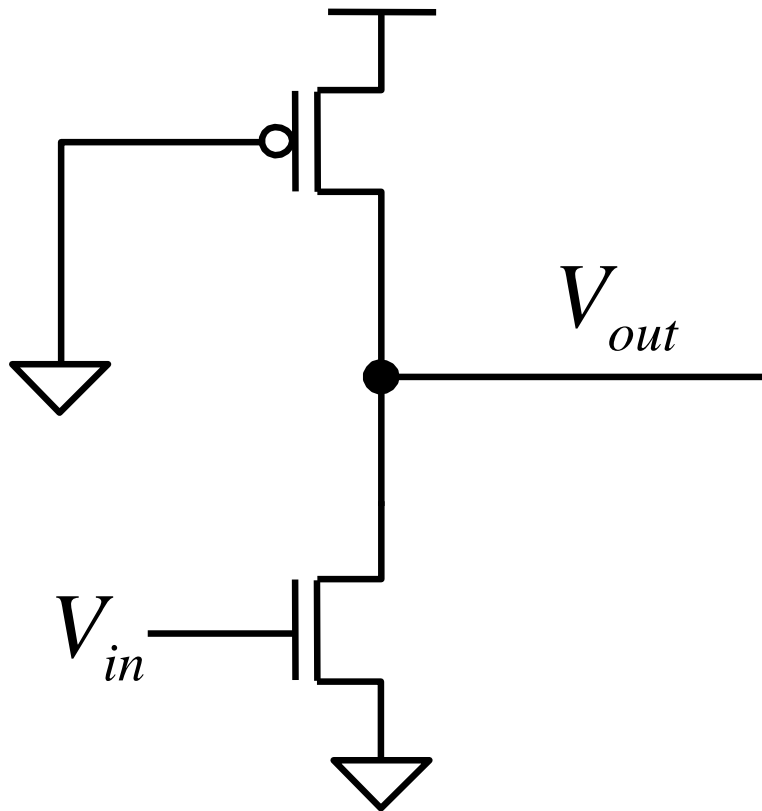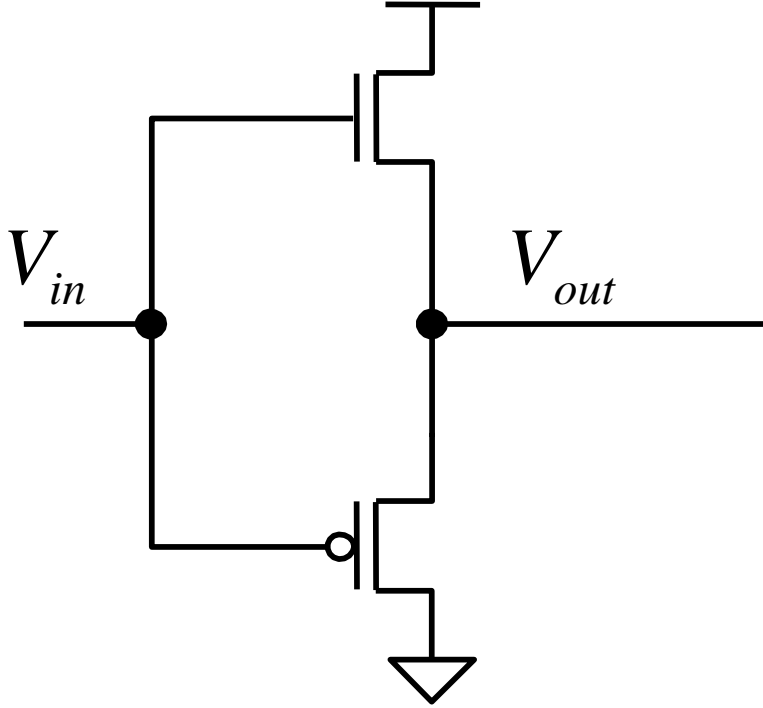
Figure 1: Pseudo NMOS inverter.

Figure 2: Circuit X.

4 Pseudo NMOS Inverter

Problem 4.1 Sizing. Figure 1 shows a circuit known as a pseudo-NMOS inverter since the depletion-mode NMOS device has been replaced with a grounded-gate PMOS. Using the following device parameters for the transistors:

- NMOS: $V_{T0} = 0.6$V, $L = 0.8\mu$m, $\lambda = 0.0$V^{-1}, $\mu C_{ox} = 60\mu$A/V^2

- PMOS: $V_{T0} = -0.7$V, $L = 0.8\mu$m, $\lambda = 0.0$V^{-1}, $\mu C_{ox} = 25\mu$A/V^2

and assuming the power supply voltage V_{DD} is 3.3 V, find the (W_n/W_p) ratio so that the switching (inversion) threshold voltage of the circuit is $V_M = 1.4$V. How does the (W_n/W_p) ratio differ from the ratio you found for the CMOS inverter in Homework #2, Problem 3.1?

Problem 4.2 Noise Margins. Calculate the noise margins for the circuit you designed in Problem 4.1.

Problem 4.3 V_{in} Overdrive. Calculate the required input voltage V_{in} to force the output voltage to 0.6V for the circuit you designed in Problem 4.1.

5 Circuit X

Problem 5.1 Function. Sketch the Voltage Transfer Curve for the circuit drawn in Figure 2. Label the values of V_{OH} and V_{OL}. What is the logical function performed by the circuit?

Problem 5.2 Switching Threshold. Consider the switching threshold V_M for the circuit drawn in Figure 2. Does the definition stated in class make sense for this circuit? Why or why not?

Problem 5.3 Switching Threshold. Determine the switching threshold V_M for the circuit drawn in Figure 2 making any reasonable assumptions about how to properly define it.

Problem 5.4 Discussion. Is the circuit drawn in Figure 2 suitable for use as a logic gate? Why or why not? *Hint: Consider the voltage swing of the circuit.*

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.