Problem 1 (7 points) Complete the following Domino-style dynamic logic three-input AND gate. Size the transistors such that the worst case precharge time (rise time for min. size inverter) equals the worst case evaluation time assuming $V_{DD}=3.3V$, $V_{TN}=|V_{TP}|=1V$, $\mu_N=3\mu_P=300\mu A/V^2$, $\gamma=0$, $\lambda=0$, $W_{min}=1\mu m$, $L_{min}=1\mu m$. Label the inputs A, B, C, clk, the dynamic node Xb, and the output X.
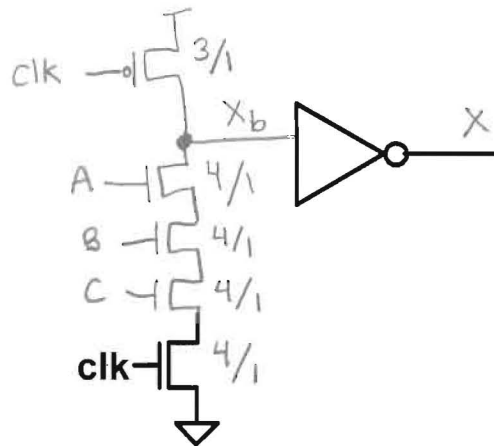
5pts. ckt + labels

2pts. Sizes

Problem 2 (3 points) For the following 1 transistor DRAM cell, fill in the boxes labeling the corresponding wires with the appropriate signal names:
Q: data storage bit
BL: bit line
WL: word line