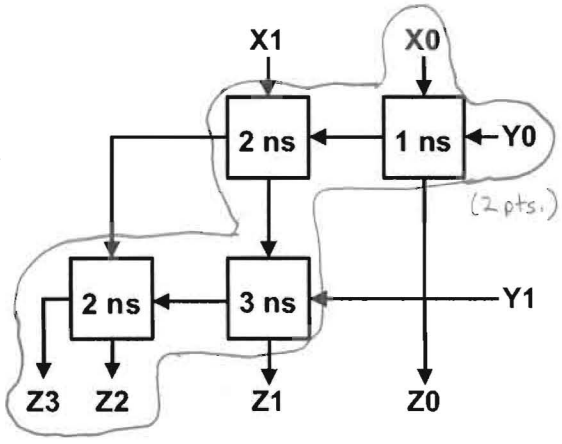
Quiz #3 **EEC118** **Spring 2010**

Name: Solutions Lab Section: _____

Problem 1 (3 points) For the array arithmetic circuit below, circle the longest delay(s) (critical paths) from inputs to outputs. What is the worst case delay?



(2 pts.)

$1 + 2 + 3 + 2 = \boxed{8ns}$ (1 pt.)

Problem 2 (2 points) Suppose the circuit above is pipelined using positive edge-triggered flip-flops with the following parameters: $t_{clk\text{-}Q} = 0.6ns$, $t_{setup} = 0.4ns$, and $t_{hold} = 0.2ns$. What is the fastest clock frequency which can be achieved using pipelining?

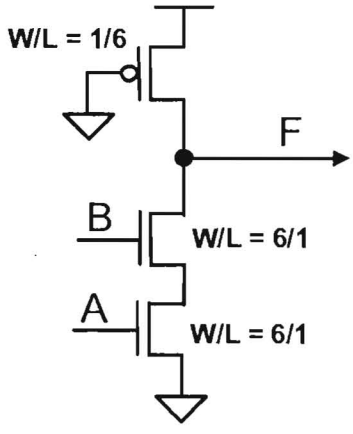
$T_{min} = t_{clk\text{-}Q} + t_{pd} + t_{setup} \Rightarrow T_{min} = 0.6ns + 3ns + 0.4ns = 4ns$

↳ 3ns smallest increment

$\boxed{f_{max} = 250MHz}$

Problem 3 (5 points) For the circuit below, assume: $V_{DD} = 3V$, $V_{T,n} = 1V$, $V_{T,p} = -1V$, $\mu_p C_{ox} = (1/2) \times 10^{-4}\ A/V^2$, $\mu_n C_{ox} = 2 \times 10^{-4}\ A/V^2$, $\lambda = 0$. What logic function does the circuit implement? What is VOL for the circuit? State any reasonable assumptions you make.

NAND



VOL: PMOS sat, NMOS linear

$$\frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p (V_{GSp} - V_{Tp})^2 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_N \left[2(V_{GSn} - V_{Tn})V_{DS,n} - V_{DS,n}^2\right]$$

$$\frac{1}{2}\left(\frac{1}{2} \times 10^{-4}\frac{A}{V^2}\right)\left(\frac{1}{6}\right)(-3V + 1V)^2 = \frac{2 \times 10^{-4} A/V^2}{2}\left(\frac{6}{2}\right)\left[2(3V - 1V)V_{OL} - V_{OL}^2\right]$$

$$5.56 \times 10^{-2} = 4V_{OL} - V_{OL}^2 \Rightarrow V_{OL}^2 - 4V_{OL} + 5.56 \times 10^{-2} = 0$$

$\boxed{V_{OL} = 0.0139\ V}$