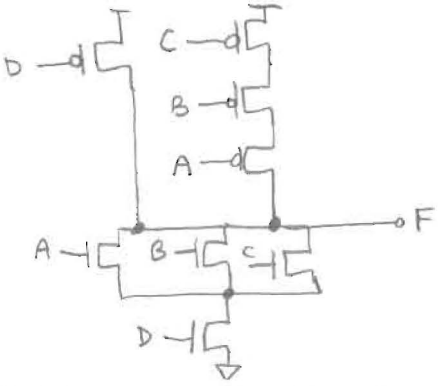
Quiz #2 **EEC118** **Spring 2010**

Name: Solutions Lab Section:_____

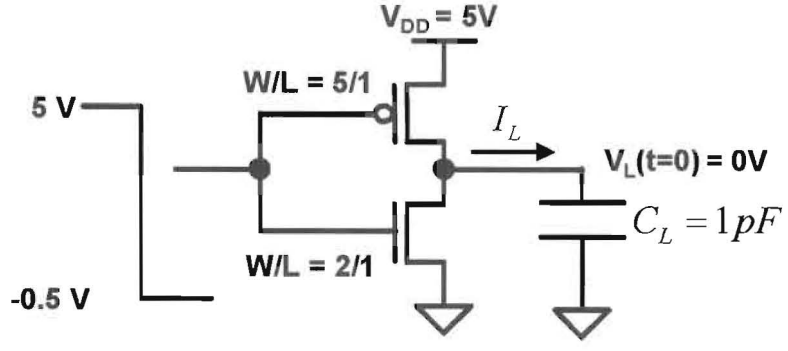
Problem 1 (5 points) Design a four-input static CMOS logic gate which implements the Boolean expression $F = \overline{(A+B+C)\bullet(D)}$. Clearly label all inputs, outputs, and power supply connections. You do not have to pick sizes for the transistors.



other solutions possible...

PUN (2 pts.)
PDN (2 pts.)
Supplies (1 pt.)

Problem 2 (5 points) Suppose a step input is applied at time t=0 to the loaded inverter with dimensions and initial conditions as shown below. Given for all transistors: $V_{T,p} = -1$ V, $\mu_p C_{ox} = (1/5) \times 10^{-3}$ A/V^2, $\lambda_p = 0.1 V^{-1}$, $V_{T,n} = 1$ V, $\mu_n C_{ox} = (1/2) \times 10^{-3}$ A/V^2, $\lambda_n = 0$. What is the current I_L immediately after the step is applied?



NMOS: cutoff (1 pt.)

PMOS: $V_{GS} = -0.5V - 5V = -5.5V < -1V$

$V_{DS} = 0V - 5V = -5V$

$V_{DS} < V_{GS} - V_{T,p}$ since $-5V < -4.5V$ $(-5.5V + 1V)$

sat (1 pt.)

$I_L = I_{DS,p}$

$$I_L = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p (V_{GS,p} - V_{T,p})^2 (1 + \lambda_p V_{DS,p}) \quad (1\text{ pt.})$$

$$= \frac{(1/5\ mA/V^2)}{2}\left(\frac{8}{1}\right)(-5.5 + 1\ V)^2 (1 + 0.1(5V)) \quad (1\text{ pt.})$$

$$= \boxed{15.2\ mA} \quad (1\text{ pt.})$$