EEC 118 Spring 2010 Midterm

Rajeevan Amirtharajah
Dept. of Electrical and Computer Engineering
University of California, Davis

May 3, 2010

This examination is closed book and closed notes. Some formulas which you may find useful are listed in the back of the exam. Calculators are allowed, however using the calculator's function memory to store course related material is NOT allowed and constitutes cheating on this exam.

For all problems, state any assumptions you make, show all work, and clearly mark your answers. Correct but unclear or ambiguous answers will not receive full credit.

Excerpts from the UC Davis Code of Academic Conduct state:

1. Each student should act with personal honesty at all times.
2. Each student should act with fairness to others in the class. This means, for example, that when taking an examination, students should not seek an unfair advantage over other classmates through cheating or other dishonest behavior.
3. Students should take group as well as individual responsibility for honorable behavior. This includes notifying the instructor or TA if you observe cheating.

I understand the honor code and agree to be bound by it.

Signature:
Name (printed): Solutions
Lab Section:

Grading:

Problem	Maximum	Score
1	8	
2	11	
3	23	
4	8	
Total	50	

1 Transistor Biasing

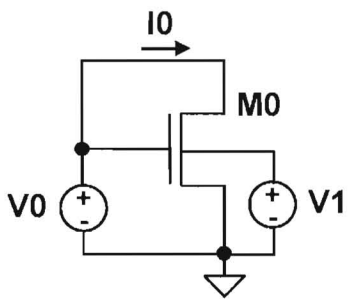


Figure 1: FET biasing circuit.

Problem 1.1 (8 points) Consider the NMOS bias circuit shown in Figure 1. Suppose we know that for the NMOS under bias, $V_{T0} = 1\text{V}$, $W/L = 7/1$, $\gamma = 0.45\text{V}^{1/2}$, $\lambda = 0\ \text{V}^{-1}$, $\mu C_{ox} = 429\ \mu\text{A/V}^2$, and $-2\Phi_F = 0.6$ V. Given that $V0 = 5\text{V}$ and $V1 = -1.6\text{V}$, find the following:

- $V_{Tn} =$ 1.32 V
- $I0 =$ 20.3 mA

$V_{T,n} = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) = 1\text{V} + 0.45\text{V}^{1/2}\left(\sqrt{0.6\text{V} + 1.6\text{V}} - \sqrt{0.6}\right)$ (2pts.)

$= 1.319\text{ V}$ (1pt.)

$V_{DS} = V_{GS} = V_0 = 5\text{V} > V_{T,n} = 1.32\text{V}$, $V_{DS} \geq V_{GS} - V_{T,n} \Rightarrow$ sat (2pts.)

$I_0 = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{T,n})^2(1 + \lambda V_{DS}) = \frac{429\mu\text{A/V}^2}{2}\left(\frac{7}{1}\right)(5 - 1.32\text{V})^2$ (2pts.) ($\lambda = 0$)

$= 20.3\text{mA}$ (1pt.)

Problem 1.1 (cont.)

2 Inverter

Figure 2 shows a circuit model for a CMOS inverter which has been damaged by electrostatic discharge (ESD). Assume all transistor W/L ratios are as shown in Figure 2 and the following transistor and supply voltage characteristics:

$V_{DD} = 5$ V

$\lambda_n = 0.02$ V^{-1}	$\lambda_p = -0.02$ V^{-1}
$V_{T0,n} = 0.9$ V	$V_{T0,p} = -0.9$ V
$\gamma_n = 0.35$ V$^{1/2}$	$\gamma_p = 0.35$ V$^{1/2}$
$\mu_n C_{ox} = 250 \times 10^{-6}$ A/V^2	$\mu_p C_{ox} = 100 \times 10^{-6}$ A/V^2

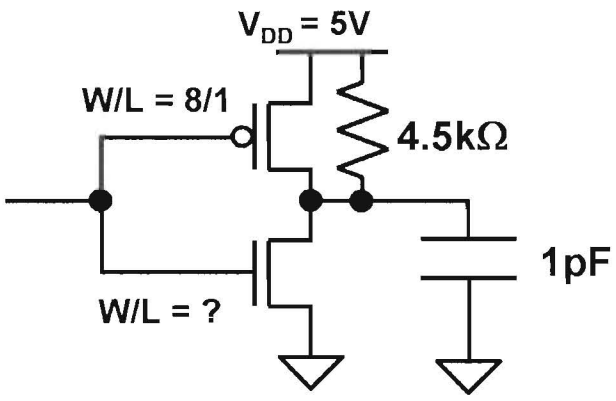


Figure 2: Circuit model for a damaged CMOS inverter.

Problem 2.1 (2 points) What is V_{OH} for the circuit in Figure 2? Justify your answer.

$V_{OH} = 5V$ (1 pt.) $V_{in} = 0V$, NMOS cutoff so $V_{out} \rightarrow V_{DD} = 5V$ (1 pt.)

Problem 2.2 (7 points) When 4V is applied at the inverter input, the output voltage is 0.5V. What is the W/L ratio for the NMOS transistor?

$I_{DS,n} = I_{DS,p} + I_R$ PMOS: $V_{GS} = -1V$, $V_{DS} = -4.5V$, $V_{GS} - V_{T,p} = -0.1\,V > V_{DS}$

sat (1 pt.)

NMOS: $V_{GS} = 4V$, $V_{DS} = 0.5V$, $V_{GS} - V_{T,n} = 3.1\,V > V_{DS}$

linear (1 pt.)

Problem 2.2 (cont.)

$$I_{DS,p} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p (V_{GS} - V_{T,p})^2 (1 + \lambda_p V_{DS})$$

$$= \frac{100\,\mu A/V^2}{2}\left(\frac{8}{1}\right)(-0.1V)^2\left(1 + (-0.02V^{-1})(-4.5V)\right)$$

$$= 4.36\,\mu A \quad (2\text{ pt.})$$

$$I_R = \frac{4.5V}{4.5k\Omega} = 1\,mA$$

$$I_{DS,n} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{T,n})(V_{DS}) - \frac{V_{DS}^2}{2}\right]$$

$$= 250\,\mu A/V^2\left(\frac{W}{L}\right)\left[(4 - 0.9V)(0.5V) - (0.5V)^2/2\right] = 1.004\,mA \approx 1\,mA \quad (2\text{pt.})$$

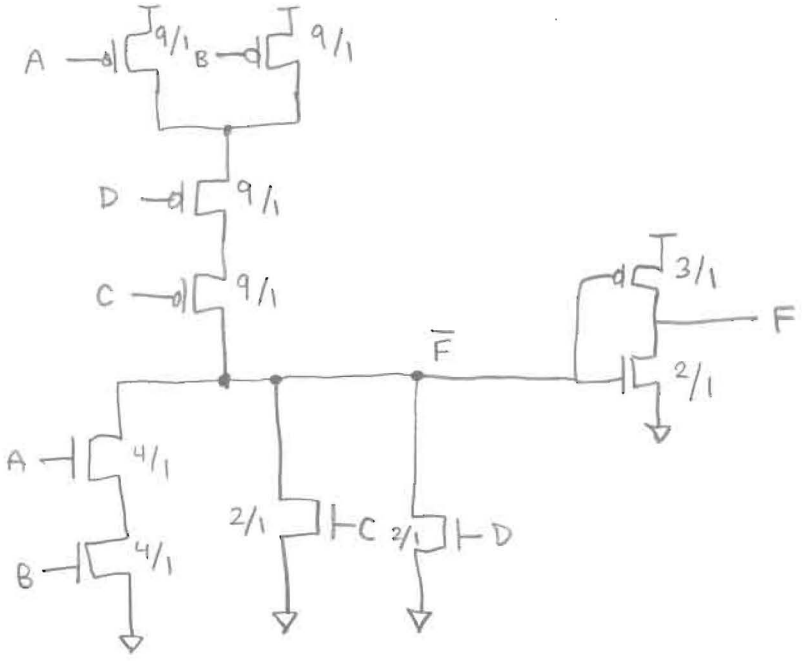
$$\boxed{\left(\frac{W}{L}\right)_N = 2.82} \text{ or } 2.81$$

Problem 2.3 (2 points) How does V_{OL} for the inverter compare to 0.5V (circle one)? Justify your answer.

- $V_{OL} > 0.5\text{V}$
- $V_{OL} = 0.5\text{V}$
- $V_{OL} < 0.5\text{V}$

$V_{in} = V_{OH} = 5V$, PMOS cutoff so V_{OL} slightly lower since NMOS sinks more current.

Problem 3.3 (6 points) Design a circuit that implements F which consists of a single multiple input CMOS logic gate and a static CMOS inverter.



Problem 3.4 (6 points) Assume a minimum-sized inverter has PMOS ratio $W_P/L = 3/1$ and NMOS ratio $W_N/L = 2/1$. Choose appropriate W/L ratios for the transistors in your circuit of Problem 3.3 such that the worst case rise and fall times are the same as a minimum-sized inverter. Indicate the sizes in your schematic above. Be sure to minimize the total area of the transistors.

3 Static CMOS Logic Design

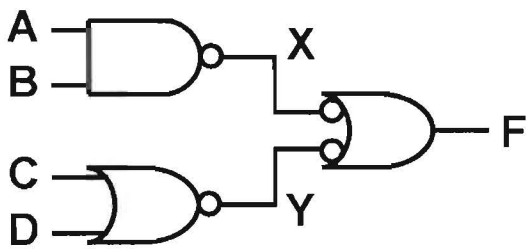
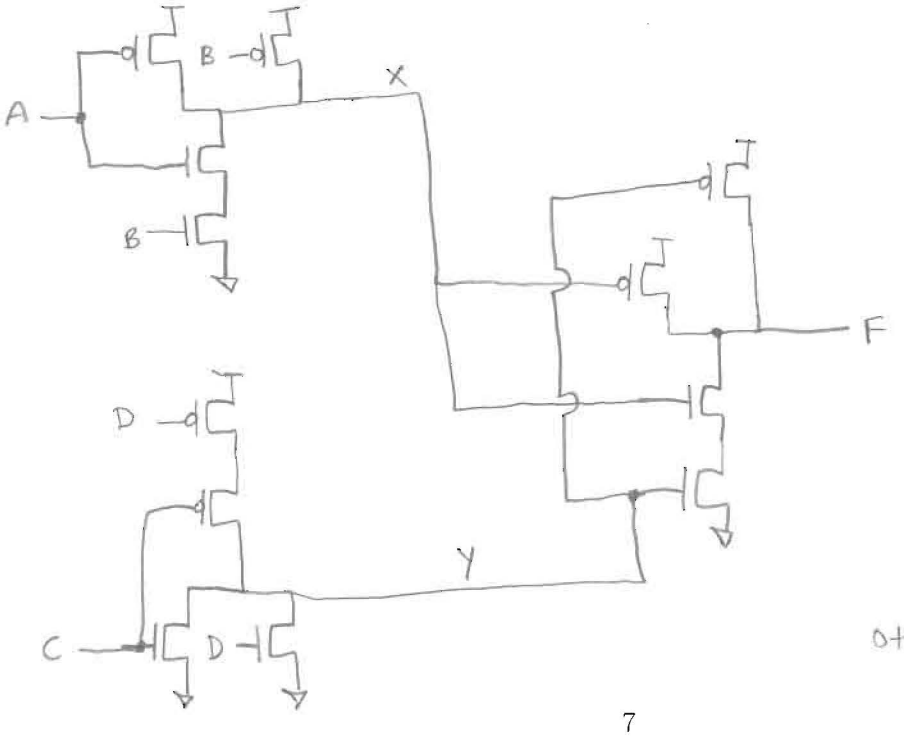


Figure 3: Logic gate network.

Problem 3.1 **(3 points)** Write a Boolean expression for the logic function F in terms of inputs A, B, C, and D implemented by the logic gate network in Figure 3.

$F = A \cdot B + C + D$ or $F = \overline{\overline{A \cdot B} + \overline{C + D}}$ or others possible

Problem 3.2 **(8 points)** Implement the circuit in Figure 3 using static CMOS circuits for the logic gates. You do not have to choose transistor sizes. Be sure to label all inputs, outputs, and other circuit nodes.



Other solutions possible...

4 Ring Oscillator

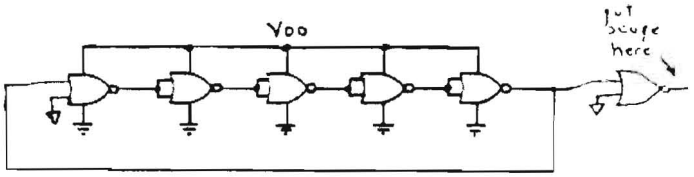


Figure 4: NAND gate ring oscillator.

Problem 4.1 (4 points) For the ring oscillator circuit shown in Figure 4 from Lab 2, use the switch RC model and the following parameters for the equivalent inverters which model the NAND gates: $R_p = 12.5k\Omega$, $R_n = 10.5k\Omega$, and $C_L = 87\text{fF}$ (C_L is the load capacitance seen by **each** NAND gate). What frequency would be measured by the scope probe when placed as shown in the figure?

$T = 2N\, t_{pd} = 2N\left(\frac{t_{pLH} + t_{pHL}}{2}\right) = 2N\left(\frac{0.69}{2}\right)(R_p + R_n)C_L$ (2pt.)

$= 2(5)\left(\frac{0.69}{2}\right)(12.5\text{k}\Omega + 10.5\text{k}\Omega)(87\text{fF}) = 6.9\text{ ns}$ (1pt.)

$\boxed{f = \frac{1}{T} = 145\text{ MHz}}$ (1pt.)

Problem 4.2 (4 points) Suppose that the transistor **widths** for the NAND gates in the oscillator of Figure 4 are doubled such that the total $C_{gd,PMOS}$ at the NAND output increases from an initial value of 17fF to 34fF and the total $C_{gd,NMOS}$ at the NAND output increases from 6fF to 12fF. All other capacitances stay the same. What would the new oscillator output frequency be? You can ignore any capacitances not connected to the output.

W_P doubled $\Rightarrow R_P \to R_P/2$, $C_{gdP} \to C_{gdp} \cdot 2$ (1pt.)

W_N doubled $\Rightarrow R_N \to R_N/2$, $C_{gdN} \to C_{gdN} \cdot 2$ (1pt.)

$C_L = C_{fixed} + 2C_{gdp} + 2C_{gdn}$, $C_L = 87\text{fF} + 2\cdot 17\text{fF} + 2\cdot 12\text{fF} = 133\text{ fF}$ (1pt.)

($2C_{gdp}$: Miller effect)

$f = 189.5\text{MHz} = \boxed{190\text{ MHz}}$

Miscellaneous Formulas

MOSFET Threshold Voltage

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

$$\gamma = \frac{\sqrt{2q \cdot N_A \cdot \epsilon_{Si}}}{C_{ox}}$$

CMOS Inverter Switching Threshold

$$V_{TH} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot (V_{DD} - |V_{T0,p}|)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

CMOS Inverter Propagation Delay Times

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})} \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)} \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

Switch Model Propagation Delay Times

$$t_{PHL} = 0.69 R_n C_L$$

$$t_{PLH} = 0.69 R_p C_L$$

$$t_f = 2.2 R_n C_L$$

$$t_r = 2.2 R_p C_L$$

Junction Capacitances

$$C_{j0} = \sqrt{\frac{\epsilon_{Si} \cdot q}{2}} \left(\frac{N_A N_D}{N_A + N_D} \right) \frac{1}{\phi_0}$$

$$C_j(V) = \frac{AC_{j0}}{\left(1 - \frac{V}{\phi_0}\right)^m}$$

$$C_{eq} = AC_{j0}K_{eq}$$