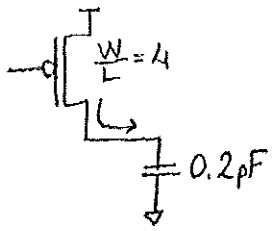
EEC 118 HOMEWORK #6 SOLUTIONS

(1) K&L 9.1

Let's use average current method.



$$I_{avg,LH} = \frac{1}{2}\left[i_{c1}(V_{in}=V_{OL},\ V_{out}=0) + i_{c2}(V_{in}=V_{OL},\ V_{out}=V_{50\%})\right]$$

$$I_{avg,LH} = \frac{1}{2}\left[i_{c1}(V_{in}=0, V_{out}=0) + i_{c2}(V_{in}=0,\ V_{out}=2.5)\right]$$

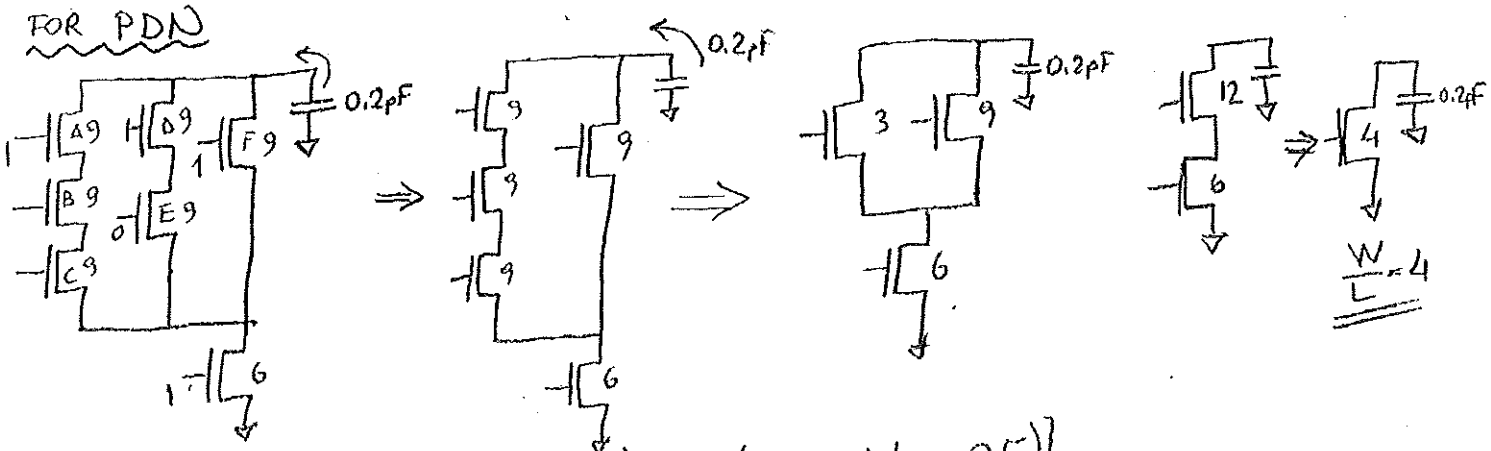
for i_{c1} $V_{DS} \geq V_{GS}-V_{tn}$, PMOS in sat $\quad i_{c1} = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(|V_{GS}|-|V_t|)^2$

$= 800\mu A$

for i_{c2} $V_{DS} \not\geq V_{GS}-V_{tn}$ PMOS in linear. $\quad i_{c2} = \frac{1}{2}k_p'\left(\frac{W}{L}\right)_p\left[2(|V_{GS}|-|V_t|)|V_{DS}| - V_{DS}^2\right] = 687.5\mu A$

$I_{avg,LH} = 743.75\mu A$

FOR PDN



$$I_{avg,HL} = \frac{1}{2}\left[i_{c1}(V_{in}=5, V_{out}=5) + i_{c2}(V_{in}=5, V_{out}=2.5)\right]$$

for i_{c1} $V_{DS} \geq V_{GS}-V_{tn}$, then NMOS in sat $\quad i_{c1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n(V_{GS}-V_t)^2 = 1600\mu A$

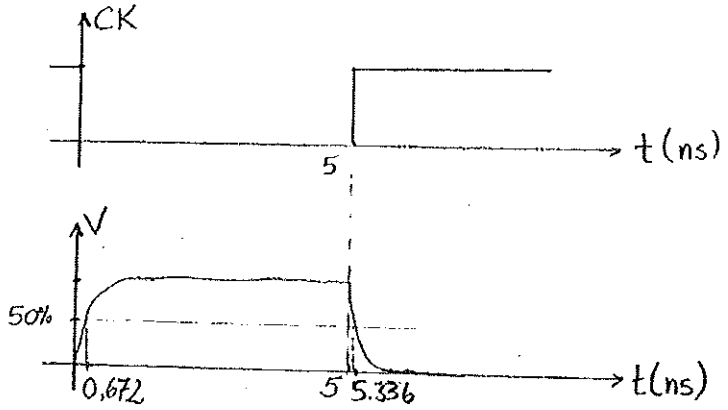
for i_{c2} $V_{DS} < V_{GS}-V_t$, then NMOS in linear $\quad i_{c2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_n\left[2(V_{GS}-V_t)V_{DS} - V_{DS}^2\right]$

$= 1375\mu A$

$I_{avg,HL} = 1487.5\mu A$

(1) cont.'ed

$$\tau_{PHL} = \frac{C_{load}.(V_{OH} - V_{50\%})}{I_{avg,HL}} \simeq 0.336\,ns \qquad \tau_{PLH} = \frac{C_{load}.(V_{50\%} - V_{OL})}{I_{avg,LH}} \simeq 0.672\,ns$$



(2.1) K&L 9.7a

Basically total charge will be shared by two caps (C_x & C_y). Here we have $C_x = C_y$ then precharged node Voltage (5v) will drop to $V_x = \frac{V_{DD}}{2} = 2.5v$ in the case of $V_{y_{init}} = 0$ ✓. But here $V_{y\,initial}$ is not known.

then $V_{x_{final}}(C_x + C_y) = V_{x_{init}} C_x + C_y . V_{y_{init}}$

$$V_{x_{final}} = \frac{5}{\frac{5C_x + V_{y_{init}} C_y}{C_x + C_y}}$$

$$V_{x_{final}} = \frac{5 + V_{y_{init}}}{2}$$

(2.2) Checking all circumstances, we see when input B is 0, (which is the case of 2.1) input A is high, the charge sharing will result in equalizing the voltages at node X and Y. Thus the voltage drop at node X may cause the voltage to the V_M of the inverter if $C_x = C_y$, $k_p = k_n$

Then we want to determine k_p and k_n such that V_M is below the equalized Voltage.

(2.2) cont.

Assume $C_X = C_Y$

$$V_M = \frac{V_{TO,n} + \sqrt{\frac{1}{k_R}}(V_{DD} + V_{TO,P})}{1 + \sqrt{\frac{1}{k_R}}} \qquad k_R = \frac{k_n}{k_p}$$

$$= \frac{1 + \sqrt{\frac{1}{k_P}}(5-1)}{1 + \sqrt{\frac{1}{k_P}}} < 2.5 \longrightarrow (C_X = C_Y).$$

$$\Rightarrow \frac{k_P}{k_n} < 1$$