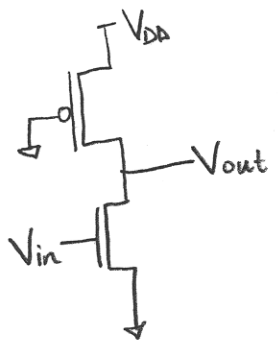
EEC118 HOMEWORK SOLUTIONS 3

(1.1) $V_{TH} = V_{in} = V_{OUT} = 1.4v$



PMOS $|V_{DS}| = 1.9v$ $|V_{GS}| = 3.3v$ $|V_{To}| = 0.7v$

$|V_{DS}| \overset{?}{>} |V_{GS} - V_{To}|$ $\quad 1.9 \not> 2.6$ Linear

NMOS $V_{DS} = 1.4$ $V_{GS} = 1.4$ $\longrightarrow V_{DS} > |V_{GS} - V_{To}|$ ✓ saturation

$$I_{DN} = \frac{\mu_n C_{ox}}{2} \frac{W_n}{L} (1.4 - 0.6)^2$$

$$I_{DP} = \frac{\mu_p C_{ox}}{2} \frac{W_p}{L} \left(2(3.3 - |-0.7|)1.9 - (1.9)^2\right)$$

$I_{DN} = I_{DP}$

$\frac{W_n}{W_p} = 4.08$

It is 4.38 times bigger than that $\frac{W_n}{W_p}$

We need bigger NMOS here.

(1.2) V_{OH}

$V_{in} = 0 \Longrightarrow$ then NMOS is cut-off,

$V_{GSP} > V_{TOP}$ conducts but no current then

no voltage drop at $V_{DSP} \Longrightarrow V_{out} = V_{OH} = 3.3v$

V_{OL}

assume $V_{in} = V_{OH} = V_{DD} = 3.3v$ then NMOS is linear b/c $V_{DSN} < (V_{GSN} - V_{TON})$

PMOS is in saturation

then $I_{DN} = \frac{\mu_n C_{ox}}{2} \frac{W_n}{L} \left(2(3.3 - 0.6)V_{OL} - V_{OL}^2\right)$ $\quad I_{DP} = \frac{\mu_p C_{ox}}{2} \frac{W_p}{L} \left(|3.3| - |-0.7|\right)^2$

$I_{DN} = I_{DP} \Longrightarrow V_{OL}^2 - 5.4V_{OL} + 0.69 = 0$ $\quad V_{OL} = 0.13v$

(1.2) cont'ed

V_{IL}

$V_{in} = V_{IL}$ then NMOS $\Rightarrow V_{DS} > (V_{GS} - V_{to})$ saturation

PMOS $\Rightarrow$ Linear region

$$I_{DN} = I_{DP} \quad \frac{\mu_n C_{ox}}{2}\frac{W_n}{L}(V_{IL}-0.6)^2 = \frac{\mu_p C_{ox}}{2}\frac{W_p}{L}\left(2(3.3-1-0.71)(V_{out}-3.3)-(V_{out}-3.3)^2\right)$$

(I) $$\frac{60}{25}\cdot\frac{W_n}{W_p}(V_{IL}-0.6)^2 = -5.2(V_{out}-3.3)-(V_{out}-3.3)^2$$

$\frac{\partial V_{out}}{\partial V_{in}} \Rightarrow$ $$9.79(2(V_{IL}-0.6) = -5.2\left(\frac{\partial V_{out}}{\partial V_{in}}\right)^{-1} - 2\cdot\left(\frac{\partial V_{out}}{\partial V_{in}}\right)^{-1}(V_{out}-3.3)$$

$$V_{out} = 9.79V_{IL} - 5.175$$ Plug V_{out} in (I)

$$9.79(V_{IL}-0.6)^2 = -5.2(9.79V_{IL}-5.175-3.3)-(9.79V_{IL}-5.175-3.3)^2$$

$$105.63V_{IL}^2 - 126.78V_{IL} + 31.28 = 0 \qquad V_{IL} = 0.85v$$

V_{IH}

$V_{in} = V_{IH}$ then NMOS $V_{DS} \not> V_{GS} - V_t$ linear

PMOS $V_{DS} > V_{GS} - V_t$ saturation

$$\frac{\mu_n C_{ox}}{2}\frac{W_n}{L}\left[2(V_{IH}-0.6)V_{out} - V_{out}^2\right] = \frac{\mu_p C_{ox}}{2}\frac{W_p}{L}(3.3-0.7)^2$$

(II) $$2(V_{IH}-0.6)V_{out} - V_{out}^2 = \frac{25}{60}\times\frac{1}{4.08}\times 6.76$$

$\frac{\partial V_{out}}{\partial V_{in}} \Rightarrow$ $$2V_{out} + 2(V_{IH}-0.6)\left(\frac{\partial V_{out}}{\partial V_{in}}\right)^{-1} - 2V_{out}\cdot\left(\frac{\partial V_{out}}{\partial V_{in}}\right)^{-1} = 0 \quad \Rightarrow V_{out} = 0.5V_{IH} - 0.3$$

Plug V_{out} in (II)

$$2(V_{IH}-0.6)(0.5V_{IH}-0.3)-(0.5V_{IH}-0.3)^2 = 0.69$$

$$0.75V_{IH}^2 - 0.9V_{IH} - 0.42 = 0 \qquad V_{IH} = 1.56v$$

$$NM_L = V_{IL} - V_{OL} = 0.72v$$

$$NM_H = V_{OH} - V_{IH} = 1.74v$$

(1.3) Want $V_{OL} = 0.6V$

PMOS: $V_{GS} = -3.3V$, $V_{DS} = -2.7V < V_{GS} - V_{TP} = -3.3V - -0.7V = -2.6V$

saturation

NMOS: $V_{DS} = V_{OL} = 0.6V$

Assume linear

$$I_{DS,N} = I_{DS,P} \Rightarrow \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_N \left[2(V_{in} - V_{T\emptyset,N})V_{OL} - V_{OL}^2\right] = \frac{\mu_p C_{ox}}{2}\left[-V_{DD} - V_{T\emptyset,P}\right]^2$$

$$\frac{60\mu A/V^2}{2}(8)\left[2(V_{in} - 0.6V)(0.6V) - (0.6V)^2\right] = \frac{25\mu A/V^2}{2}\left[-3.3V + +0.7V\right]^2(12)$$

$\boxed{V_{in} = 4.42V}$ $V_{GS} = V_{in}$, $4.42V - 0.6V = 3.82V > V_{DS} = 0.6V$ linear ✓

(2.1) The highest voltage V_{out} can reach before NMOS cuts off is $V_{DD} - V_{T,n} \Rightarrow \boxed{V_{OH} = V_{DD} - V_{T,n}}$

The lowest voltage V_{out} can reach before PMOS cuts off is $0V - V_{T,P} \Rightarrow \boxed{V_{OL} = |V_{T,P}|}$ $(V_{T,P} < 0)$

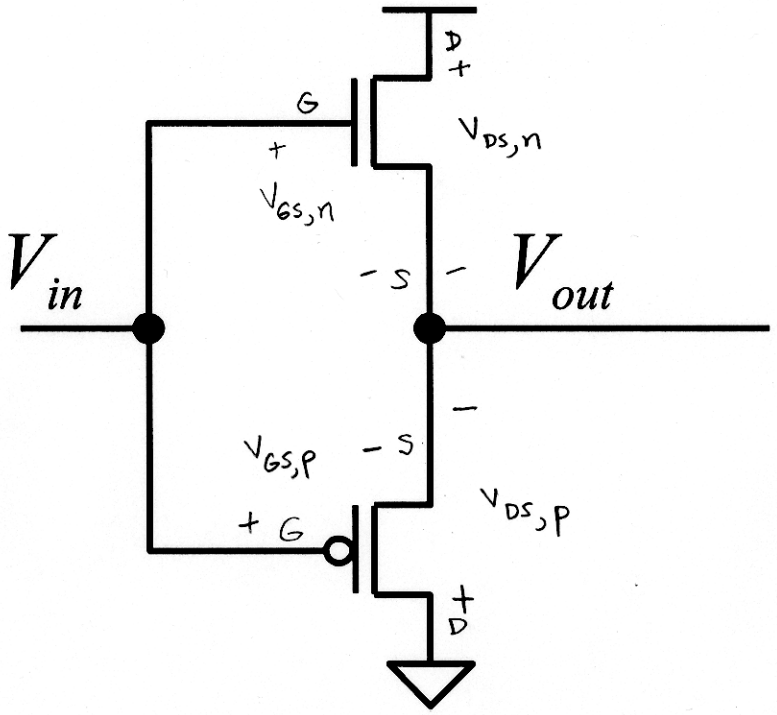
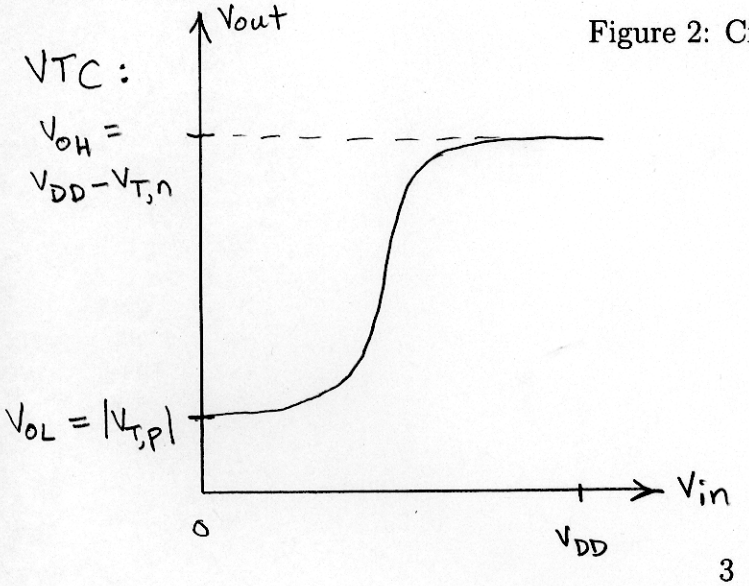


Figure 2: Circuit X.

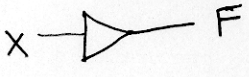


Truth table:

in	out
0	0
1	1

buffer!

$\boxed{F = X}$



(2.2) Not enough information to calculate exactly, so make some plausible assumptions:

Assume $K_R = 1$ (just like ideal CMOS inverter)

$V_{T,n} = |V_{T,p}|$ (symmetric device thresholds)

$V_{DD} > V_{T,n} + |V_{T,p}|$ (devices both on at same time under <u>some</u> V_{in} conditions)

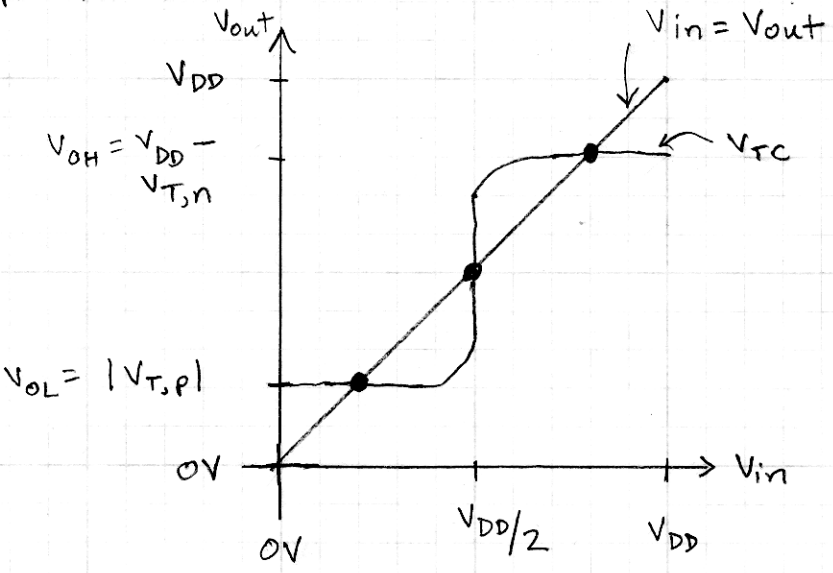
Under these assumptions, the device currents for both NMOS and PMOS are <u>equal</u> for equal V_{GS} ($V_{GS,n} = V_{GS,p}$).

Since $V_{TH} = V_{in} = V_{out} \Rightarrow V_{GS,p} = V_{GS,n} = 0 \Rightarrow$ NMOS, PMOS both in <u>cutoff</u>, $I_{D,n} = I_{D,p} = 0$

However, they have finite impedance due to <u>subthreshold</u> conduction, these will be equal, therefore:

$$\boxed{V_{TH} = V_{DD}/2}$$

Graphical solution: (same assumptions as above)



Three points where V_{TC} meets $V_{in} = V_{out}$ line. Two of those points are where $V_{out} = V_{OL}$ and $V_{out} = V_{OH} \Rightarrow$ circuit is <u>not</u> switching $\therefore$

$$\boxed{V_{TH} = V_{DD}/2}$$ (third point)

(2.3) Suppose the input can swing between 0V and V_{DD}:

$$\Delta V_{in} = V_{DD} - 0\,V = V_{DD}$$

The output can only swing from

$$\Delta V_{out} = V_{OH} - V_{OL} = V_{DD} - V_{T,n} - |V_{T,p}| < \Delta V_{in}$$

2.4 Normally, we want logic gate output swings to be <u>larger</u> than input swings (this is called level restoration) so that input noise affects the output less. Therefore, this buffer is <u>not</u> suitable as a logic gate since $\Delta V_{out} < \Delta V_{in}$.