EEC 118 Spring 2010 Final

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This examination is closed book and closed notes. You are allowed one 8.5 x 11 inch sheet (both sides) on which you may write formulas. Calculators are allowed, however using the calculator's function memory to store course related material is NOT allowed and constitutes cheating on this exam.

For all problems, state any assumptions you make, show all work, and clearly mark your answers. Correct but unclear or ambiguous answers will not receive full credit.

Excerpts from the UC Davis Code of Academic Conduct state:

1. Each student should act with personal honesty at all times.
2. Each student should act with fairness to others in the class. This means, for example, that when taking an examination, students should not seek an unfair advantage over other classmates through cheating or other dishonest behavior.
3. Students should take group as well as individual responsibility for honorable behavior. This includes notifying the instructor or TA if you observe cheating.

I understand the honor code and agree to be bound by it.

Signature: Solutions
Name (printed):
Lab Section:

Grading:

Problem	Maximum	Score	Problem	Maximum	Score
1	19		4	20	
2	18		5	13	
3	30				
Total	100				

Device Parameters

For **all** problems in this exam, assume we are using enhancement-type NMOS and PMOS transistors which have the characteristics shown in Table 1, unless otherwise specified. All dimensions are in microns. Also, assume **minimum** length devices unless otherwise specified.

Parameter	NMOS	PMOS
V_{T0}	0.7 V	-0.7 V
μC_{ox}	300 μA/V^2	100 μA/V^2
γ	0 V$^{1/2}$	0 V$^{1/2}$
W_{min}	1.0μm	1.0μm
L_{min}	1.0μm	1.0μm
λ	0.0 V^{-1}	0.0 V^{-1}
V_{DD}	5 V	

Table 1: Assumed Transistor Parameters.

Problem 1.3 (**5 points**) Assuming $V_{Tn} = 1.0\text{V}$, find the value of $V0$ which yields a current $I0 = 1\text{mA}$.

Saturation $I_\phi = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{T,n})^2$ (2 pts.)

$1\text{ mA} = \frac{300\,\mu\text{A/V}^2}{2}\left(\frac{4}{1}\right)(V_\phi - 1.0\text{V})^2$ (2 pts.)

$\boxed{V_\phi = 2.291\text{ V}}$ (1 pt.)

Problem 1.4 (**4 points**) Suppose $\lambda = 0.06\text{V}^{-1}$. Assuming the value of $V0$ which you found in Problem 1.3, what is the new value of $I0$?

$I_\phi' = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_\phi - V_{T,n})^2(1 + \lambda V_\phi)$ (2 pts.)

$= (1\text{ mA})(1 + 0.06\text{V}^{-1} \cdot 2.291\text{V})$ (1 pt.)

$= \boxed{1.137\text{ mA}}$ (1 pt.)

1 Transistor Current Biasing

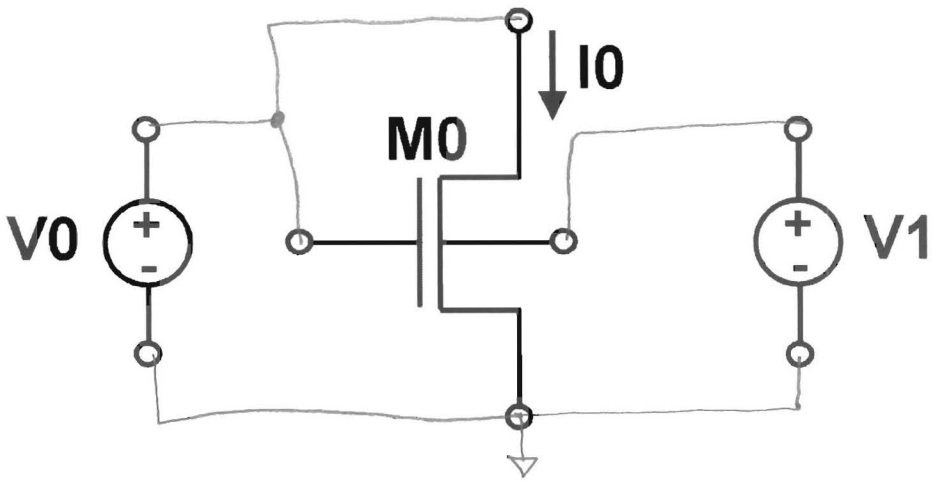


Figure 1: Voltage setup for NMOS biasing.

Assume that NMOS transistor $M0$ in Figure 1 has $W/L = 4$, $\gamma = 0.33\text{V}^{\frac{1}{2}}$, and $-2\Phi_F = 0.6\text{V}$ in the following problems.

Problem 1.1 (5 points) Connect the voltage souces $V0$ and $V1$ to the transistor $M0$ terminals in Figure 1 such that (a) $M0$ is in either saturation or cutoff (but not in the linear regime) by adjusting $V0$ and (b) adjusting $V1$ varies the threshold voltage V_{Tn}. (1 pt. ea. wire)

Problem 1.2 (5 points) Find the value of $V1$ which yields $V_{Tn} = 1.0\text{V}$.

$$V_{T,n} = V_{T\phi,n} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \qquad (2\text{ pts.})$$

$$1.0\text{V} = 0.7\text{V} + (0.33\text{V}^{1/2})\left(\sqrt{|0.6\text{V} - V_1|} - \sqrt{|0.6\text{V}|}\right) \qquad (2\text{ pts.})$$

$$|0.6\text{V} - V_1| = \left[\left(\frac{1.0 - 0.7}{0.33}\right) + \sqrt{0.6}\right]^2$$

$$\boxed{V_1 = -2.235\text{ V}} \qquad (1\text{ pt.})$$

2 Inverter Characteristics

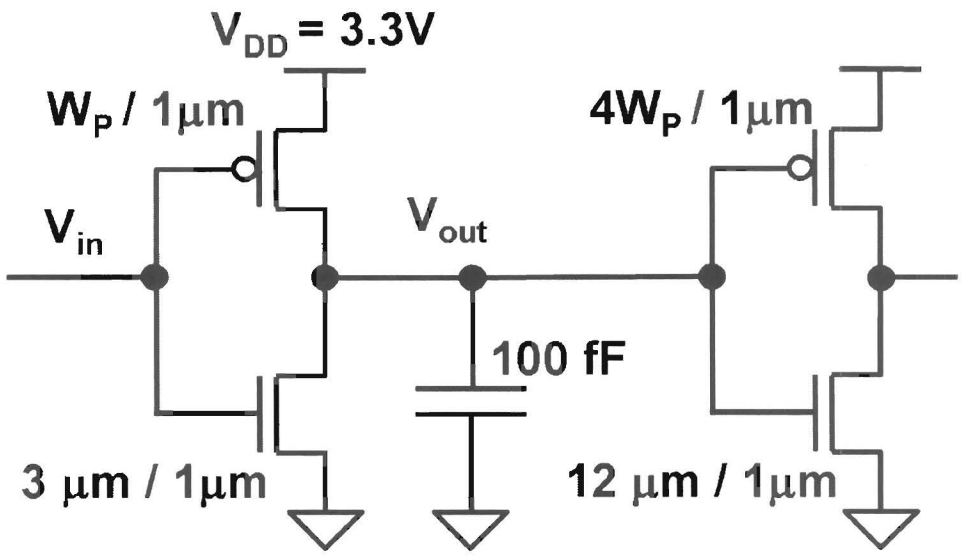


Figure 2: Cascaded inverters forming part of a buffer chain.

Problem 2.1 (12 points) Figure 2 shows a CMOS inverter driving a 4X bigger inverter. Neglecting all FET capacitances, find W_P such that the 10%-90% rise time (t_r) of V_{out} equals 140ps. Assume an ideal step voltage on V_{in} and approximate the charging current by averaging the initial and final drain currents.

$$t_r = \frac{C\Delta V}{I_{av}} \Rightarrow I_{av} = \frac{C\Delta V}{t_r} = \frac{(100\,fF)(0.8 \times 3.3V)}{140\,ps} = 1.88\,mA \qquad (3\,pts.)$$

Ideal Step: NMOS cutoff

$V_{out} = 0.1(3.3V) = 0.33V$
$V_{in} = 0V$
$V_{T\phi,P} = -0.7V$

$V_{GS} - V_{T\phi P} = -3.3V + 0.7V = -2.6V$
$V_{DS} = 0.33V - 3.3V = -2.97V$
$\Rightarrow$ PMOS sat (1 pt.)

$$I_{DS,P(1)} = \frac{\mu_P C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{T\phi,P})^2 = \frac{100\mu A/V^2}{2}\left(\frac{W_P}{1}\right)(-2.6V)^2 = 338\frac{\mu A}{\mu m} W_P \qquad (2\,pts.)$$

$V_{out} = 0.9(3.3V) = 2.97V \Rightarrow V_{DS} = -0.33V \Rightarrow$ PMOS lin (1 pt.)

$$I_{DS,P(2)} = \mu_P C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS} - V_{T\phi,P})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Problem 2.1 (cont.)

$$I_{DS,P(2)} = 100\frac{\mu A}{V^2}\left(\frac{W_P}{1}\right)\left[(-2.6V)(-0.33V) - \frac{(-0.33V)^2}{2}\right] \quad (2\text{ pts.})$$

$$= 80.4\frac{\mu A}{\mu m}(W_P)$$

$$W_P = \frac{1.88\text{ mA}}{\frac{1}{2}(338\mu A/\mu m + 80.4\mu A/\mu m)} = \boxed{9\ \mu m} \quad (3\text{ pts.})$$

Problem 2.2 (6 points) Assuming the value for W_P you found in Problem 2.1 and the capacitances in Table 2 in addition to the 100fF in the figure, what is the new value of t_r?

Capacitance/Width (fF/μm)	PMOS	NMOS
C_{gs}	0.8	0.8
C_{gd}	0.8	0.8
C_{db}	1.0	0.9
C_{sb}	1.0	0.9

Table 2: PMOS and NMOS capacitances per unit width.

(4 pts.)

$$C_{TOT} = 100\text{ fF} + \underbrace{3\mu m\, C_{gd,n}\cdot 2 + W_P C_{gd,P}\cdot 2}_{\text{1st inverter output + Miller effect}} + \underbrace{3\mu m\, C_{db,n} + W_P C_{db,P}}_{\text{1st inverter output}} + \underbrace{4W_P C_{gs,P} + 12\mu m\, C_{gs,n}}_{\text{2nd inverter input}}$$

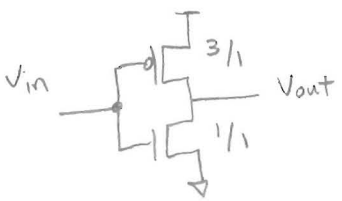
$$= 100\text{ fF} + 3\mu m(0.8\text{ fF}/\mu m)2 + 9\mu m(0.8\text{ fF}/\mu m)2 + 3\mu m(0.9\text{ fF}/\mu m) + 9\mu m(1.0\text{ fF}/\mu m)$$
$$+ 4(9\mu m)(0.8\text{ fF}/\mu m) + 12\mu m(0.8\text{ fF}/\mu m)$$

$$= 169.3\text{ fF} \quad (1\text{ pt.})$$

$$t_r' = \frac{169.3\text{ fF}}{100\text{ fF}}(140\text{ ps}) = \boxed{237\text{ ps}} \quad (1\text{ pts.})$$

3 Static CMOS, Dynamic Logic, and Pseudo NMOS

Problem 3.1 (3 points) Draw and label the schematic for a minimum-sized static CMOS inverter assuming the transistor parameters of Table 1. Size the circuit for an inverter switching threshold $V_M = 0.5V_{DD}$.



(2pts schematic)
(1 pt. sizes)

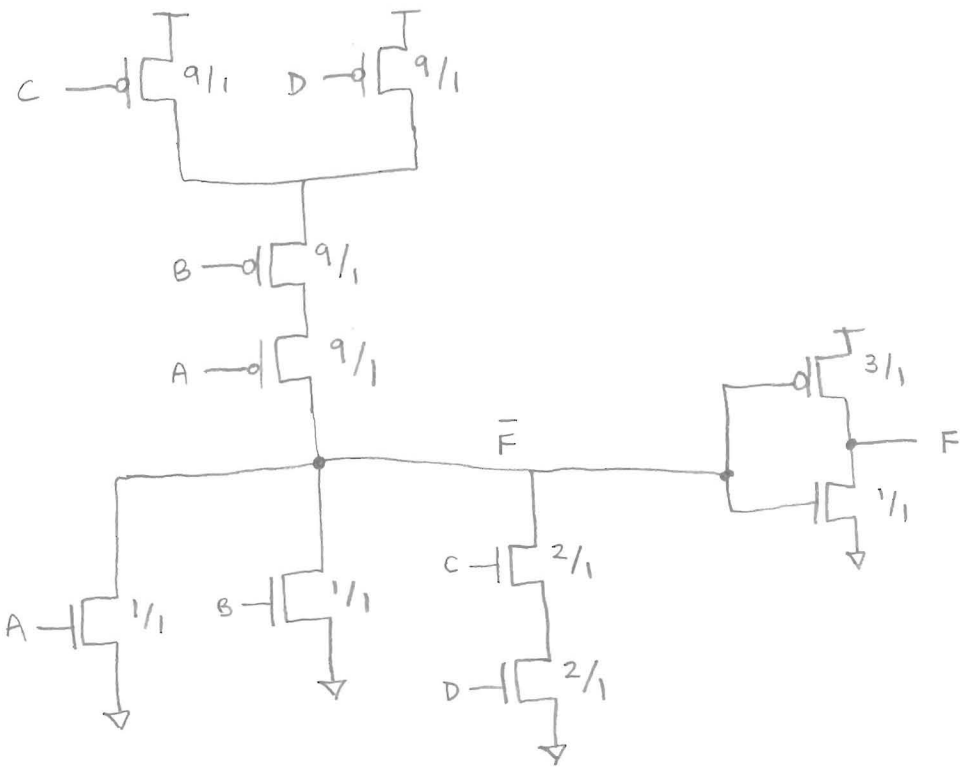
Problem 3.2 (2 points) Suppose the inverter you designed in Problem 3.1 drives a 45fF capacitance at 4.1GHz. How much power does it consume assuming $V_{DD} = 5$V?

$P = CV_{DD}^2 f$ (1 pt.)

$= (45\,fF)(5\,V)^2(4.1\,GHz)$

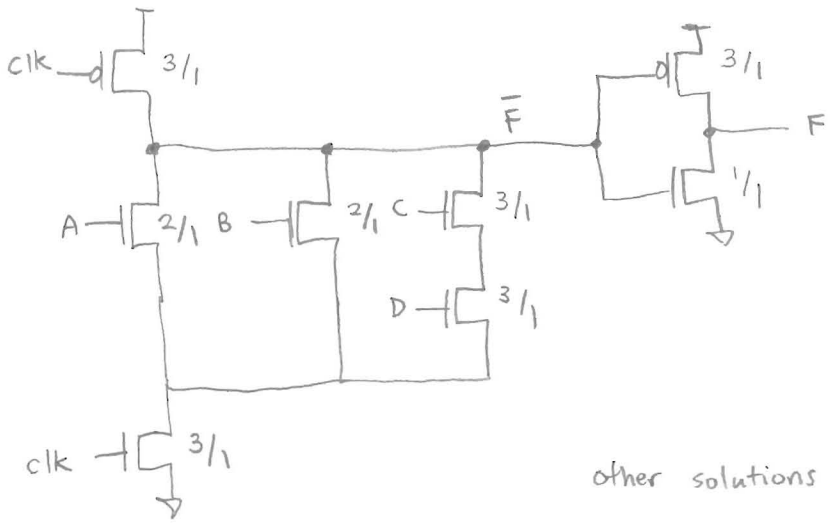
$= \boxed{4.61\,mW}$ (1 pt.)

Problem 3.3 (11 points) Implement the logic function $F = A + B + CD$ using a 4-input static CMOS logic gate and a single minimum-sized inverter as designed in Problem 3.1. Size the 4-input gate such that the worst case rise and fall times at its output are equal to the minimum-sized inverter.

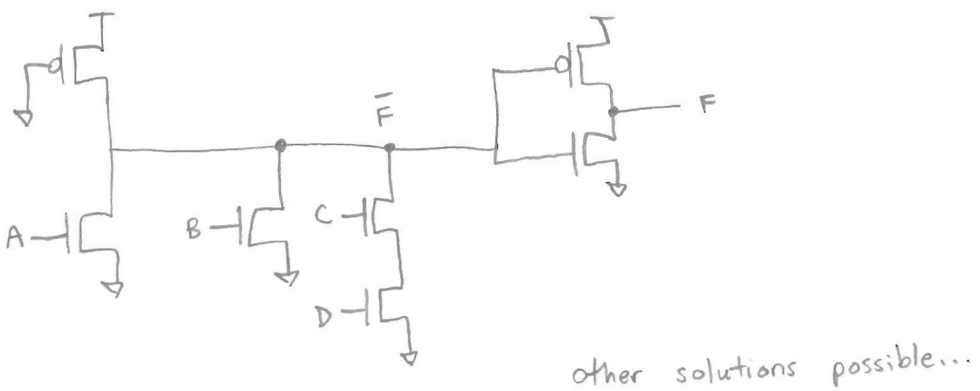


other solutions possible...

Problem 3.4 (**9 points**) Implement the logic function F using a 4-input dynamic logic gate and a single minimum-sized inverter as designed in Problem 3.1. Size the 4-input gate such that the worst case rise and fall times at the dynamic node are equal to the minimum-sized inverter.



Problem 3.5 (**5 points**) Implement the logic function F using a 4-input pseudo-NMOS logic gate and a single minimum-sized inverter as designed in Problem 3.1. You do not have to size the transistors.



4 Sequential Element Design

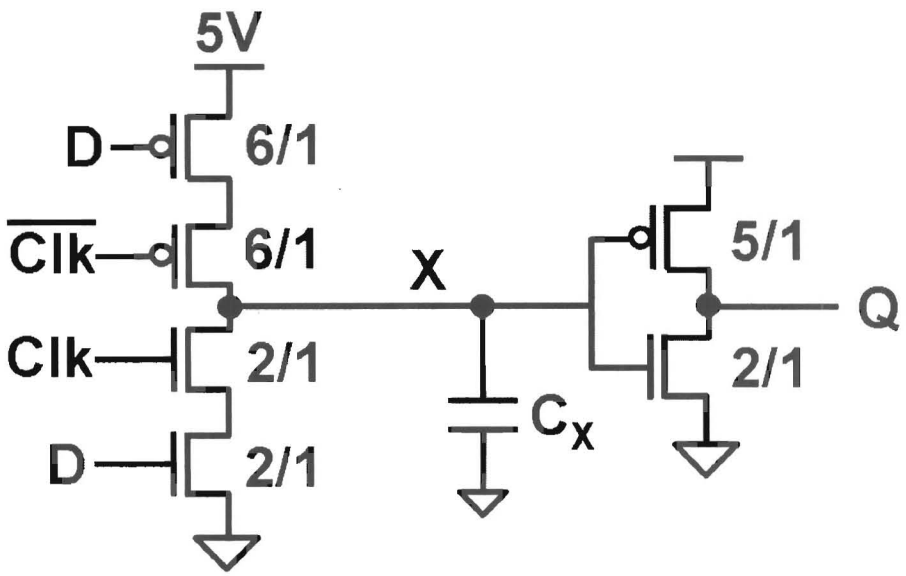


Figure 3: Transparent Latch.

Figure 3 shows a transparent latch circuit.

Problem 4.1 (2 points) Is this circuit a static or dynamic sequential element (circle one)? Justify your answer.

- Static
- (Dynamic)

C_x stores data as charge
No feedback

Problem 4.2 (2 points) Is this latch transparent during the positive or negative phase of the clock (circle one)? Justify your answer.

- (Positive)
- Negative

When clock is high, $Q = D$
When clock is low, $X = \overline{D}$ (last value), therefore Q = last value of

Problem 4.3 (10 points) The delay through the latch is determined by the rise and fall times at internal node X. Suppose $C_X = 9\text{fF}$. Using the switch RC model for the transistors, calculate the rise and fall times of node X assuming simultaneous ideal steps on D and Clk or $\overline{Clk}$ and that the initial resistance remains unchanged throughout the transition.

- $t_r =$ 35.7 ps
- $t_f =$ 35.7 ps

t_r: $V_X = 0V$, $D = Clk = 0V$, $V_{DS,P} = -5V \Rightarrow$ NMOS cutoff, PMOS sat (1 pt.)

$I_{DS,P} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_{eq}(V_{GS} - V_{T\phi,P})^2 = \frac{100\,\mu A/V^2}{2}\left(\frac{6}{2}\right)(-5V + 0.7V)^2$ (2 pt.)

$= 2.77\,mA$

$R_P = \frac{V_{DS,P}}{I_{DS,P}} = \frac{5V}{2.77mA} = 1.803\,k\Omega$ (1 pt.) $C_X = 9fF$

$t_r = 2.2 R_P C_X = 2.2\,(1.803\,k\Omega)(9fF) = 35.7\,ps$ (1 pt.)

t_f: $V_X = V_{DD} = 5V$, $D = Clk = 5V$, $V_{DS,n} = 5V \Rightarrow$ NMOS sat, PMOS cutoff (1 pt.)

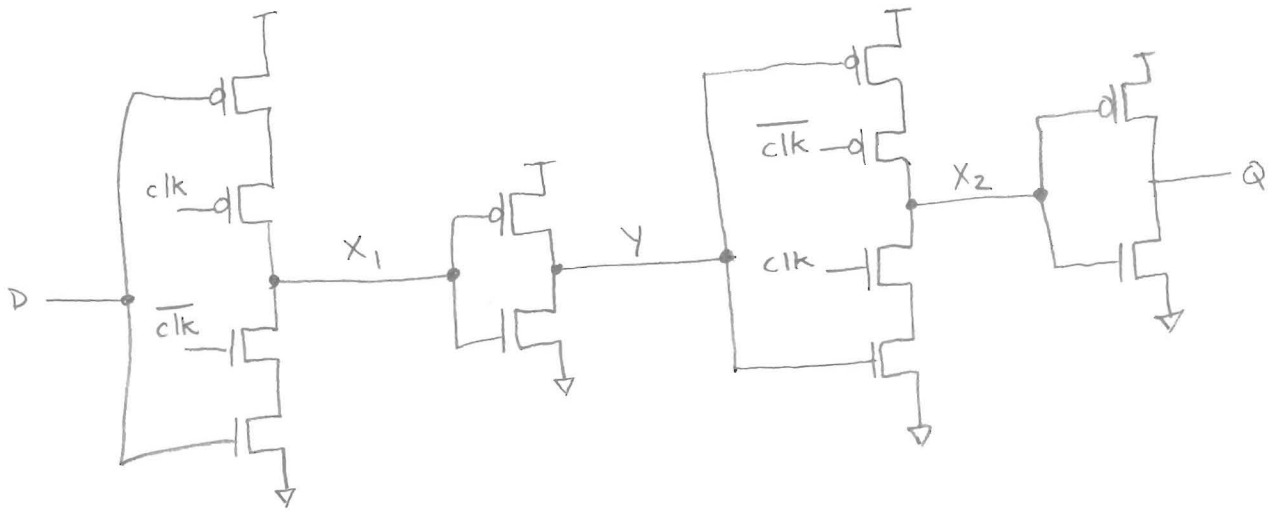
$I_{DS,n} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{eq}(V_{GS} - V_{T\phi,n})^2 = \frac{300\,\mu A/V^2}{2}\left(\frac{2}{2}\right)(5V - 0.7V)^2$ (2 pt.)

$= 2.77\,mA$

$R_N = \frac{V_{DS,N}}{I_{DS,N}} = 1.803\,k\Omega$ (1 pt.)

$t_f = 2.2 R_N C_X = 2.2\,(1.803k\Omega)(9fF) = 35.7\,ps$ (1 pt.)

Problem 4.4 (6 points) Design a **positive edge-triggered flip-flop** using two of the latch circuits shown in Figure 3. Be sure to label all data and clock inputs and outputs on your circuit schematic. You do not have to size the transistors.



(schematic 4 pts.)
(labels 2pts.)

5 One Transistor Memory

For this problem, assume the transistor characteristics as shown in Table 1 and all transistor widths and lengths are 1μm, unless otherwise specified. Figure 4 shows a one transistor memory cell connected to bit line BL with access to the storage node capacitance C_S controlled by word line WL. $\overline{PC}$ controls the precharge PMOS transistor while a tristate write driver is controlled by active high write enable WE.

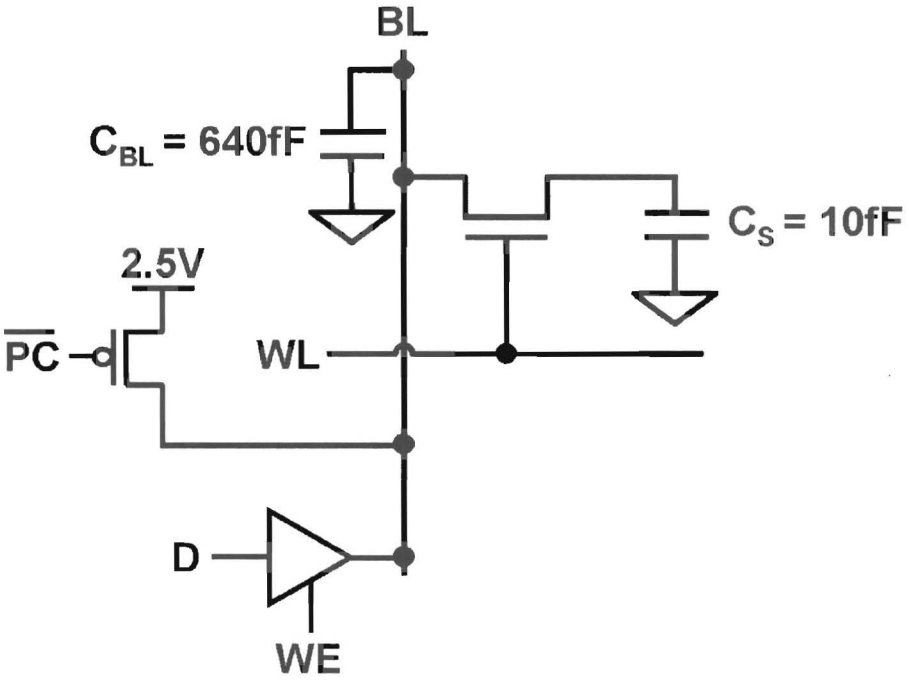


Figure 4: One transistor memory cell.

Problem 5.1 (2 points) What type of memory cell is shown in Figure 4 (circle one)? Justify your answer.

- SRAM
- (DRAM)

Bit stored as charge on C_S
No feedback or inverters

Problem 5.2 (**4 points**) Suppose during Write operations, the bit line voltage swings between 0V and $V_{DD} = 5$V while the word line voltage swings between 0V and 5.5V. What are the highest and lowest voltages (corresponding to storing a '1' and a '0', respectively) that can be stored on C_S?

- Logic '1' $V_S =$ 4.8V (1 pt.)
- Logic '0' $V_S =$ 0V (1 pt.)

$V_{DD} = V_{BL} = 5V$, $V_{WL} = 5.5V \Rightarrow V_S = V_{WL} - V_{TO,n} =$ **4.8V**, NMOS cuts off (2 pts.)

Problem 5.3 (**7 points**) During a Read operation, the write driver is disabled ($WE = 0$V) and the bit line BL is precharged by $\overline{PC}$ going low for a short time and initializing the voltage on bit line capacitance C_{BL}. The word line WL is driven to 5.5V. What is the final voltage on the bit line after WL goes high for the two storage node voltages you found in Problem 5.2? What is the voltage difference ΔV between reading a '1' and a '0'?

- Logic '1' Final $V_{BL} =$ **2.535V**
- Logic '0' Final $V_{BL} =$ **2.462V**
- $\Delta V =$ 2.535V − 2.462 = **73mV** or 74mV (1 pt.)

(1): $Q_{BL} = C_{BL}\frac{V_{DD}}{2}$ $Q_S = C_S V_{S(1)}$

$$V_{BL,final} = \frac{Q_{BL} + Q_S}{C_{BL} + C_S}$$

$$V_{BL,final} = \frac{(640\,fF)(2.5V) + (10fF)(4.8V)}{(640\,fF + 10fF)}$$

$= 2.535V$ (3 pts.)

(0): $Q_{BL} = C_{BL}\frac{V_{DD}}{2}$ $Q_S = C_S V_{S(0)}$

$$V_{BL,final} = \frac{(640\,fF)(2.5V) + (10fF)(0V)}{(640\,fF + 10fF)}$$

$= 2.462V$ (3 pts.)