EEC 118 Spring 2009 Final

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This examination is closed book and closed notes. You are allowed one 8.5 x 11 inch sheet (both sides) on which you may write formulas. Calculators are allowed, however using the calculator's function memory to store course related material is NOT allowed and constitutes cheating on this exam.

For all problems, state any assumptions you make, show all work, and clearly mark your answers. Correct but unclear or ambiguous answers will not receive full credit.

Excerpts from the UC Davis Code of Academic Conduct state:

1. Each student should act with personal honesty at all times.
2. Each student should act with fairness to others in the class. This means, for example, that when taking an examination, students should not seek an unfair advantage over other classmates through cheating or other dishonest behavior.
3. Students should take group as well as individual responsibility for honorable behavior. This includes notifying the instructor or TA if you observe cheating.

I understand the honor code and agree to be bound by it.

Signature:
Name (printed):
Lab Section:

Grading:

Problem	Maximum	Score	Problem	Maximum	Score
1	25		4	10	
2	25		5	10	
3	30				
Total	100				

Device Parameters

For **all** problems in this exam, assume we are using enhancement-type NMOS and PMOS transistors which have the characteristics shown in Table 1, unless otherwise specified. Also, assume **minimum** length devices unless otherwise specified.

Parameter	NMOS	PMOS
V_{T0}	1.0 V	-1.0 V
μC_{ox}	500 μA/V^2	200 μA/V^2
γ	0 V$^{1/2}$	0 V$^{1/2}$
W_{min}	1.0μm	1.0μm
L_{min}	1.0μm	1.0μm
λ	0.0 V^{-1}	0.0 V^{-1}
V_{DD}	5 V	

Table 1: Assumed Transistor Parameters.

1 Transistor I-V Measurements

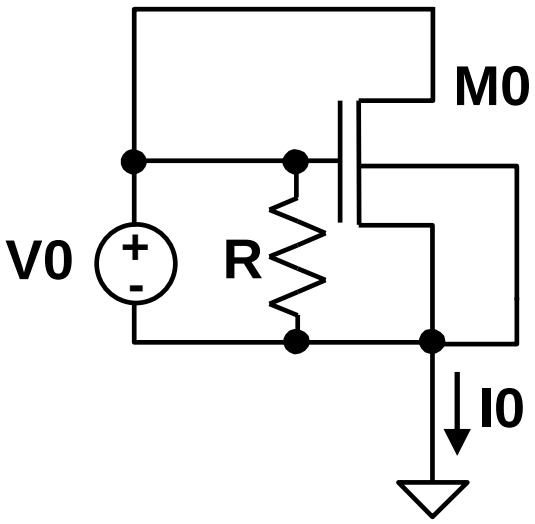

Figure 1: Measurement setup and model for an ESD-damaged NMOS transistor.

Problem 1.1 (**7 points**) Figure 1 shows a simple resistor-MOSFET (R-$M0$) model of an NMOS transistor which may have suffered damage due to electrostatic discharge (ESD). Assuming $R = \infty$, fill in Table 2 below.

V_0 (V)	I_0
0.5	
2.0	
3.0	
5	

Table 2: Problem 1.1 I-V Data.

Problem 1.2 (**5 points**) ESD damage will cause resistor R to have a finite value. Assuming $R = 10$ kΩ, fill in Table 3 below.

V_0 (V)	I_0
0.5	
2.0	
3.0	
5	

Table 3: Problem 1.2 I-V Data.

Problem 1.3 (**10 points**) Plot the I-V curves for **both** values of R on the axes below. Be sure to label both curves and the axes clearly.

Figure 2: I-V curves for both values of R.

Problem 1.4 (**3 points**) Based on this model, outline a simple experimental procedure to determine if an NMOS transistor has suffered ESD damage.

2 Inverter Characteristics

For this problem, use the device parameters in Table 1.

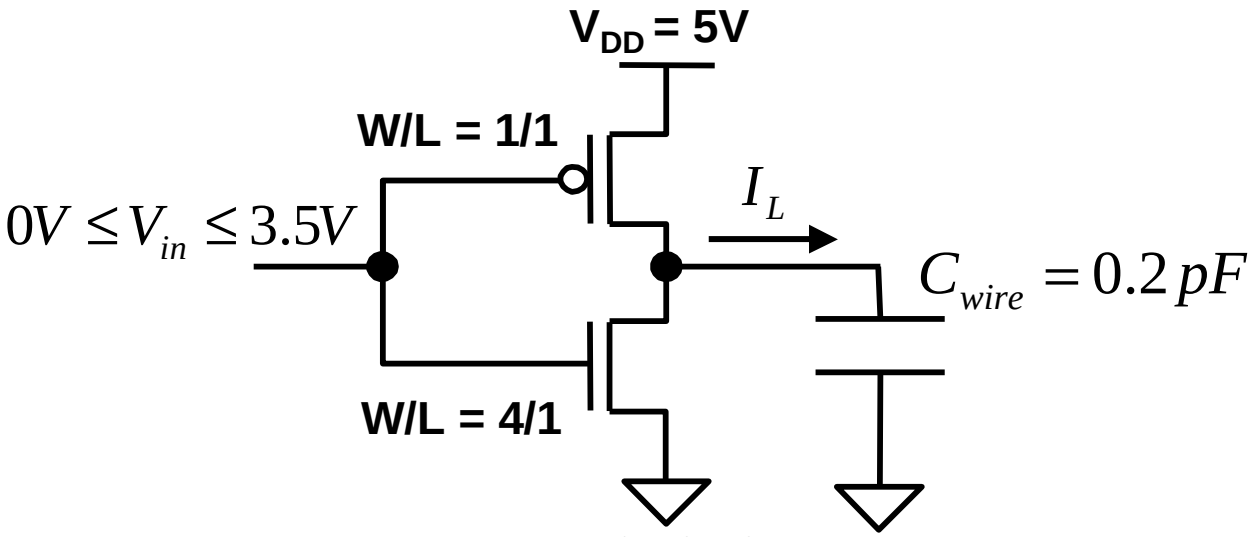

Figure 3: Inverter with reduced input swing.

Problem 2.1 (**8 points**) Figure 3 shows a loaded CMOS inverter but with reduced input voltage swing. Compute the following voltage levels given the limits on V_{in} (state any assumptions you make):

- $V_{OH} =$
- $V_{OL} =$

Problem 2.2 (**14 points**) Now assume that V_{in} can swing rail-to-rail (0V to $V_{DD} = 5$V. Find t_{pLH} assuming an ideal step input by averaging the appropriate currents at the beginning and end of the output transition and assuming the capacitances in Table 4 in addition to C_{wire} in the figure.

Capacitor (pF)	PMOS	NMOS
C_{gs}	0.05	0.2
C_{gd}	0.05	0.2
C_{db}	0.1	0.4
C_{sb}	0.1	0.4

Table 4: PMOS and NMOS capacitances.

Problem 2.3 (**3 points**) Assume that V_{in} can swing rail-to-rail (0V to $V_{DD} = 5$V. Find the dynamic power consumption at the output given a switching frequency of 100 MHz and the capacitances in Table 4 in addition to C_{wire} in the figure.

3 Static CMOS, Dynamic Logic, and Pseudo NMOS

Problem 3.1 (**3 points**) Draw and label the schematic for a minimum-sized static CMOS inverter assuming the transistor parameters of Table 1. Size the circuit for an inverter switching threshold $V_{TH} = 0.5V_{DD}$.

Problem 3.2 (**11 points**) Implement the logic function $F = A(BC + D)$ using a 4-input static CMOS logic gate and a single minimum-sized inverter as designed in Problem 3.1. Size the 4-input gate such that the worst case rise and fall times are equal to the minimum-sized inverter.

Problem 3.3 (**9 points**) Implement the logic function F using a 4-input dynamic logic gate and a single minimum-sized inverter as designed in Problem 3.1. Size the 4-input gate such that the worst case rise and fall times at the dynamic node are equal to the minimum-sized inverter.

Problem 3.4 (**6 points**) Implement the logic function F using a 4-input pseudo-NMOS logic gate and a single minimum-sized inverter as designed in Problem 3.1. You do not have to size the transistors.

Problem 3.5 (**1 point**) Which logic gate is likely to consume the most power (circle one)?

- Static CMOS
- Dynamic Logic
- Pseudo NMOS

4 Combined Logic and Sequential Element

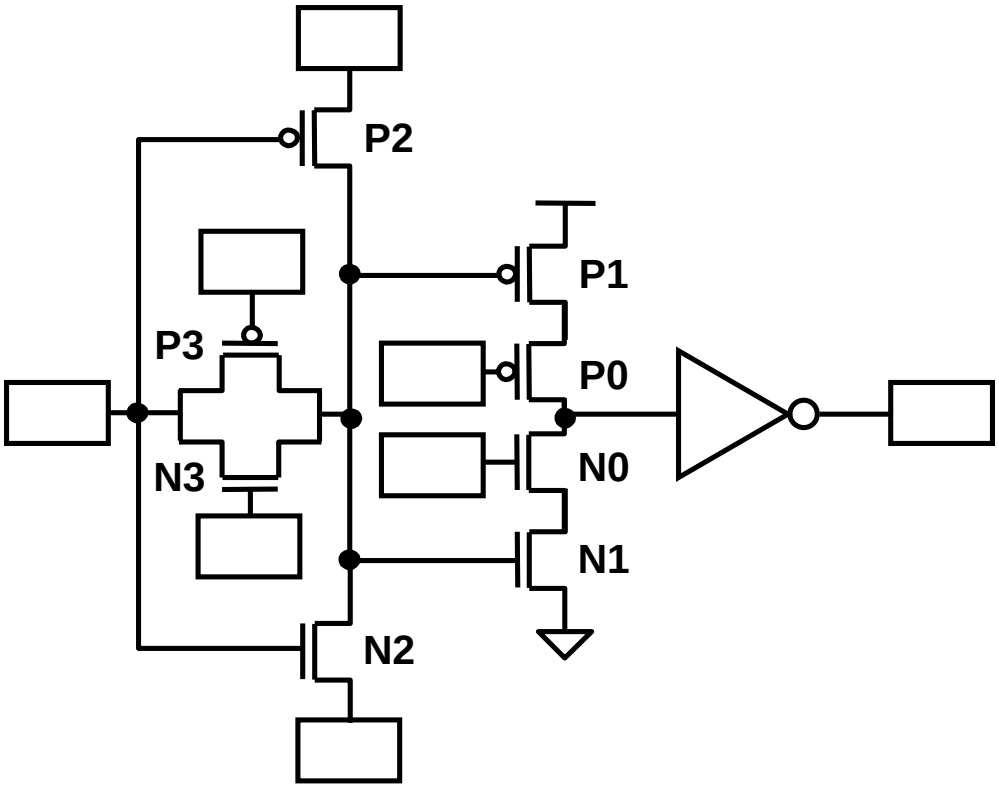

Figure 4: Combined Pass-Transistor Logic and Sequential Element.

Problem 4.1 (**4 points**) Fill in the appropriate labels in the boxes of Figure 4 for signals A, B, clk, $\overline{clk}$, and Q the such that the circuit operates as a positive transparent latch whose output $Q = A \oplus B$. (Assume you have both the true and complement versions of inputs A and B available.)

Problem 4.2 (**2 points**) Is this circuit a static or dynamic sequential element (circle one)? Justify your answer.

- Static
- Dynamic

Problem 4.3 (**2 points**) Which transistors directly affect the setup time t_{setup} for this circuit? Justify your answer.

Problem 4.4 (**2 points**) Which transistors directly affect the clock-to-Q delay t_{clk-Q} for this circuit? Justify your answer.

5 Four Transistor Memory

For this problem, assume the transistor characteristics as shown in Table 1 and all transistor widths and lengths are 1 μm, unless otherwise specified.

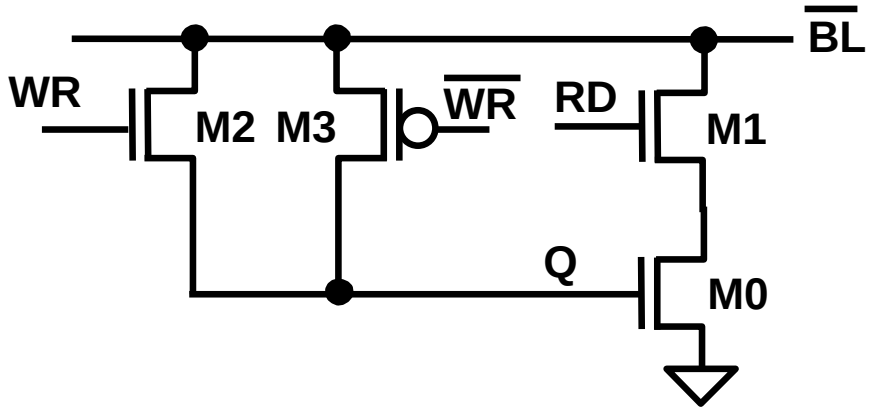

Figure 5: Four transistor memory cell.

Problem 5.1 (**2 points**) What type of memory cell is shown in Figure 5 (circle one)? Justify your answer. (Hint: **Q** is the storage node).

- Static
- Dynamic
- Flash

Problem 5.2 (**6 points**) Suppose node **Q** in Figure 5 has capacitance $C = 75$ fF and is initially at 0V. Using the switch RC model for the transistors, calculate the time to write node **Q** to $V_{DD}/2$ assuming ideal steps on WR and $\overline{WR}$ and that the initial resistance remains unchanged throughout the transition.

Problem 5.3 (**2 points**) Suppose transistor M3 is removed. How does this affect the robustness of the memory cell with respect to noise (circle one)? Justify your answer.

- Increases
- Decreases
- Stays about the same