EEC 118 Spring 2011 Midterm

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This examination is closed book and closed notes. Some formulas which you may find useful are listed in the back of the exam. Calculators are allowed, however using the calculator's function memory to store course related material is NOT allowed and constitutes cheating on this exam.

For all problems, state any assumptions you make, show all work, and clearly mark your answers. Correct but unclear or ambiguous answers will not receive full credit.

Excerpts from the UC Davis Code of Academic Conduct state:

1. Each student should act with personal honesty at all times.
2. Each student should act with fairness to others in the class. This means, for example, that when taking an examination, students should not seek an unfair advantage over other classmates through cheating or other dishonest behavior.
3. Students should take group as well as individual responsibility for honorable behavior. This includes notifying the instructor or TA if you observe cheating.

I understand the honor code and agree to be bound by it.
Signature: Solutions
Name (printed):
Lab Section:

Grading:

Problem	Maximum	Score
1	15	
2	9	
3	28	
4	11	
5	12	
Total	75	

1 Transistor Biasing

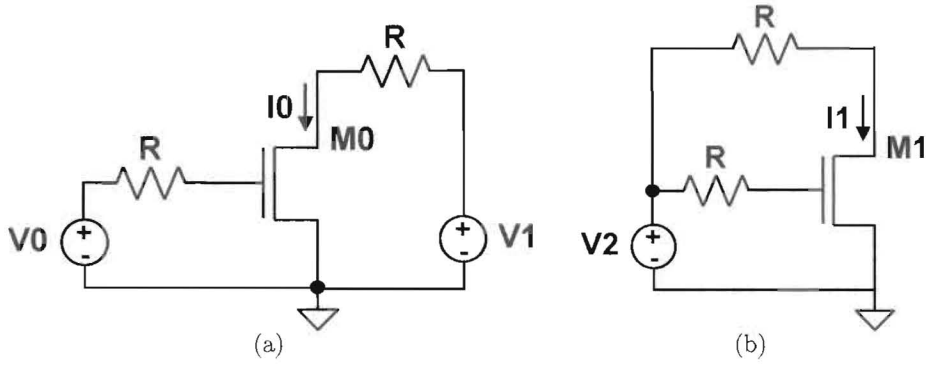


Figure 1: FET biasing circuits. (a) Two independent voltage sources. (b) One voltage source and two resistors.

Problem 1.1 (10 points) Consider the NMOS bias circuit shown in Figure 1(a). Suppose we know that for the NMOS under bias, $V_{T0,n} = 1.5\text{V}$, $W/L = 2/1$, $\gamma = 0.27\text{V}^{1/2}$, $\lambda = 0$ V^{-1}, $\mu C_{ox} = 299\ \mu\text{A/V}^2$, and $-2\Phi_F = 0.6$ V. Given that $V0 = 5\text{V}$ and $R = 50\Omega$, find the following:

- The smallest voltage $V1$ such that transistor M0 is in **saturation**: $V1 =$ 3.68 V
- The current $I0$ for the value of $V1$ you found: $I0 =$ 3.66 mA

$V_{DS} = V1 - I_\phi R$ $V_{GS} = V_\phi$
$V_{BS} = 0V$ (implicit)

For saturation, $V_{DS} \geq V_{GS} - V_{T,n} \Rightarrow V1 - I_\phi R \geq V_\phi - V_{T,n}$

$$I_{\phi,} = I_{DS} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_\phi - V_{T,n}\right)^2$$

$$= \frac{299\,\mu A/V^2}{2}\left(\frac{2}{1}\right)\left(5V - 1.5V\right)^2 = 3.66\text{ mA}$$

$$V1 \geq V_\phi - V_{T,n} + I_\phi R$$

$$\geq 5V - 1.5V + (3.66\text{ mA})(50\,\Omega)$$

$$\geq 3.68\text{ V}$$

Problem 1.2 (**5 points**) Consider the NMOS bias circuit shown in Figure 1(b). Assume transistor M1 has the same parameters as transistor M0 in Problem 1.1 except its W/L ratio is **unknown**. Given that when $V2 = 3.3\text{V}$ and $R = 500\Omega$, the NMOS $V_{DS} = V2/2$, find W/L for M1.

$V2 = 3.3V \qquad V_{DS} = \frac{V2}{2} = 1.65V \qquad V_{GS} = V2 \Rightarrow V_{GS} - V_{T,n} = V2 - V_{T,n} \qquad V_{BS} = 0V \text{ (implicit)}$

$= 3.3V - 1.5V$

$= 1.8V$

$V_{GS} - V_{T,n} > V_{DS} \Rightarrow \underline{\text{linear}}$

$$I_1 = \frac{V_2 - V_{DS}}{R} = \frac{V_2}{2R} = 3.3\text{mA} = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{T,n}) V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$\Rightarrow \left(\frac{W}{L}\right) = \frac{3.3\text{mA}}{299\frac{\mu A}{V^2}\left[(3.3V - 1.5V)(1.65V) - \frac{(1.65V)^2}{2}\right]}$$

$$\boxed{\frac{W}{L} = 6.86}$$

2 Logic Gate

Figure 2 shows a circuit model for a one input CMOS logic gate. Assume all transistor W/L ratios are as shown in Figure 2 and the following transistor and supply voltage characteristics:

$V_{DD} = 5$ V

$\lambda_n = 0.02$ V^{-1}	$\lambda_p = -0.02$ V^{-1}
$V_{T0,n} = 0.8$ V	$V_{T0,p} = -0.8$ V
$\gamma_n = 0.33$ V$^{1/2}$	$\gamma_p = 0.33$ V$^{1/2}$
$\mu_n C_{ox} = 350 \times 10^{-6}$ A/V^2	$\mu_p C_{ox} = 100 \times 10^{-6}$ A/V^2
$W_{min} = 2$	$L_{min} = 1$

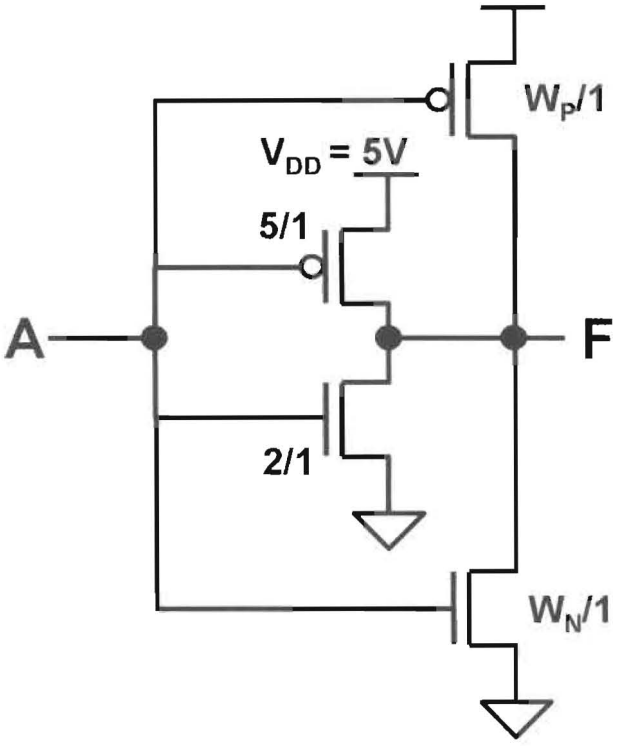


Figure 2: Circuit schematic for a logic gate.

Problem 2.1 (1 point) What Boolean logic function is implemented by the circuit in Figure 2?

$F = \overline{A}$ INV

Problem 2.2 (6 points) Find W_P and W_N such that the **worst case** rise and fall times of the circuit in Figure 2 are equal. Be sure to minimize the total transistor area. Justify your answers below.

- $W_P =$ 9
- $W_N =$ 2

Need $\frac{\text{total PMOS width}}{\text{total NMOS width}} = \frac{k_n'}{k_p'} = \frac{350\,\mu A/V^2}{100\,\mu A/V^2} = 3.5 = \frac{5+W_P}{2+W_N}$

$W_N \geq 2$, so choose $W_N = 2$ (min. area)

$\therefore\ W_P = 3.5(2+W_N) - 5 = 14 - 5 = 9$

Problem 2.3 (2 points) Given your sizes from Problem 2.2 above, what are V_{OH} and V_{OL} for the circuit in Figure 2? Justify your answers.

- $V_{OH} = V_{DD} = 5V$
- $V_{OL} = 0V$ (ground)

Parallel transistors can be combined, so ckt is a CMOS inverter which has full output swing.

3 Static CMOS Logic Design

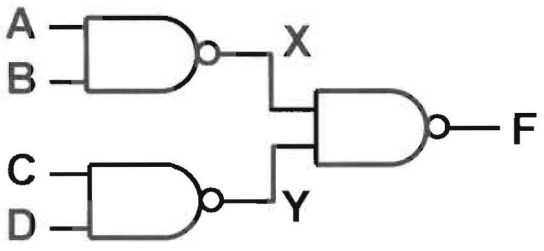
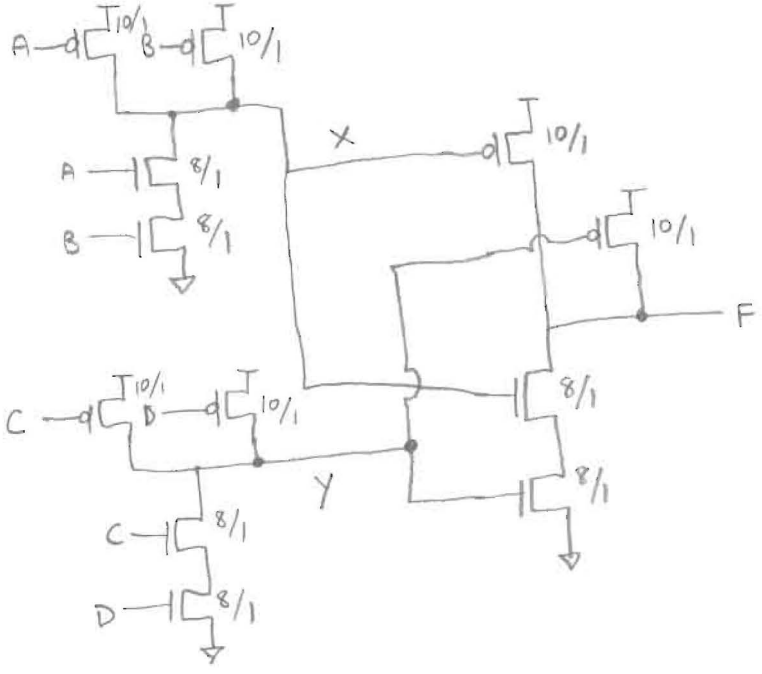


Figure 3: Logic gate network.

Problem 3.1 (**3 points**) Write a Boolean expression for the logic function F in terms of inputs A, B, C, and D implemented by the logic gate network in Figure 3.

$F = A \cdot B + C \cdot D$

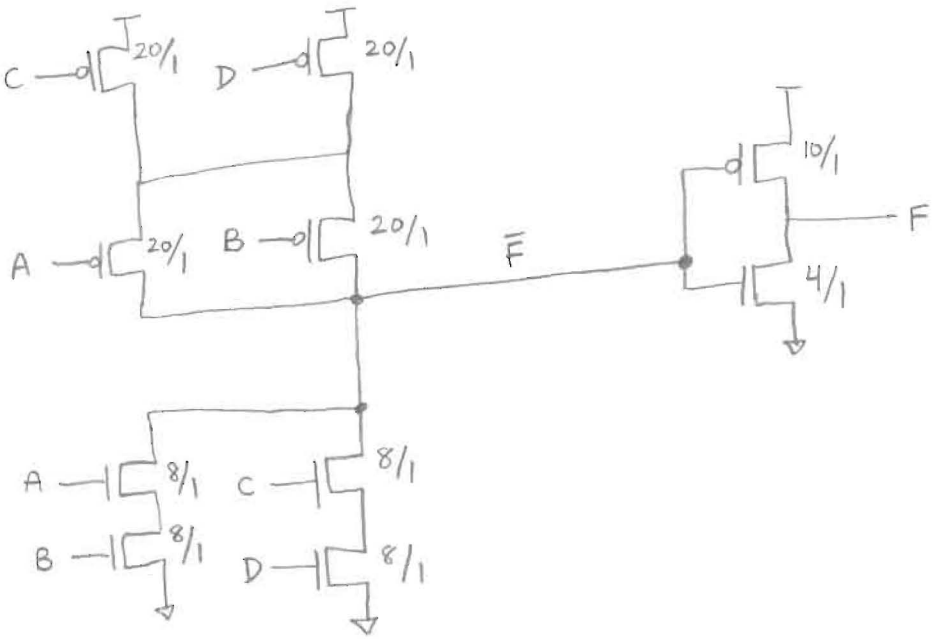
Problem 3.2 (**8 points**) Implement the circuit in Figure 3 using static CMOS circuits for the individual logic gates. You will need at least three static CMOS gate circuits (some may be the same). Be sure to label all inputs, outputs, and other circuit nodes.



other solutions possible ...

Problem 3.3 (**4 points**) Assume a minimum-sized inverter has PMOS ratio $W_P/L = 10/1$ and NMOS ratio $W_N/L = 4/1$. Choose appropriate W/L ratios for the transistors in your circuit of Problem 3.2 such that the worst case rise and fall times are the same as a minimum-sized inverter. Indicate the sizes in your schematic above. Be sure to minimize the total area of the transistors.

Problem 3.4 (**7 points**) Design a circuit that implements F which consists of a single multiple input CMOS logic gate and a static CMOS inverter.



other solutions possible

Problem 3.5 (**6 points**) Choose appropriate W/L ratios for the transistors in your circuit of Problem 3.4 such that the worst case rise and fall times are the same as the minimum-sized inverter in Problem 3.3. Indicate the sizes in your schematic above. Be sure to minimize the total area of the transistors.

4 Ring Oscillator

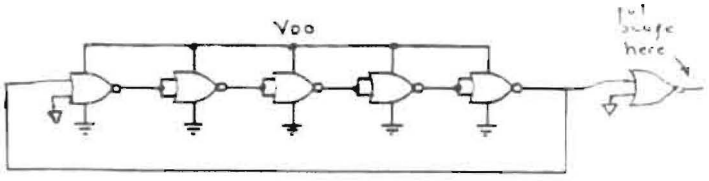


Figure 4: NOR gate ring oscillator.

Problem 4.1 (4 points) For the ring oscillator circuit shown in Figure 4 from Lab 2, use the switch RC model and the following parameters for the equivalent inverters which model the NOR gates: $R_p = 11k\Omega$, $R_n = 10k\Omega$, and $C_L = 99\text{fF}$ (C_L is the load capacitance seen by **each** NOR gate). What frequency would be measured by the scope probe when placed as shown in the figure?

$$f = \frac{1}{T} = \frac{1}{N(t_{pLH} + t_{pHL})} = \frac{1}{5(0.69 R_p C_L + 0.69 R_n C_L)}$$

$$= \frac{1}{5(0.69 \cdot 11k\Omega \cdot 99fF + 0.69 \cdot 10k\Omega \cdot 99fF)}$$

$$= \boxed{150.87\ \text{MHz}}$$ (139.4 MHz or other values acceptable → roundoff errors)

Problem 4.2 (7 points) Suppose the equivalent inverter resistance for the NMOS devices ($R_n = 10k\Omega$) in the NOR gates was measured by averaging the resistance at the beginning and end of a **best case fall time** measurement. Find the W/L of the NMOS devices given $V_{DD} = 5$ V, $V_{T0,n} = 1.0$ V, $\mu_n C_{ox} = 30 \times 10^{-6}$ A/V^2, $\gamma_n = 0.0$ V$^{1/2}$, $\lambda_n = 0.0$ V^{-1}.

$t_f = t_2 - t_1$ @ t_2: $V_{out} = 0.1 V_{DD}$; @ t_1: $V_{out} = 0.9 V_{DD}$ } $V_{out} = V_{DS}$ for NOR gate equivalent inverter.

$$R_n = \frac{1}{2}\left(\frac{V_{DS}@t_2}{I_{DS}@t_2} + \frac{V_{DS}@t_1}{I_{DS}@t_1}\right)$$

$V_{GS} = V_{DD}$, therefore

@ t_1: $V_{DS} = 0.9 V_{DD} = 4.5V \geq V_{DD} - V_{T\phi,n} = 5 - 1V = 4V$

sat

@ t_2: $V_{DS} = 0.1 V_{DD} = 0.5V < V_{DD} - V_{T\phi,n} = 4V$

linear

Problem 4.2 (cont.)

$$R_n = \frac{1}{2}\left[\frac{0.1V_{DD}}{\mu_n C_{ox}\left(2\cdot\frac{W}{L}\right)\left[(V_{DD}-V_{T\phi,n})0.1V_{DD} - \frac{(0.1V_{DD})^2}{2}\right]} + \frac{0.9V_{DD}}{\frac{\mu_n C_{ox}}{2}\left(2\cdot\frac{W}{L}\right)(V_{DD}-V_{T\phi,n})^2} \right]$$

↑ NMOS parallel for best case fall time

Plugging in values and solving for $\frac{W}{L}$,

$$\boxed{\frac{W}{L} = 1.16}$$ or 1.31 if 20%-80% fall time assumed

5 Latch

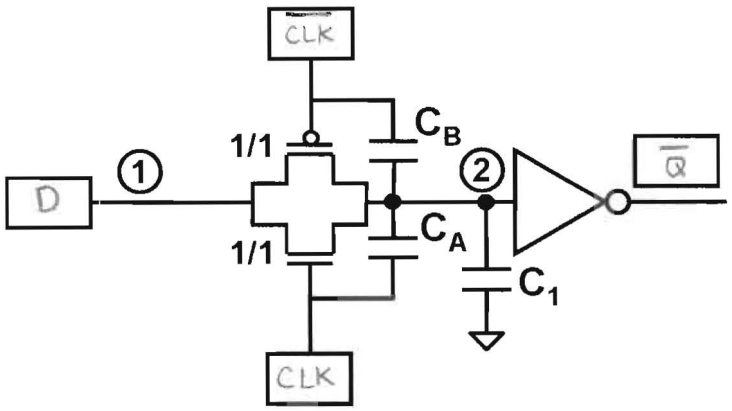


Figure 5: Latch schematic.

Problem 5.1 (**4 points**) For the latch circuit shown in Figure 5, label the boxes D, CLK, $\overline{CLK}$, $\overline{Q}$ such that the circuit works as a **positive transparent** inverting latch.

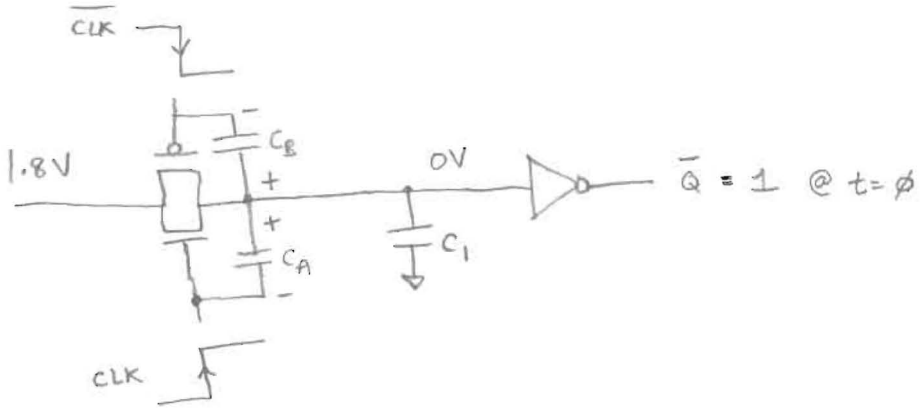
Problem 5.2 (**2 points**) Is the circuit in Figure 5 a static or dynamic latch (circle one)? Justify your answer.

- Static
- Dynamic — No positive feedback, logic level stored as capacitor charge.

Problem 5.3 (**6 points**) Suppose the latch is used as the slave stage of an edge-triggered flip-flop and that node 1 and node 2 in Figure 5 are initially at 1.8V and 0V, respectively. Assuming $R_p = 300\Omega$ for a PMOS device with $W/L = 1/1$ and $R_n = 100\Omega$ for an NMOS device with $W/L = 1/1$, $C_A = 19$fF, $C_B = 23$fF, $C_1 = 150$fF, and t_{pHL} for the inverter is 8.9ps, estimate the clock-to-Q delay for the latch using the switch RC model for the transistors.

Problem 5.3 (cont.)

$t_{C\to Q}$: when CLK goes high, D propagates to output $\overline{Q}$



$R_{eq} = R_n \| R_p = 100\,\Omega \| 300\,\Omega = 75\,\Omega$

$t_{C\to Q} = 0.69\, R_{eq}\, C_{TOT} + t_{pHL}$

ΔV for $C_B = 1.8V - (-1.8V) = 3.6V$ ← Miller effect

ΔV for $C_1 = 1.8V - 0V = 1.8V$

ΔV for $C_A = 0V - 0V = 0V$ ← ignore C_A's contribution to delay

$C_{TOT} = C_1 + 2C_B = 150\,fF + 2 \cdot 23\,fF = 196\,fF$

$t_{C\to Q} = 0.69 \cdot 75\,\Omega \cdot 196\,fF + 8.9\,ps$

$\boxed{t_{C\to Q} = 19.043\,ps}$

$C_{TOT} = C_1 + C_A + C_B = 192\,fF \Rightarrow t_{C\to Q} = 18.836\,ps$

$C_{TOT} = C_1 + 2 \cdot (C_A + C_B) = 234\,fF \Rightarrow t_{C\to Q} = 21.01\,ps$

Miscellaneous Formulas

MOSFET Threshold Voltage

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

$$\gamma = \frac{\sqrt{2q \cdot N_A \cdot \epsilon_{Si}}}{C_{ox}}$$

CMOS Inverter Switching Threshold

$$V_{TH} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot (V_{DD} - |V_{T0,p}|)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

CMOS Inverter Propagation Delay Times

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})} \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)} \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

Switch Model Propagation Delay Times

$$t_{PHL} = 0.69 R_n C_L$$

$$t_{PLH} = 0.69 R_p C_L$$

$$t_f = 2.2 R_n C_L$$

$$t_r = 2.2 R_p C_L$$

Junction Capacitances

$$C_{j0} = \sqrt{\frac{\epsilon_{Si} \cdot q}{2} \left(\frac{N_A N_D}{N_A + N_D} \right) \frac{1}{\phi_0}}$$

$$C_j(V) = \frac{AC_{j0}}{\left(1 - \frac{V}{\phi_0}\right)^m}$$

$$C_{eq} = AC_{j0}K_{eq}$$