EEC 118 Spring 2011 Final

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This examination is closed book and closed notes. You are allowed one 8.5 x 11 inch sheet (both sides) on which you may write formulas. Calculators are allowed, however using the calculator's function memory to store course related material is NOT allowed and constitutes cheating on this exam.

For all problems, state any assumptions you make, show all work, and clearly mark your answers. Correct but unclear or ambiguous answers will not receive full credit.

Excerpts from the UC Davis Code of Academic Conduct state:

1. Each student should act with personal honesty at all times.
2. Each student should act with fairness to others in the class. This means, for example, that when taking an examination, students should not seek an unfair advantage over other classmates through cheating or other dishonest behavior.
3. Students should take group as well as individual responsibility for honorable behavior. This includes notifying the instructor or TA if you observe cheating.

I understand the honor code and agree to be bound by it.

Signature:
Name (printed):
Lab Section:

Grading:

Problem	Maximum	Score	Problem	Maximum	Score
1	20		4	15	
2	25		5	15	
3	25				
Total	100				

Device Parameters

For **all** problems in this exam, assume we are using enhancement-type NMOS and PMOS transistors which have the characteristics shown in Table 1, unless otherwise specified. All dimensions are in microns. Also, assume **minimum** length devices unless otherwise specified.

Parameter	NMOS	PMOS
V_{T0}	0.8 V	-0.8 V
μC_{ox}	300 μA/V^2	100 μA/V^2
γ	0 V$^{1/2}$	0 V$^{1/2}$
W_{min}	1.0μm	1.0μm
L_{min}	1.0μm	1.0μm
λ	0.0 V^{-1}	0.0 V^{-1}
V_{DD}	5 V	

Table 1: Assumed Transistor Parameters.

Capacitance/Width (fF/μm)	PMOS	NMOS
C_{gs}	1.5	1.4
C_{gd}	1.5	1.4
C_{db}	1.0	0.9
C_{sb}	1.0	0.9

Table 2: PMOS and NMOS capacitances per unit width.

1 Transistor Current Biasing

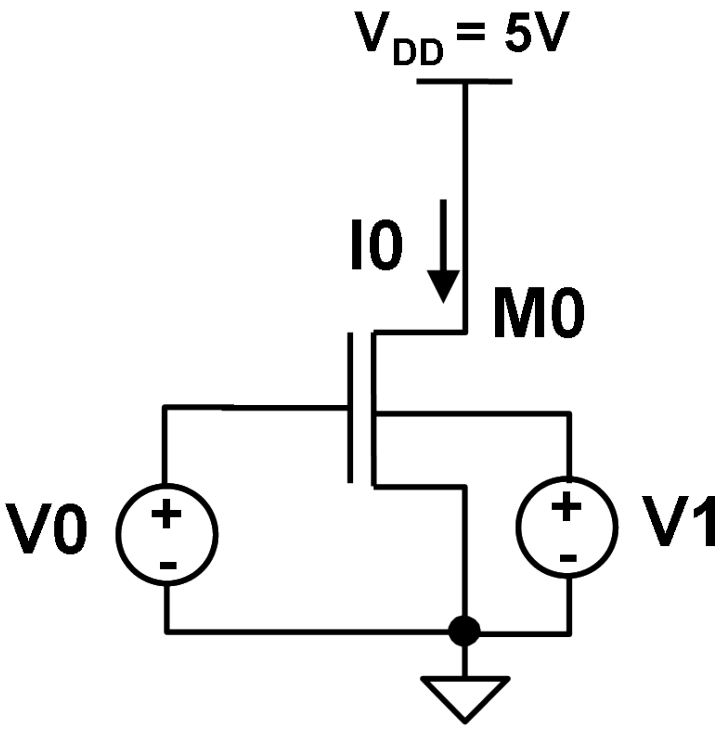

Figure 1: Voltage setup for NMOS biasing.

Assume that NMOS transistor $M0$ in Figure 1 has $W/L = 4$, $\gamma = 0.33\text{V}^{\frac{1}{2}}$, and $-2\Phi_F = 0.6\text{V}$ in the following problems.

Problem 1.1 (**5 points**) Find the value of $V1$ which yields $V_{Tn} = 1.1\text{V}$.

Problem 1.2 (**7 points**) Given the value of $V1$ you found in Problem 1.1, fill in the table below for the different values of $V0$.

- $V0 = 0\text{V}$, $I0 =$
- $V0 = 1.0\text{V}$, $I0 =$
- $V0 = 4.0\text{V}$, $I0 =$
- $V0 = 7.0\text{V}$, $I0 =$

Problem 1.3 (**5 points**) Assuming the value of $V1$ which you found in Problem 1.1, find the value of $V0$ which yields a current $I0 = 1\text{mA}$.

Problem 1.4 (**3 points**) Suppose $\lambda = 0.06\text{V}^{-1}$ and that when $V_{GS} < V_{Tn}$, the NMOS drain current is:

$$I_{DS} = I_S e^{\frac{V_{GS}-V_{Tn}}{kT/q}} \left(1 - e^{\frac{-V_{DS}}{kT/q}}\right)(1 + \lambda V_{DS}) \tag{1}$$

where $I_S = 4.85\mu\text{A}$ and $kT/q = 26\text{mV}$. Assuming $V0 = 1.0\text{V}$ and $V1$ which you found in Problem 1.1, what is the new value of $I0$ at this $V0$?

2 Inverter Characteristics and Logical Effort

Problem 2.1 (**3 points**) Draw and label the schematic for a minimum-sized static CMOS inverter assuming the transistor parameters of Table 1. Size the circuit for an inverter switching threshold $V_M = 0.5V_{DD}$.

Problem 2.2 (**2 points**) Suppose the inverter you designed in Problem 2.1 drives a total capacitance of 45fF at 4.1GHz. How much power does it consume assuming $V_{DD} = 5$V?

Problem 2.3 (**4 points**) Suppose the inverter you designed in Problem 2.1 drives an identical copy of itself. Using the capacitance values from Table 2, find the total load capacitance seen by the driver $C_T = C_p + C_{in}$, where C_p is the unloaded (intrinsic) output capacitance of the driver and C_{in} is the input capacitance of the receiver.

- $C_p =$
- $C_{in} =$
- $C_T =$

Problem 2.4 (**6 points**) Find t_{pLH} for the inverter you designed in Problem 2.1 driving a total capacitance of C_T (from Problem 2.3). Assume an ideal step voltage on V_{in} and approximate the charging current by averaging the initial and final drain currents.

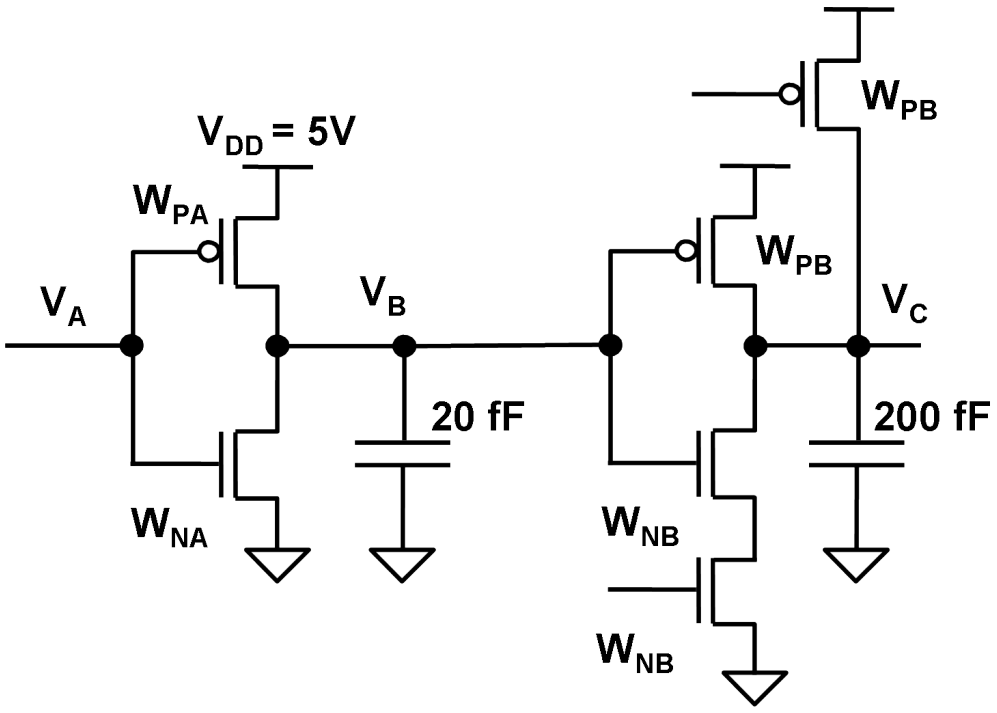

Figure 2: Cascaded inverter and NAND gate forming part of a logic network.

Problem 2.5 (**1 point**) Figure 2 shows a CMOS inverter driving a 20fF wire load and a 2-input NAND gate driving a 200fF wire load. You will use the method of **logical effort** to minimize the delay of these gates by finding the optimal transistor widths. First, find the normalized parasitic delay $p = C_p/C_{in}$ from the values you found above.

- $p =$

Problem 2.6 (**5 points**) Find the optimal transistor widths for the FETs in Figure 2 assuming each logic stage has an identical effort delay $f = gh$ of 4.

- $W_{PA} =$
- $W_{NA} =$
- $W_{PB} =$
- $W_{NB} =$

Problem 2.6 (cont.)

Problem 2.7 (**4 points**) Find the normalized path delay D and the absolute path delay D_{abs} assuming the sizes you found in Problem 2.6 and $\tau = t_{pLH}$ you found in Problem 2.4.

- $D =$
- $D_{abs} =$

3 Static CMOS, Dynamic Logic, and Pseudo NMOS

Problem 3.1 (**11 points**) Implement the logic function $F = ABD + CD$ using a 4-input static CMOS logic gate with a minimum number of transistors and a single minimum-sized inverter as designed in Problem 2.1. Size the 4-input gate such that the worst case rise and fall times at its output are equal to the minimum-sized inverter.

Problem 3.2 (**9 points**) Implement the logic function F using a 4-input dynamic logic gate and a single minimum-sized inverter as designed in Problem 2.1. Size the 4-input gate such that the worst case rise and fall times at the dynamic node are equal to the minimum-sized inverter.

Problem 3.3 (**5 points**) Implement the logic function F using a 4-input pseudo-NMOS logic gate and a single minimum-sized inverter as designed in Problem 3.1. You do not have to size the transistors.

4 Sequential Element Design

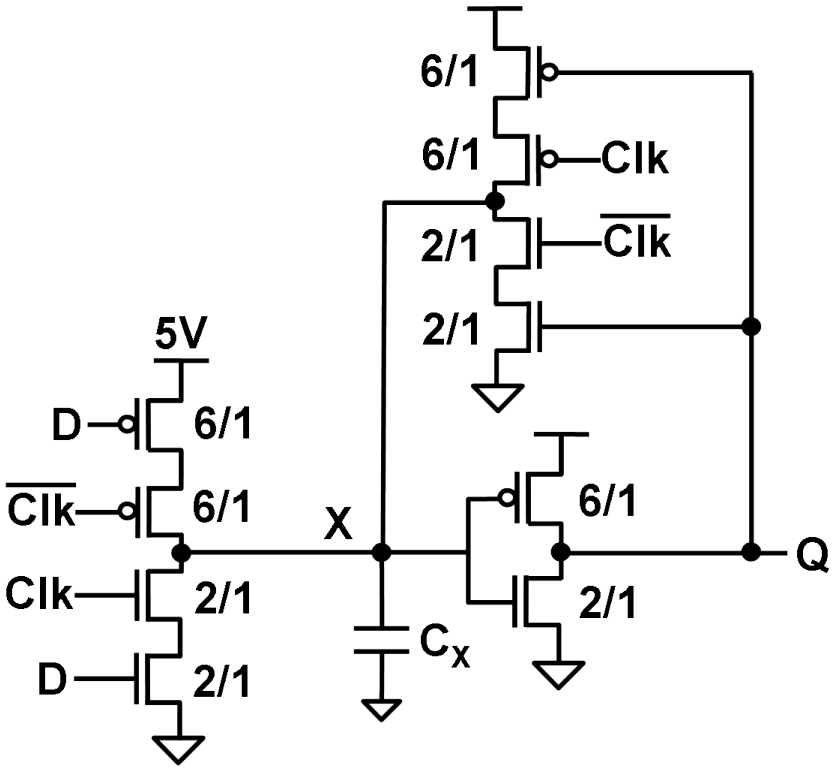

Figure 3: Transparent Latch.

Figure 3 shows a transparent latch circuit.

Problem 4.1 (**2 points**) Is this circuit a static or dynamic sequential element (circle one)? Justify your answer.

- Static
- Dynamic

Problem 4.2 (**2 points**) Is this latch transparent during the positive or negative phase of the clock (circle one)? Justify your answer.

- Positive
- Negative

Problem 4.3 (**10 points**) The delay through the latch is determined by the rise and fall times at internal node X. Suppose $C_X = 25\text{fF}$. Using the switch RC model for the transistors, calculate the rise and fall times of node X assuming simultaneous ideal steps on D and Clk or $\overline{Clk}$ and that the initial resistance remains unchanged throughout the transition.

- $t_r =$
- $t_f =$

Problem 4.4 (**1 point**) Briefly describe a set of conditions on Clk and $\overline{Clk}$ which could cause the latch to operate incorrectly.

5 Eight Transistor Memory Cell

For this problem, assume the transistor characteristics as shown in Table 1 and all transistor widths and lengths are 1μm, unless otherwise specified. Figure 4 shows an eight transistor memory cell. The inverters are CMOS inverters.

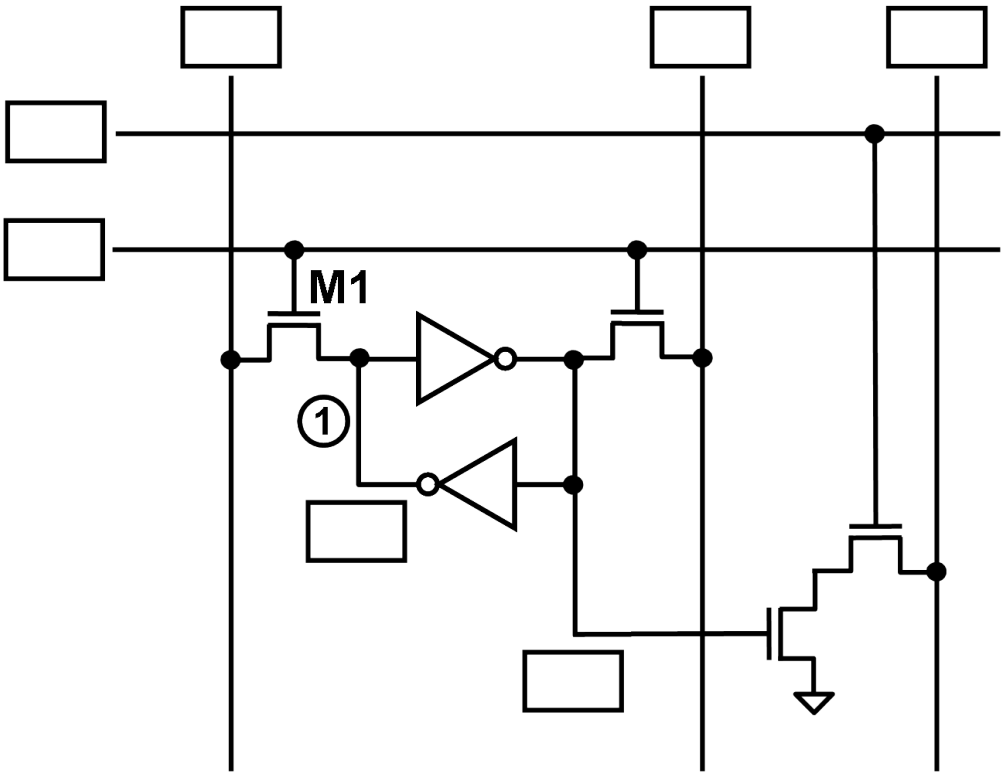

Figure 4: Eight transistor memory cell.

Problem 5.1 (**2 points**) What type of memory cell is shown in Figure 4 (circle one)? Justify your answer.

- SRAM
- DRAM
- ROM

Problem 5.2 (**4 points**) Label Figure 4 to clearly indicate the storage (data) node Q, the write word line WWL, the read word line RWL, the write bit line WBL, and the read bit line RBL. Also label the complements of any signals if necessary.

Problem 5.3 (**4 points**) Assume Node 1 is a storage node and NMOS M1 connects to a bidirectional bit line. If Node 1 stores a logic '0' and the bit line is held at V_{DD}, write an equation which can be solved for the voltage V_1 at Node 1. State any reasonable assumptions you make. Simplify the equation but you do not need to solve for V_1.

Problem 5.4 (**4 points**) Under the same assumptions as in Problem 5.3, if Node 1 stores a logic '1' and the bit line is held at 0V, write an equation which can be solved for the voltage V_1 at Node 1. State any reasonable assumptions you make. Simplify the equation but you do not need to solve for V_1.

Problem 5.5 (**1 point**) What is the principal advantage of the memory cell shown in Figure 4 over a conventional six transistor SRAM cell?