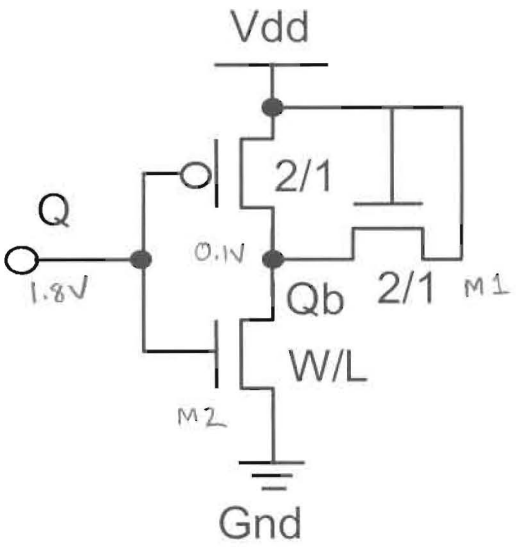
Quiz #4 **EEC116** **Fall 2011**

Name: Solutions Lab Section: _____

Problem 1 (7 points) Consider the following half-circuit for analyzing the read Static Noise Margin for a memory cell. Find W/L such that node Qb is at 100mV given V_{DD}=1.8V, node Q is 1.8V, $V_{T,n}$=0.5V, $\mu_n C_{ox}$=3 x 10^{-4}A/V^2, $V_{T,p}$=-0.5V, $\mu_p C_{ox}$ = 1 x 10^{-4}A/V^2, $\lambda = 0$, $\gamma = 0$. Show all work to receive full credit.



M1 Sat PMOS off (2pts.)

M2 lin

KCL @ Qb: (3pts.)

$$\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{DD}-V_{Qb}-V_{T,n})^2 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 \left[2(V_{DD}-V_{T,n})V_{Qb}-V_{Qb}^2\right]$$

$$\Rightarrow \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_1 \frac{(V_{DD}-V_{Qb}-V_{T,n})^2}{2(V_{DD}-V_{T,n})V_{Qb}-V_{Qb}^2} \quad (1\text{pt.})$$

$$= \left(\frac{2}{1}\right) \frac{(1.7V-0.5V)^2}{2(1.8V-0.5V)(0.1V)-(0.1V)^2}$$

$$= \boxed{11.52} \quad (1\text{pt.})$$

Problem 2 (3 points) For the following 1 transistor DRAM cell, fill in the boxes labeling the corresponding wires with the appropriate signal names: (1pts ea.)

Q: data storage bit

BL: bit line

WL: word line