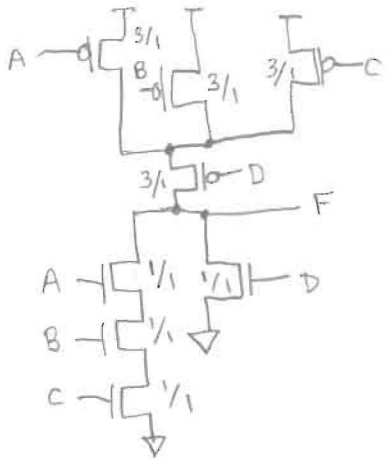
Quiz #2 **EEC116** **Fall 2011**

Name: Solutions Lab Section:_____

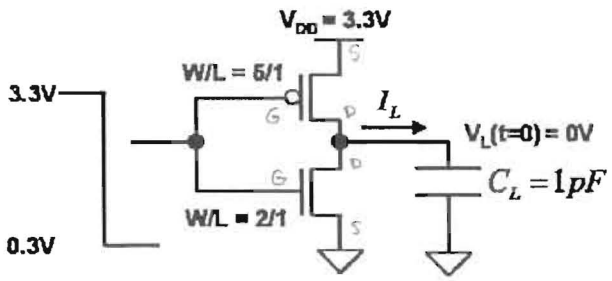
For all transistors: $L_{min} = 1\ \mu m$, $W_{min} = 1\ \mu m$, $V_{T,p} = -1\ V$, $\mu_p C_{ox} = (1/6) \times 10^{-3}\ A/V^2$, $\lambda_p = 0.0V^{-1}$, $V_{T,n} = 1\ V$, $\mu_n C_{ox} = (1/2) \times 10^{-3}\ A/V^2$, $\lambda_n = 0.0V^{-1}$.

Problem 1 (5 points) Design a four-input static CMOS logic gate which implements the Boolean expression $F = \overline{A \bullet B \bullet C + D}$. Clearly label all inputs, outputs, and power supply connections. Pick sizes for the transistors such that the worst case rise and fall times of the output are equal to a minimum-sized inverter.



0.5 pt. ea. FET
1 pt. labels

Problem 2 (5 points) A step input is applied at time t=0 to the loaded inverter with dimensions and initial conditions as shown below. What is the current I_L immediately after the step is applied?



PMOS: $V_{GS} = -3V$ $V_{DS} = -3.3V$

$V_{GS} - V_{T,p} = -2V > V_{DS}$ saturation (1 pt.)

NMOS: $V_{GS} = 0.3V < V_{T,n} = 1V$ cutoff (1 pt.)

$$I_L = I_{DS,p} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{GS,p} - V_{T,p}\right)^2 \quad (2\ pts.)$$

$$= \frac{(1/6 \times 10^{-3}\ A/V^2)}{2}\left(\frac{5}{1}\right)(-3.0V - -1V)^2 \quad (0.5\ pt.)$$

$$= \boxed{1.67mA} \quad (0.5\ pt.)$$