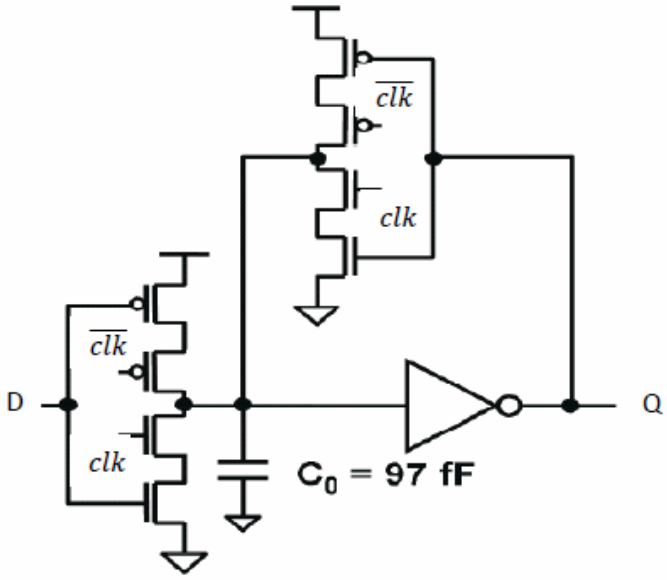
EEC116 Problem Set #4 Solution

1. Transparent Latch

Problem 1.1



We want the latch to be transparent when clk is positive, so we put clk at the gates of the NMOS's and clk_bar at the gates of the PMOS's. The feedback inverter makes it static instead of dynamic.

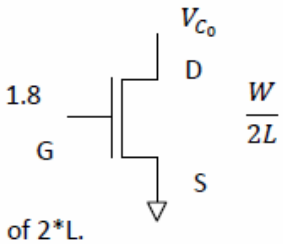
Problem 1.2

Since the output equals the input after some delay, we imagine the input D at V_{DD} and the output Q low before the clk signal goes high. We're given the t_{pLH} for the second inverter which is the delay for the output to go from GND to 0.5 V_{DD}. Assuming that t_{pLH2} is the time from when the input changes to it's 50% value till the output rises to the 50% value, the t_{pLH} from the input to the output is approximately $t_{HL1} + t_{pLH2}$ because we need the time it takes the voltage at the capacitor V_{C_0} or the input to the second inverter to become 0.5 V_{DD}. We don't have to calculate the full fall time for the first inverter.

Using the average current method, $\tau_{pHL1} = \frac{C_{load}\Delta V}{I_{avg}}$ where ΔV is 0.5V_{DD}.

$$I_{avg} = \frac{1}{2}\left[I(V_{in} = 1.8, V_{C_0} = 1.8) + I(V_{in} = 1.8, V_{C_0} = 0.9)\right]$$

Saturation since $V_{DS} \geq V_{GS} - V_{T,n}$ Linear since $V_{DS} < V_{GS} - V_{T,n}$



We can treat the two NMOS in series as one NMOS with an effective length of 2*L.

$$I_{avg} = \frac{k_n}{4}\left[(V_{GS} - V_{T,n})^2 + 2(V_{GS} - V_{T,n})V_{DS} - V_{DS}{}^2\right] = \frac{300\mu A}{4}\frac{0.45}{2 * 0.180}[1.2^2 + 2(1.2)(0.9) - 0.9^2]$$
$$= 262\ \mu A$$

$\tau_{HL} = \frac{97\,fF*0.9\,V}{262\,\mu A} = \underline{333\text{ ps}}$ $\boxed{t_{pLH} = 333\,ps + 45\,ps = 378\,ps}$

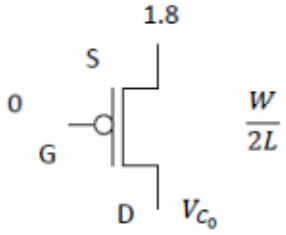
You can also use the 2nd approximation using the saturation current, which gives $\tau_{HL} = 323$ ps and $\boxed{t_{pLH} = 323\,ps + 45\,ps = 368\,ps}$.

Problem 1.3

The same can be done as in the previous problem, but for the output falling from high to low and the input low before clock goes high. Therefore, we will be focus on the PMOS in the first inverter, and the second inverter has t_{pHL} = 45 ps.

$$I_{avg} = \frac{1}{2}\left[I(V_{in} = 0, V_{C_0} = 0) + I(V_{in} = 0, V_{C_0} = 0.9)\right]$$

Saturation since $|V_{DS}| \geq |V_{GS}| - |V_{T,p}|$ Linear since $|V_{DS}| < |V_{GS}| - |V_{T,p}|$



$$I_{avg} = \frac{k_p}{4}\left[(V_{GS} - V_{T,p})^2 + 2(V_{GS} - V_{T,p})V_{DS} - V_{DS}{}^2\right]$$

$$= \frac{100\mu A}{4}\frac{1.44}{2*0.180}[(-1.1)^2 + 2(-1.1)(-0.9) - (-0.9)^2] = 238\,\mu A$$

$\tau_{pLH1} = \frac{97\,fF*0.9\,V}{238\,\mu A} = 367$ ps $\boxed{t_{pHL} = 367\,ps + 45\,ps = 412\text{ ps}}$

Using the second average current approximation, $\boxed{t_{pHL} = 360\text{ ps} + 45\text{ ps} = 405\text{ ps}}$

Problem 1.4

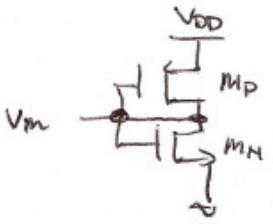
The Master stage latch in the flip-flop determines when a signal is "let in" or is the first of the two cascaded latches. In this case since the flip-flop is negative edge triggered, meaning that the output will hold the input value when the clock goes low, the master latch is active when the clock is high. The setup time is the time the input has to be stable before the active edge so that it can propagate to the input of the slave stage and be held. In this case, the longest possible propagation delay will determine the setup time. The longest propagation delay we see from the ideal clock pulse to the output changing to the 50% value is 412 ps. To be more conservative so that output reaches GND and since it's an ideal clock, it would most likely take another 45 ps resulting in a setup time of <u>457 ps.</u>

2. Flip-Flop

2.1

The Active low signal $\overline{CLR}$ drives the gate of transistor P_7. if $\overline{CLR}$ is set to "0", transistor P_7 pulls the gates of P_5 & N_5 up to V_{DD}. this sets Q low or clears Q and does not rely on the clock therefore it is Asynchronous.

2.2



$$I_P = I_N \Rightarrow \frac{K_N}{2}(V_{gs} - V_{TN})^2 = \frac{K_P}{2}(V_{DD} - V_m - |V_{TP}|)^2$$

$$\frac{K_N}{K_P}(V_m - V_{TN})^2 = (V_{DD} - V_m - |V_{TP}|)^2$$

$$\sqrt{\frac{K_N}{K_P}}(V_m - V_{TN}) = (V_{DD} - V_m - |V_{TP}|) \Rightarrow \sqrt{\frac{K_N}{K_P}} V_m + V_m = V_{DD} + \sqrt{\frac{K_N}{K_P}} V_{TN} - |V_{TP}|$$

Solve for V_m =

$$\frac{V_{DD} + \sqrt{\frac{K_N}{K_P}} V_{TN} - |V_{TP}|}{1 + \sqrt{\frac{K_N}{K_P}}}$$

The only difference between the c²mos stage and the inverter is the ratio of K_N/K_P

for the inverter

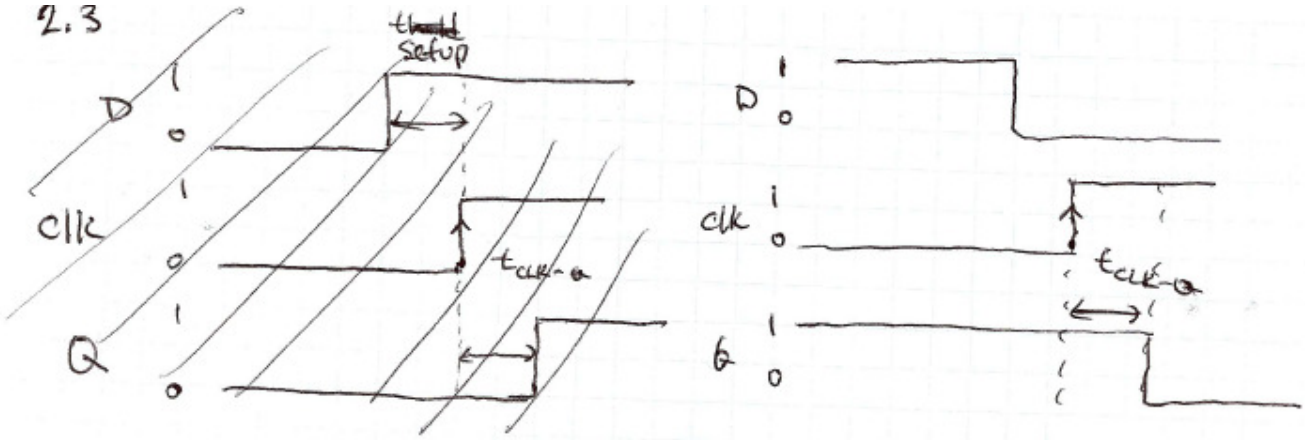
$$\frac{K_N}{K_P} = \frac{300\,\mu A/V^2 \cdot 1.4/0.6}{100\,\mu A/V^2 \; 2.8/0.6} = \frac{800}{466} = 1.7$$

for the c²mos

$$\frac{K_N}{K_P} = \frac{300\,\mu A/V^2 \cdot 1.4/1.2}{100\,\mu A/V^2 \; 2.8/1.2} = \frac{400}{233} = 1.7$$

The Ratios of K_N/K_P is equal so the thresholds (V_m) are equal.

2.3



When the clock is Low, the storage node formed by the gates of transistors N_1 & P_1 is discharged when the signal D ~~falls~~. is Low.

After the clock rises, the "0" stored on the gates of N_1 & P_1 is passed to Q. When the clock signal is high the C^2MOS stage drives the inverter formed By transistors N_5 & P_5 to a logic "1". ~~This inverter~~ then drives the output Q Low.

From the we see that we need to compute the delay through the C^2MOS stage & the inverter.

the total delay will be

$$t_{clk-Q} = \tau_{PLH_{C^2MOS}} + \tau_{PHL_{INV}}$$

to find these we need to determine the load capacitance & the average current for both individually.

$$\tau_{PLH\ C^2MOS} = \frac{C\,\Delta V}{I_{AVG}} \qquad \Delta V = V_{SS} \rightarrow V_{DD}/2 \quad (10\%\ V_{DD} \rightarrow 90\%\ V_{DD})$$

$$I_{AVG} = \frac{1}{2}\left(I_{sat,P} + I_{lin,P}\right)$$

$$I_{sat,P} = \frac{k_P}{2}\left(V_{DD} - |V_{TP}|\right)^2 \qquad k_P = \mu_p C_{ox} \cdot \frac{2.8}{1.2} = 233\ \mu A/V^2$$

$$I_{sat,P} = \frac{233.3\ \mu A/V^2}{2}\left(1.8 - |-0.7|\right)^2 = 141\ mA$$

Note: 2L is the effective length.

$$I_{LIN,P} = k_P\left[\left(V_{GS} - |V_{tp}|\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

LINEAR when $V_{DS} < V_{GS} - V_{t,P}$ $\quad V_{GS} = V_{DD}$

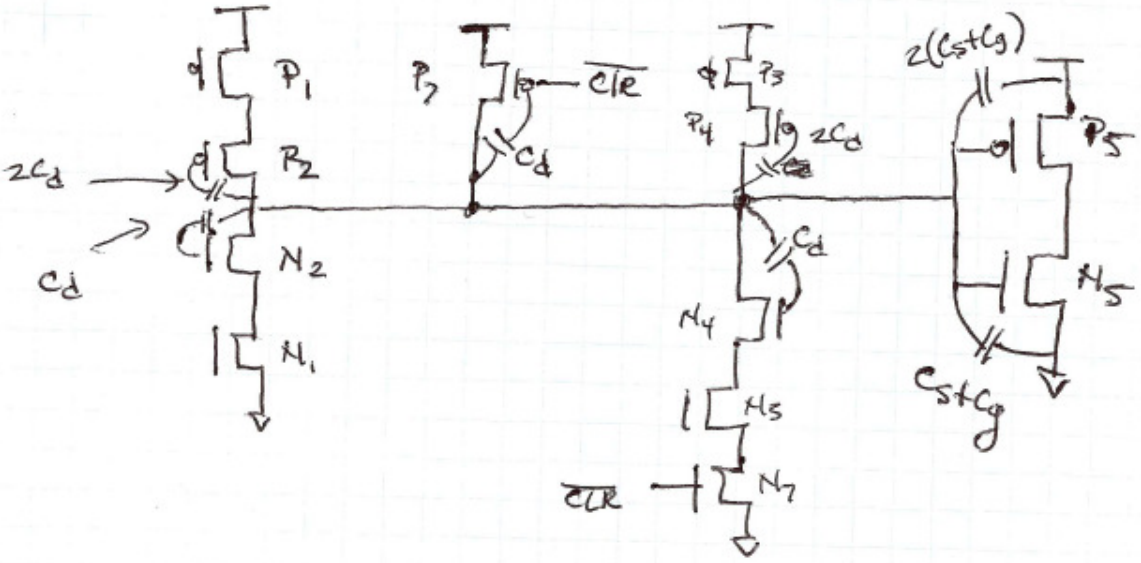
Assume mid point $V_{DS} = \frac{V_{DD} - |V_{TP}|}{2} = \frac{1.8 - |-0.7|}{2} = 0.65$

$$I_{LIN,P} = 233\ \mu A/V^2\left[\left(1.8 - |0.7|\right)0.65 - \frac{1}{2}\,0.65^2\right]$$

$$I_{LIN,P} = 233\ \mu A/V^2 \cdot 0.503\ V^2 = 117.5\ \mu A$$

$$I_{Avg_{PP}} = \frac{141\,mA + 118.5\,mA}{2} \approx 129.25\,mA$$

Next we need to find the total capacitance connected to the output of the C^2MOS stage.



ALL Pmos devices have capacitances which are 2x larger as they have twice the area.

$$C = 7C_d + 3C_s + 3C_g = 10C_s + 3C_g$$

$$C = 10 \cdot 10fF + 3 \cdot 15fF = 145fF$$

$$T_{PLH\ C^2MOS} = \frac{145fF \cdot 0.9V}{129.23\,mA} = 1nS$$

$$t_{PHL_{INV}} = \frac{C\Delta V}{I_{AVG}} \qquad I_{AVG} = \frac{1}{2}\left(I_{sat,N} + I_{Lin,N}\right)$$

$$I_{sat,N} = \frac{k_N}{2}\left(V_{GS} - V_{TN}\right)^2 \qquad k_N = \mu_N C_{ox}\frac{1.4}{0.6} = 700\,mA/V^2$$

$$I_{sat,N} = \frac{k_N}{2}\left(1.8 - 0.6\right)^2 = 504\,\mu A$$

$$I_{Lin,N} = k_N\left[\left(V_{GS} - V_{TN}\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Assume mid point $\quad V_{DS} = \frac{V_{DD} - V_{TN}}{2} = 0.6$

$$I_{Lin,N} = 700\,mA/V^2\left[\left(1.8 - 0.6\right)0.6 - \frac{1}{2}0.6^2\right] = 378\,mA$$

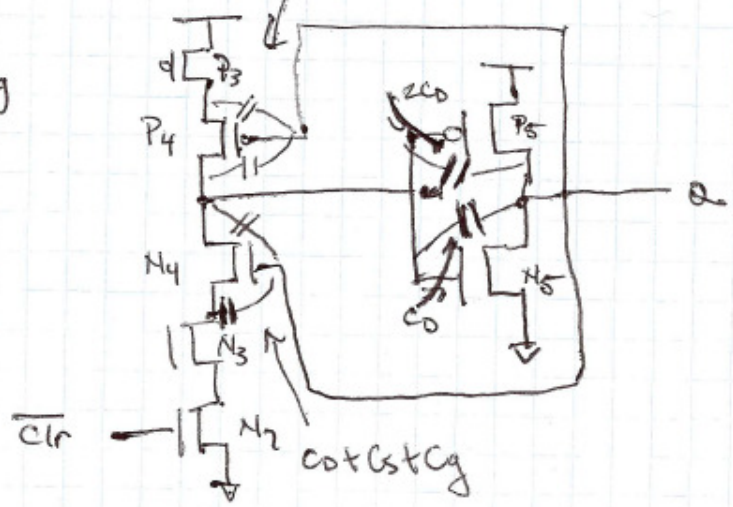
$$I_{AVG,N} = \frac{504\,\mu A + 378\,mA}{2} = 441\,mA$$

$2C_D + 2C_S + 2C_g$

$C = 6C_D + 3C_S + 3C_g$

$C = 9C_S + 3C_g$

$C = 135\,fF$

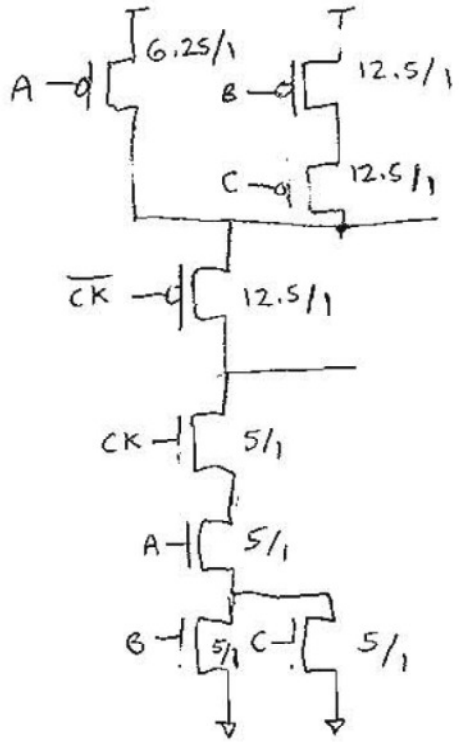


$$t_{PHL_{INV}} = \frac{135fF \cdot 0.9V}{441\,mA} = 0.276\,ns$$

$$T_{Clk-Q} = 1.276\,ns$$

3. Mixed Combinational and Sequential Logic

$F = A(B+C)$



For $t_{fall} = t_{rise}$, $\mu_n W_n = \mu_p W_p$

$\Rightarrow W_p = \frac{\mu_n}{\mu_p} W_n = 2.5\, W_n$

Other solutions possible ...