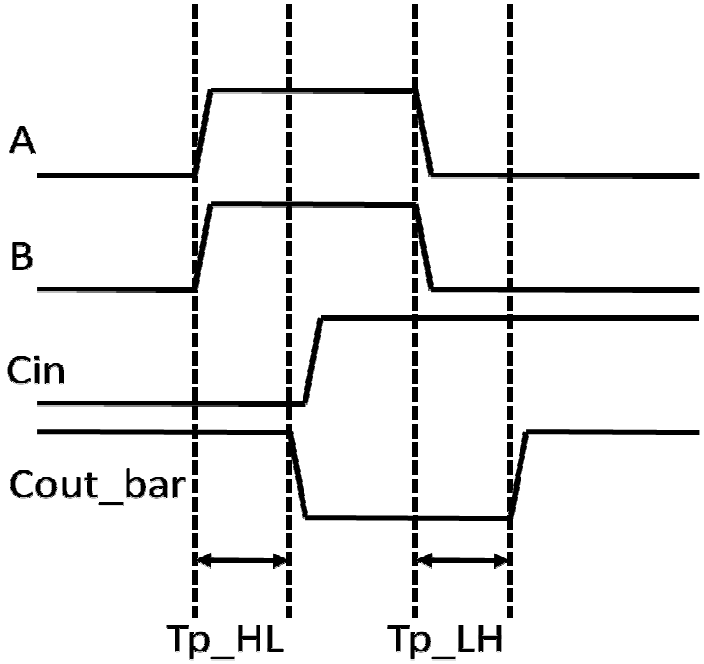
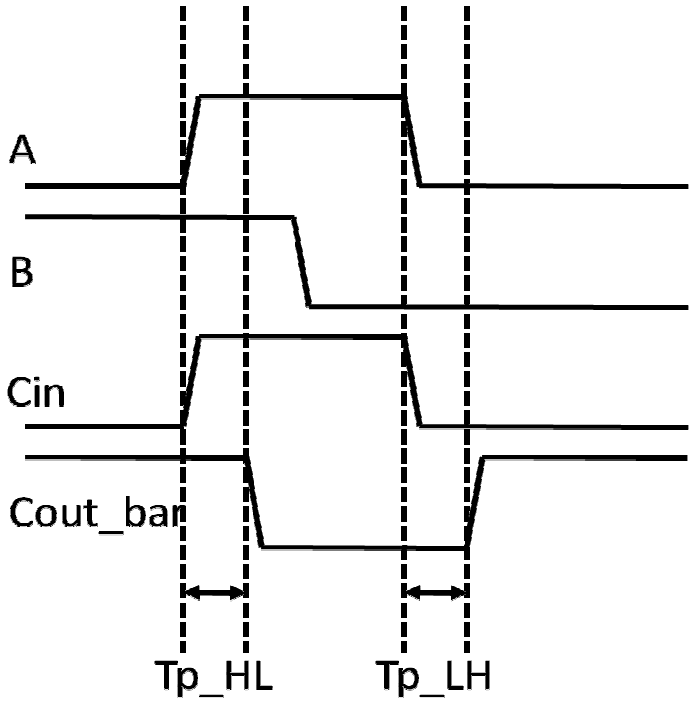
EEC116 Problem Set #3 Solution

1. Mirror Adder Delay Parameters

1.1



1.2



1.3

$$\tau_{pHL} = \frac{\frac{C_{load}V_{dd}}{2}}{I_{average}} = \frac{C_{load}V_{dd}}{I_{ds,NMOS,SAT}(Vout = Vdd) + I_{ds,NMOS,TRIODE}\left(Vout = \frac{Vdd}{2}\right)}$$

$$\tau_{pLH} = \frac{\frac{C_{load}V_{dd}}{2}}{I_{average}} = \frac{C_{load}V_{dd}}{I_{ds,PMOS,SAT}(Vout = 0) + I_{ds,PMOS,TRIODE}\left(Vout = \frac{Vdd}{2}\right)}$$

Worst Case:

$$k_p = \left(\frac{W}{L}\right)_P \mu_P C_{ox} = \frac{2}{0.8} * 150 = 375\ \mu A/V^2$$

$$k_n = \left(\frac{W}{L}\right)_N \mu_N C_{ox} = \frac{1}{0.8} * 300 = 375\ \frac{\mu A}{V^2}$$

Best Case:

$$k_p = \left(\frac{W}{L}\right)_P \mu_P C_{ox} = \frac{4}{0.8} * 150 = 750\ \mu A/V^2$$

$$k_n = \left(\frac{W}{L}\right)_N \mu_N C_{ox} = \frac{2}{0.8} * 300 = 750\ \frac{\mu A}{V^2}$$

Worst Case:

$$I_{ds,NMOS,SAT}(Vout = Vdd) = \frac{375 * 10^{-6}}{2}(1.8 - 0.4)^2 = 367.5\ uA$$

$$I_{ds,NMOS,TRIODE}\left(Vout = \frac{Vdd}{2}\right) = 375 * 10^{-6} * \left((1.8 - 0.4) * 0.9 - \frac{(0.9)^2}{2}\right) = 320.6\ uA$$

$$I_{ds,PMOS,SAT}(Vout = 0) = \frac{375 * 10^{-6}}{2}(1.8 - 0.5)^2 = 316.8\ uA$$

$$I_{ds,PMOS,TRIODE}\left(Vout = \frac{Vdd}{2}\right) = 375 * 10^{-6} * \left((1.8 - 0.5) * 0.9 - \frac{(0.9)^2}{2}\right) = 286.8\ uA$$

Best Case:

$$I_{ds,NMOS,SAT}(Vout = Vdd) = \frac{750 * 10^{-6}}{2}(1.8 - 0.4)^2 = 735\ uA$$

$$I_{ds,NMOS,TRIODE}\left(Vout=\frac{Vdd}{2}\right)=750*10^{-6}*\left((1.8-0.4)*0.9-\frac{(0.9)^2}{2}\right)=641.2\,uA$$

$$I_{ds,PMOS,SAT}(Vout=0)=\frac{750*10^{-6}}{2}(1.8-0.5)^2=633.6\,uA$$

$$I_{ds,PMOS,TRIODE}\left(Vout=\frac{Vdd}{2}\right)=750*10^{-6}*\left((1.8-0.5)*0.9-\frac{(0.9)^2}{2}\right)=573.7\,uA$$

Worst Case:

$$\tau_{pHL}=\frac{4.8*10^{-15}*1.8}{367.5\,uA+320.6\,uA}=12.5\,ps$$

$$\tau_{pLH}=\frac{4.8*10^{-15}*1.8}{316.8\,uA+286.8\,uA}=14.3\,ps$$

Best Case:

$$\tau_{pHL}=\frac{4.8*10^{-15}*1.8}{735\,uA+641.2\,uA}=6.2\,ps$$

$$\tau_{pLH}=\frac{4.8*10^{-15}*1.8}{633.6\,uA+573.7\,uA}=7.2\,ps$$

ALTERNATE SOLUTION FOR 1.3:

$$\tau_{pHL} = \frac{1}{k_n}\frac{C_{load}}{(V_{DD} - V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right]$$
$$= \frac{1}{k_n}\frac{4.8 * 10^{-15}}{(1.8 - 0.4)}\left[\frac{2 * 0.4}{1.8 - 0.4} + \ln\left(\frac{4(1.8 - 0.4)}{1.8} - 1\right)\right] = \frac{1}{k_n} * 4.52 * 10^{-15}$$

$$\tau_{pLH} = \frac{1}{k_p}\frac{C_{load}}{(V_{DD} - |V_{T,p}|)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right)\right]$$
$$= \frac{1}{k_p}\frac{4.8 * 10^{-15}}{(1.8 - 0.5)}\left[\frac{2 * 0.5}{1.8 - 0.5} + \ln\left(\frac{4(1.8 - 0.5)}{1.8} - 1\right)\right] = \frac{1}{k_p} * 5.18 * 10^{-15}$$

Worst Case:

$$k_p = \left(\frac{W}{L}\right)_P \mu_P C_{ox} = \frac{2}{0.8} * 150 = 375\ \mu A/V^2$$

$$k_n = \left(\frac{W}{L}\right)_N \mu_N C_{ox} = \frac{1}{0.8} * 300 = 375\ \frac{\mu A}{V^2}$$

Best Case:

$$k_p = \left(\frac{W}{L}\right)_P \mu_P C_{ox} = \frac{4}{0.8} * 150 = 750\ \mu A/V^2$$

$$k_n = \left(\frac{W}{L}\right)_N \mu_N C_{ox} = \frac{2}{0.8} * 300 = 750\ \frac{\mu A}{V^2}$$

Worst Case:

$$\tau_{pHL} = \frac{1}{k_n} * 4.52 * 10^{-15} = 12\ ps$$

$$\tau_{pLH} = \frac{1}{k_p} * 5.18 * 10^{-15} = 13.3\ ps$$

Best Case:

$$\tau_{pHL} = \frac{1}{k_n} * 4.52 * 10^{-15} = 6\ ps$$

$$\tau_{pLH} = \frac{1}{k_p} * 5.18 * 10^{-15} = 6.66\ ps$$

1.4 To find Resistance, Rds:

Worst Case:

$$\left(\frac{W}{L}\right)_P = \frac{2}{0.8}; \quad I_{ds} = \frac{\left(150 * 10^{-6} * \frac{2}{0.8}\right)}{2}(1.8 - 0.5)^2 = 316.8uA$$

$$\left(\frac{W}{L}\right)_N = \frac{1}{0.8}; \quad I_{ds} = \frac{\left(300 * 10^{-6} * \frac{1}{0.8}\right)}{2}(1.8 - 0.4)^2 = 367.5uA$$

Best Case:

$$\left(\frac{W}{L}\right)_P = \frac{4}{0.8}; \quad I_{ds} = \frac{\left(150 * 10^{-6} * \frac{4}{0.8}\right)}{2}(1.8 - 0.5)^2 = 633.75uA$$

$$\left(\frac{W}{L}\right)_N = \frac{2}{0.8}; \quad I_{ds} = \frac{\left(300 * 10^{-6} * \frac{2}{0.8}\right)}{2}(1.8 - 0.4)^2 = 735uA$$

Worst Case:

$$R_{ds,P} = \frac{V_{ds}}{I_{ds}} = \frac{1.8}{316.8uA} = 5681.8\ Ohms;$$
$$t_{rise} = R_{ds,P} C_{load} \ln\left(\frac{0.9Vdd}{0.1Vdd}\right) = 5681.8 * 4.8fF * \ln(9) = 59\ ps$$
$$R_{ds,N} = \frac{V_{ds}}{I_{ds}} = \frac{1.8}{367.5uA} = 4897.9\ Ohms;$$
$$t_{fall} = 4897.9 * 4.8fF * \ln(9) = 52\ ps$$

Best Case:

$$R_{ds,P} = \frac{V_{ds}}{I_{ds}} = \frac{1.8}{633.75uA} = 2840.2\ Ohms;$$
$$t_{rise} = 2840.2\ * 4.8fF * \ln(9) = 30\ ps$$

$$R_{ds,N} = \frac{V_{ds}}{I_{ds}} = \frac{1.8}{735uA} = 2448.9\ Ohms;$$
$$t_{fall} = 2448.9 * 4.8fF * \ln(9) = 26\ ps$$

2. Power Dissipation Components

2.1 From the power equation, total power is equal to the sum of dynamic and static/leakage power.

*load capacitance = Dynamic power / (supply voltage squared * frequency)*

But we are only given **total power** and not dynamic power. If leakage is negligible when compared to the dynamic power, then we create the table below to obtain the load capacitance while letting total power=dynamic power. With this, the load capacitance is around **2.8 uF**.

Frequency (MHz)	Total Power (uW)	Load Cap (not accounting leakage)
10	101.3	**3.12654E-06**
20	190.4	**2.93827E-06**
30	279.5	**2.87551E-06**
40	368.6	**2.84414E-06**
50	457.7	**2.82531E-06**
60	546.8	**2.81276E-06**
70	635.9	**2.80379E-06**
80	725	**2.79707E-06**
90	814.1	**2.79184E-06**
100	903.2	**2.78765E-06**

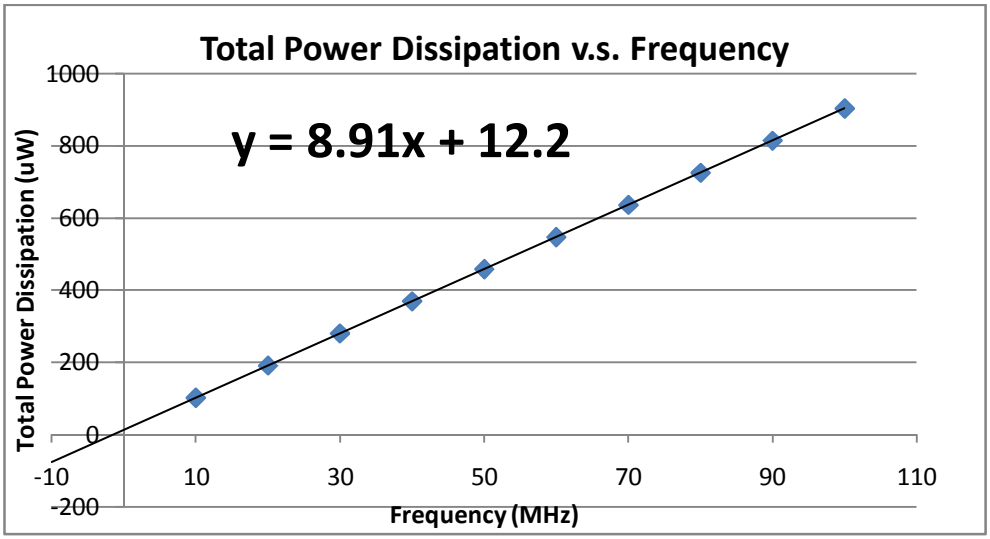
Using results from problem 2.2, we modify the above table and correct the load capacitance by subtracting the leakage power (12.2 uW) from the total power. From table below, load capacitance is 2.75 uF

*load capacitance =(Total power-Leakage Power) / (supply voltage squared * frequency)*

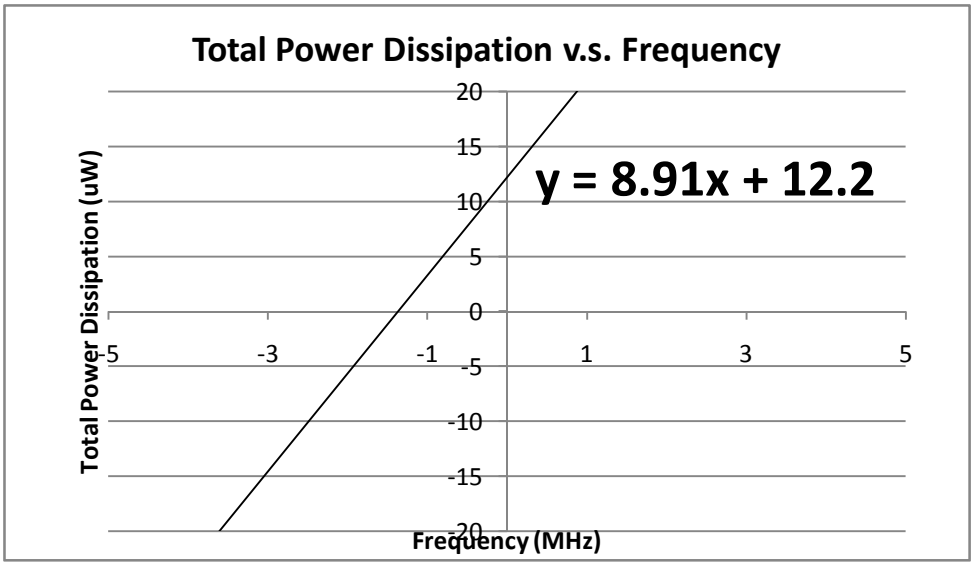
Frequency (MHz)	Total Power (uW)	Load Cap (not accounting leakage)	Load Cap (accounting leakage)
10	101.3	3.12654E-06	**2.75E-06**
20	190.4	2.93827E-06	**2.75E-06**
30	279.5	2.87551E-06	**2.75E-06**
40	368.6	2.84414E-06	**2.75E-06**
50	457.7	2.82531E-06	**2.75E-06**
60	546.8	2.81276E-06	**2.75E-06**
70	635.9	2.80379E-06	**2.75E-06**
80	725	2.79707E-06	**2.75E-06**
90	814.1	2.79184E-06	**2.75E-06**
100	903.2	2.78765E-06	**2.75E-06**

2.2 If we plot the data given, we obtain a graph with total power dissipation at the Y axis, and Frequency at the X axis. We can find the leakage power by plotting a trendline for the data, and look at the power consumption when frequency = 0, this gives us the leakage power.

Note: the slope, 8.91 is simply the dynamic energy (in uJ), which is equal to C*Vdd*Vdd. If you divide 8.91 by Vdd squared, you obtain 2.75 uF, which is the load capacitance calculated before.



Zoomed version of the same plot above shows the leakage power more clearly.



From the plot above, we see the static/leakage power is approx 12.2 uW (at frequency = 0).

This gives a leakage current of <u>12.2 uW / 1.8 V = 6.7uA</u>

3. Floorplanning and Layout Optimization

In the Lagrange Multiplier Method, we like to minimize a function f() while satisfying some constraint given by g()=c;
For two variables x and y, we can formulate the problem as:

minmize f(x,y)
such that g(x,y)

Using g and f above, we can write the formula below where lambda is the lagrange multipler.

f(x,y) = lambda * g(x,y) (1)
f(x,y) – lambda * g(x,y) = 0 (2)

To solve the equation above, we calculate the partial derivatives of (2), set them to 0, and solve the results simultaneously for x and y. See 3.1 and 3.2 for example.

3.1 Intuitively, the minimum area is the area taken up by the N required full adders, which is just **Amin = N*Lx*Ly.** But the question remains: what is the optimal shape of the final N-bit full adder layout?

Here, we will use Lagrange Multipliers to verifiy our intuition. We will minimize the area, such that the overall outline is a rectangle.

minmize f(x,y)=xy

such that g(x,y)=2x+2y

Using Eq. (2), we write: xy – lambda *(2x+2y)

Partial derivative wrt. X : y – lambda*2 = 0 -> y = 2*lambda

Partial derivative wrt. Y: x – lambda*2 = 0 -> x = 2*lambda

** The results above shows x = y = 2*lambda, which implies the geometry of the overall layout should be a square, and x = y = sqrt(N) for an N-bit adder.

3.2 Here, we will minimize the perimeter such that the overall area is a rectangle.

minmize f(x,y)= 2x+2y

such that g(x,y)=xy

Using Eq. (2), we write: 2x+2y – lambda *(xy)

Partial derivative wrt. X : 2 – lambda*y = 0 -> y = 2 / lambda

Partial derivative wrt. Y: 2 – lambda*x = 0 -> x = 2 / lambda

** The results above show x = y = 2 / lambda, which implies the geometry of the overall layout should be a square, and x = y for an N-bit adder. Pmin = 2*sqrt(N)*Lx + 2*sqrt(N)*Ly = 4 * sqrt(N)*Lx