EEC116 Problem Set #2 Solution

1. FET Capacitances

1.1

Assuming an abrupt junction (m=0.5). Drain voltage is negative when the DB junction is reverse biased, which is the case we have. (Rabaey page 76, 82, 83, 111)

$$\emptyset_r = \frac{kT}{q} = 0.026V, \;\; \emptyset_0 = \emptyset_T \ln\left(\frac{N_A N_D}{{N_i}^2}\right) = 0.026\ln\left(\frac{10^{16} * 10^{20}}{(1.5 * 10^{10})^2}\right) = 0.933V$$

$$C_{j0} = \sqrt{\left(\frac{\varepsilon_{si} q}{2}\frac{N_A N_D}{N_A + N_D}\right)\emptyset_0^{-1}} = \sqrt{\left(\frac{\varepsilon_{si} q}{2}\frac{N_A N_D}{N_A + N_D}\right)\emptyset_0^{-1}} = \sqrt{\left(\frac{11.7 * 8.854 * 10^{-14}}{2}\frac{10^{16} * 10^{20}}{10^{16} + 10^{20}}\right)\frac{1}{0.933}}$$
$$= 2.98 * \frac{10^{-8}F}{cm^2}$$

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{\emptyset_0}\right)^m} = \frac{2.98 * 10^{-8}}{\left(1 - \frac{-5}{0.933}\right)^{0.5}} = 1.18 * 10^{-8} F/cm^2$$

$$\emptyset_{0+} = \emptyset_T \ln\left(\frac{N_{A+} N_D}{{N_i}^2}\right) = 0.026\ln\left(\frac{10^{19} * 10^{20}}{(1.5 * 10^{10})^2}\right) = 1.111V$$

$$C_{jsw0} = \sqrt{\left(\frac{\varepsilon_{si} q}{2}\frac{N_{A+} N_D}{N_{A+} + N_D}\right)\emptyset_{0+}^{-1}} = \sqrt{\left(\frac{11.7 * 8.854 * 10^{-14}}{2}\frac{10^{19} * 10^{20}}{10^{19} + 10^{20}}\right)\frac{1}{1.111}} = 8.23 * 10^{-7} F/cm^2$$

$$C_{jsw} = \frac{C_{jsw0}}{\left(1 - \frac{V_D}{\emptyset_{0+}}\right)^m} = \frac{8.23 * 10^{-7}}{\left(1 - \frac{-5}{1.111}\right)^{0.5}} = 3.51 * 10^{-7} F/cm^2$$

$C_{diff} = C_{bottom} + C_{sw}$

$= C_j * AREA + C_{jsw} * PERIMETER = C_j L_s W + C_{jsw} x_j (2L_s + W)$

$= (1.18 * 10^{-8})(5 * 10^{-4})(10 * 10^{-4}) + (3.51 * 10^{-7})(0.4 * 10^{-4})(2(5 * 10^{-4}) + 10 * 10^{-4})$

$= \mathbf{34} * \mathbf{10^{-15}} \boldsymbol{F}$

$@ V_D = 2.5 \rightarrow C_{diff} = \mathbf{44} * \mathbf{10^{-15}} \boldsymbol{F}$

1.2 $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 * 8.854 * 10^{-14}}{200 * 10^{-8}} = 1.7 * 10^{-7}\frac{F}{cm^2}$$

$$C_{GD}(overlap) = C_{ox} W x_d = (1.7 * 10^{-7})(10 * 10^{-4})(0.25 * 10^{-4}) = \mathbf{4.31} * \mathbf{10^{-15}} \boldsymbol{F}$$

2. Enhancement Load Inverter

Problem 2.1

For V_{OH}, The load transistor is diode connected and forced to operate in saturation. This requires at least a threshold drop across the transistor, and so the NMOS cannot pull the output all the way up to V_{DD}.

$$V_{T,LOAD} = V_{T0,LOAD} + \gamma\left(\sqrt{|2\phi_F + V_{OH}|} - \sqrt{|2\phi_F|}\right)$$

$$V_{OH} = V_{DD} - V_{T,LOAD} \Rightarrow V_{T,LOAD} = V_{DD} - V_{OH}$$

$$V_{DD} - V_{OH} = V_{T0,LOAD} + \gamma\left(\sqrt{|2\phi_F + V_{OH}|} - \sqrt{|2\phi_F|}\right)$$
$$\Rightarrow 5 - 0.8 = V_{OH} + 0.38\sqrt{0.6 + V_{OH}} - 0.38\sqrt{0.6}$$

$$(4.5 - V_{OH})^2 = \left(0.38\sqrt{0.6 + V_{OH}}\right)^2$$
$$\Rightarrow {V_{OH}}^2 - 9.132V_{OH} + 20.109 = 0 \Rightarrow V_{OH} = \underline{\underline{3.706V}}$$

For V_{OL}, the load operates in saturation, while the driver is linear.

$$I_{driver} = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)_d \left(2(V_{DD} - V_{T0})V_{OL} - {V_{OL}}^2\right)$$

$$I_{load} = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)_l (V_{DD} - V_{OL} - V_{T,load})^2$$
$$\Rightarrow I_{load} = \frac{\mu C_{OX}}{2}\left(\frac{W}{L}\right)_l \left(V_{DD} - V_{OL} - V_{T0} - \gamma\left(\sqrt{|2\phi_F + V_{OL}|} - \sqrt{|2\phi_F|}\right)\right)^2$$

$$I_{driver} = I_{load}$$

$$I_{load} = 22.5\left(4.494 - V_{OL} - 0.38\sqrt{0.6 + V_{OL}}\right)^2$$
$$I_D = 1512V_{OL} - 180{V_{OL}}^2$$

Using these two equations, we can iteratively solve for V_{OL}.

$V_{OL}(V)$	$I(\mu A)$
1	204.3
0.1373	365.5
0.2491	341.3
0.2346	344.4
0.2342	344.5
0.2343	344.4

$$V_{OL} = \underline{\underline{0.2343V}}$$

Problem 2.2

$$NM_L = V_{IL} - V_{OL} \Rightarrow V_{IL} - 0.23$$
$$NM_H = V_{OH} - V_{IH} \Rightarrow 3.7 - V_{IH}$$

We see that in contrast to a CMOS inverter, we can not get our outputs to either rail. This results in reduced noise margins and robustness of operation.

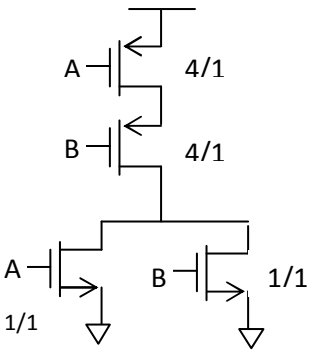
Because the outputs do not go rail to rail, and the load transistor is always on, a constant DC current flows, resulting in constant power dissipation, unlike a CMOS inverter.

Problem 2.3

When $V_{in}=V_{OH}$ the driver transistor operates in the linear region and the current is the same through both transistors.

$$I_{driver} = \mu_n C_{OX}\left(\frac{W}{L}\right)\left(2(V_{OH} - V_{T0})V_{OL} - V_{OL}{}^2\right)$$
$$= \frac{45}{2} \times 8\left(2(3.7 - 0.8)0.234 - 0.234^2\right)$$
$$= \underline{\underline{234\mu A}}$$

3. Two Input CMOS NOR Gate



$V_{OH} = 5\ volts\ and\ V_{OL} = 0\ volts$

An equivalent inverter would have $\left(\frac{W}{L}\right)_P = \left(\frac{W}{L}\right)_N = \frac{2}{1}$, therefore

$$k_p = \left(\frac{W}{L}\right)_P \mu_P C_{ox} = 2 * 20 = 40\ \mu A/V^2$$

$$k_N = \left(\frac{W}{L}\right)_N \mu_N C_{ox} = 2 * 40 = 80\ \mu A/V^2$$

$$k_R = \frac{k_N}{k_p} = \frac{80}{40} = 2$$

$$V_{IL} = \frac{2V_{out}+V_{th,p}-Vdd+k_R V_{th,n}}{1+k_R} = \frac{2V_{out}+0.7-5+1.4}{3} \rightarrow V_{out} = 1.5V_{IL} + 0.97 \quad (1)$$

$$\frac{k_n}{2}(V_{IN} - V_{TH,N})^2 = \frac{k_P}{2}\left(2\left(V_{IN} - V_{dd} - V_{TH,P}\right)(V_{OUT} - V_{dd}) - (V_{OUT} - V_{dd})^2\right)$$

$$\rightarrow 40(V_{IL} - 0.7)^2 = 20(2(V_{IL} - 5 + 0.7)(V_{OUT} - 5) - (V_{OUT} - 5)^2) \quad (2)$$

Now Plug (1) into (2) for V_{OUT} and solve for V_{IL}

$$\rightarrow\ 1.25V_{IL}^2 + 6.07V_{IL} - 17.43 = 0$$

$$\boldsymbol{V_{IL} = 2.02\ volts}$$

$$V_{IH} = \frac{V_{dd} + V_{th,p} + k_R(2V_{out}+V_{th,n})}{1 + k_R} = \frac{5 - 0.7 + 2(2V_{out} + 0.7)}{3}$$

$$\rightarrow V_{out} = 0.75V_{IH} - 1.425 \quad (3)$$

$$\frac{k_n}{2}\left(2\left(V_{IH} - V_{TH,N}\right)V_{OUT} - {V_{OUT}}^2\right) = \frac{k_P}{2}\left(V_{IH} - V_{dd} - V_{th,p}\right)^2$$

$$\rightarrow\ 40(2(V_{IH} - 0.7)V_{out} - V_{out}^2) = 20(V_{IH} - 5 + 0.7)^2 \quad (4)$$

$$Now\ plug\ equation\ (3) into (4) for\ V_{out} and\ solve\ for\ V_{IH}$$

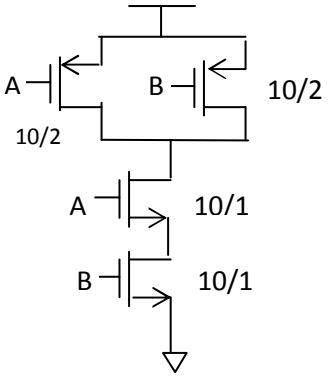
$$\rightarrow 0.88V_{IH}^2 + 5.08V_{IH} - 18.56 = 0$$

$$\rightarrow \boldsymbol{V_{IH} = 2.53\ volts}$$

$$\boldsymbol{NM_L = V_{IL} - V_{OL} = 2.02V}$$

$$\boldsymbol{NM_H = V_{OH} - V_{IH} = 2.47V}$$

4. Two Input CMOS NAND Gate



An equivalent inverter would have $\left(\frac{W}{L}\right)_P = \left(\frac{W}{L}\right)_N = \frac{10}{2}$, therefore

$$k_p = \left(\frac{W}{L}\right)_P \mu_P C_{ox} = 5 * 10 = 50\ \mu A/V^2$$

$$k_N = \left(\frac{W}{L}\right)_N \mu_N C_{ox} = 5 * 20 = 100 \frac{\mu A}{V^2}$$

$$\tau_{pHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{pLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right)\right]$$

$$\tau_{pHL} = \frac{0.1 * 10^{-12}}{100 * 10^{-6}(4)}\left[\frac{2}{4} + \ln\left(\frac{4 * 4}{5} - 1\right)\right] = \mathbf{0.675ns}$$

$$Note: \tau_{pLH} is\ simply\ 2\tau_{pHL}\ because k_N = 2 * k_P$$

$$\rightarrow \boldsymbol{\tau_{pLH} = 1.35ns}$$

5. Logic Circuit

5.1

Remember:

$-$ *two switches in series have a logic al AND relationship,*

$-$*two switches in parallel have a logical OR relationship*

So we obtain the following expression for F,

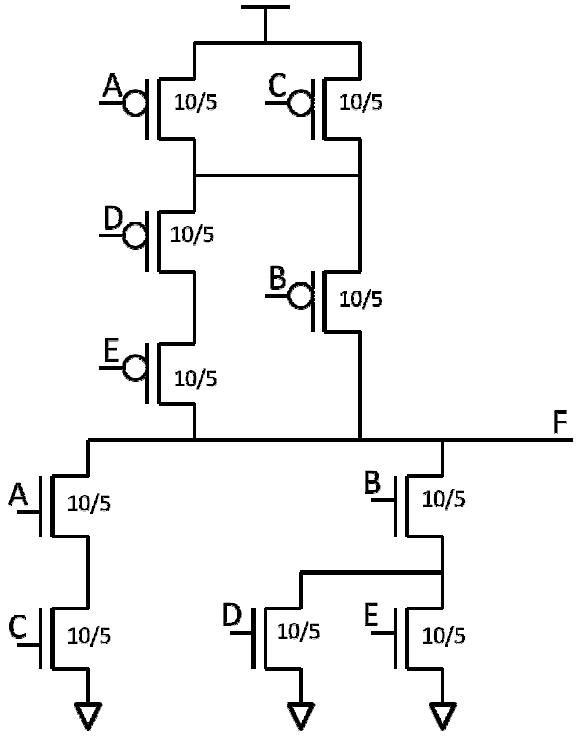
$$F = \overline{(A \cdot C) + \big(B \cdot (D + E)\big)}$$

The expression is negated (*a bar on top*)*because the schematic given is the PDN*.

5.2

The complete circuit is shown below.

The goal: size the worse case pull up and pull down path's resistance to the resistance of a minimum sized NMOS – W/L=10/5
To size the individual transistors, we start by assigning the minimum W/L to every transistor.



1) Let's find the worse case pull-down path. We notice the worse case path in the PULL DOWN network is two transistors long, and three possible paths, AC, BD, or BE. We double the widths of all transistors here so the worse case path will have the same resistance as a single NMOS. So W/L of all NMOS = 20/5
2) We now move onto the PULL UP network. Let's first account for the difference in process parameters:
   - Since lambda is zero, and the threshold voltage for PMOS and NMOS are symmetrical (ignoring body effect), we only need to account for the difference in mu Cox between N and P MOS. Notice the 3x relationship.

   - So we increase the size of each PMOS transistor by 3 times. So W/L of all PMOS = 30/5
3) Now equalize for the worse case. The worse case here is three transistors long, and two possible paths: ADE or CDE. We triple the sizes of each of those transistors. So W/L for the PMOS transistor for inputs A, C, D, and E are 90/5.
4) Now we move onto the last transistor. What do we do with the PMOS for input B? This transistor participate in the paths BC and BA where transistors A and C both have W/L=90/5. We must make sure these two paths meet the worse case pull up resistance requirement, too. We compare the resistance of these two paths to the resistance of a single NMOS. We perform the following analysis:

$$R_{nmos} \geq?\ R_{pmos,B} + R_{pmos,A} \qquad (want)$$

$$\left(\frac{1}{uCox\left(\frac{W}{L}\right)}\right)_{nmos} \geq? \left(\frac{1}{uCox\left(\frac{W}{L}\right)}\right)_{pmos,B} + \left(\frac{1}{uCox\left(\frac{W}{L}\right)}\right)_{pmos,A}$$

$$\left(\frac{1}{300\left(\frac{10}{5}\right)}\right)_{nmos} \geq? \left(\frac{1}{100\left(\frac{30}{5}\right)}\right)_{pmos,B} + \left(\frac{1}{100\left(\frac{90}{5}\right)}\right)_{pmos,A} \qquad (\boldsymbol{equation\ 1})$$

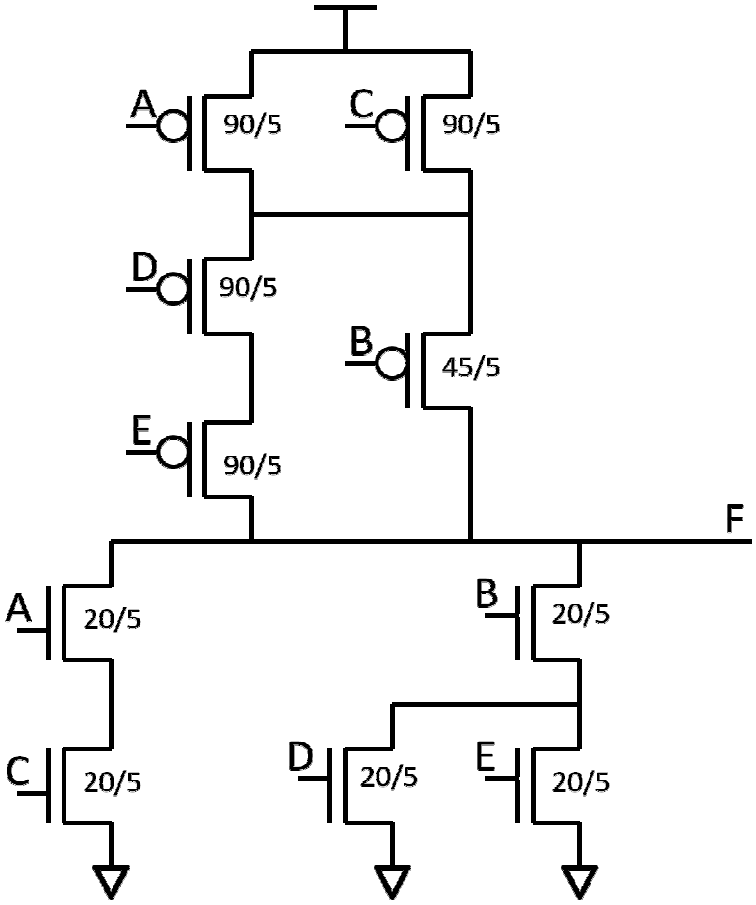
$$\frac{1}{3000} \geq? \frac{1}{3000} + \frac{1}{9000} = \frac{4}{9000} = \frac{1}{2250}$$

We see that this condition is FALSE, so W/L=30/5 is NOT OK and we need to increase it. So let's equate the RHS and LHS of equation (1) and solve for $\left(\frac{W}{L}\right)$ of the B input PMOS.

$$\frac{1}{600} = \frac{1}{100\left(\frac{W}{L}\right)} + \frac{1}{1800}$$

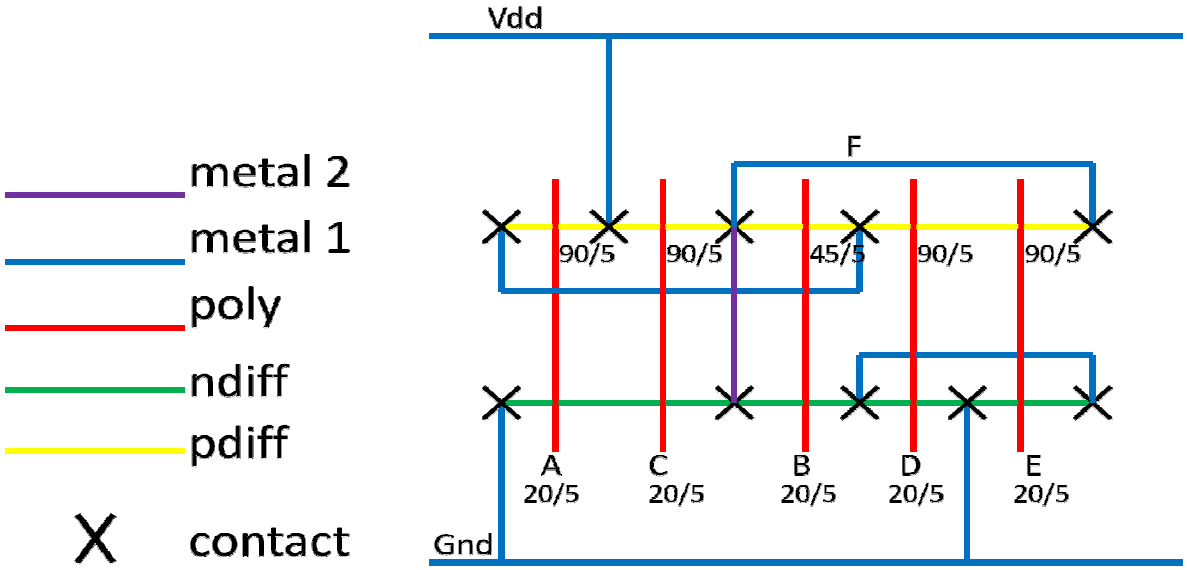
$$3 = \frac{18}{\left(\frac{W}{L}\right)} + 1 \quad \rightarrow \left(\frac{W}{L}\right) = \frac{18}{2} = 9 = \frac{45}{5}$$

We see W/L of the PMOS for input B needs to be 45/5. A final schematic with sizes is shown below.



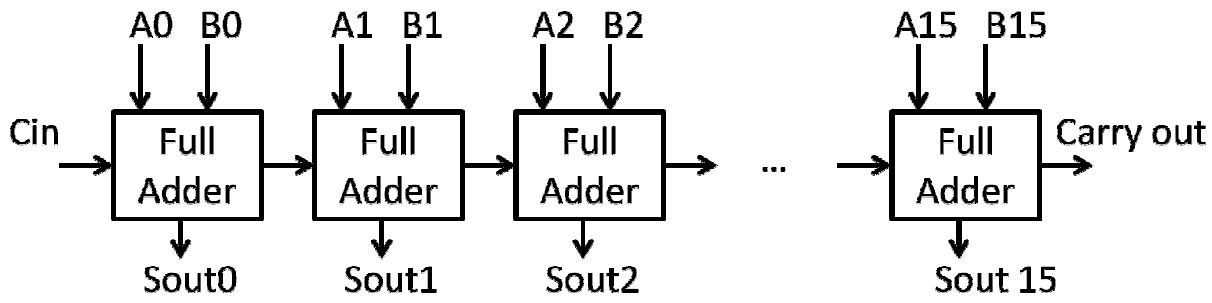
5.3

Stick Diagram.



6. Ripple Carry Adder Delay

A 16-bit carry ripple adder is shown below.



The delay for the carry output and sum output for the individual full adders are given, they are:

$$\tau_{p,sum} = \frac{3.0n + 3.9n}{2} = 3.45ns$$

$$\tau_{p,cout} = \frac{3.2n + 4.5n}{2} = 3.85ns$$

The worse case path occurs when a change in either Cin,A0, or B0 causes Carry out to toggle. The signal change propagates from the least significant FA to the most significant FA through the carry in and carry out ports. The delay of this path is:

$$\tau_{p,worse\ case} = \tau_{adder} = 16\tau_{p,cout} = 61.6ns$$