EEC116 Problem Set #1 Solution

# 1.IC Trends

1.1 Here, we can derive a formula for exponential growth.

$$x_1 = x_0 + x_0 * r; \quad (1)$$

$where\ x_0\ is\ the\ starting\ amount, r\ is\ the\ rate\ of\ growth\ or\ decay, and\ x_1\ is\ the\ new\ amount.$

$If\ the\ growth\ or\ decay\ is\ repeated\ at\ a\ regular\ interval, we\ can\ write\ the\ expressions\ below,$

$$for\ the\ second\ growth\ or\ decay,\ x_2 = x_1 + x_1 * r; (2)$$

...

$$for\ the\ nth\ growth\ or\ decay, \quad x_n = x_{n-1} + x_{n-1} * r;$$

$Substituting\ (1)\ into\ (2)\ and\ we\ obtain\ the\ following,\ x_2 = x_0 + 2x_0 r + x_0 r^2 = x_0(1+r)^2$

$$\boldsymbol{Generalizing\ this\ expression, we\ obtain\ y = x(1+r)^n}$$

$$\boldsymbol{where\ x\ is\ the\ starting\ value, n\ is\ the\ number\ of\ times\ x\ grows,}$$

$$\boldsymbol{r\ is\ the\ rate\ of\ growth, and\ y\ is\ the\ final\ value.}$$

$Note: this\ is\ the\ same\ formula\ for\ calculating\ compound\ interest.$

$Integration\ complexity\ assumes\ growth\ of\ 4x\ (r = 3)\ every\ 3\ years\ as\ on\ page\ 7\ of\ Rabaey.$

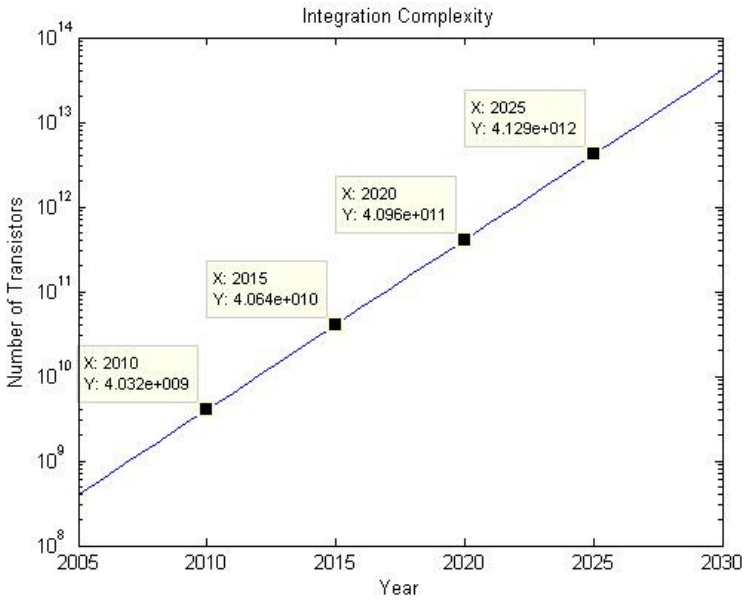
$Starting\ with\ 400M\ transistors\ in\ year\ 2005,$

$@2010 \rightarrow n = 5, y = 400 * 10^6(4)^{\frac{5}{3}} \cong 4\ billion\ transistors$

$@2015 \rightarrow n = 10, y = 400 * 10^6(4)^{10/3} \cong 40\ billion\ transistors$

$@2020 \rightarrow n = 15, y = 400 * 10^6(4)^{15/3} \cong 400\ billion\ transistors$

$@2025 \rightarrow n = 20, y = 400 * 10^6(4)^{20/3} \cong 4000\ billion\ transistors$




*Frequency assumes growth of* $2x$ $(r = 1)$ *every* $2$ *years.*

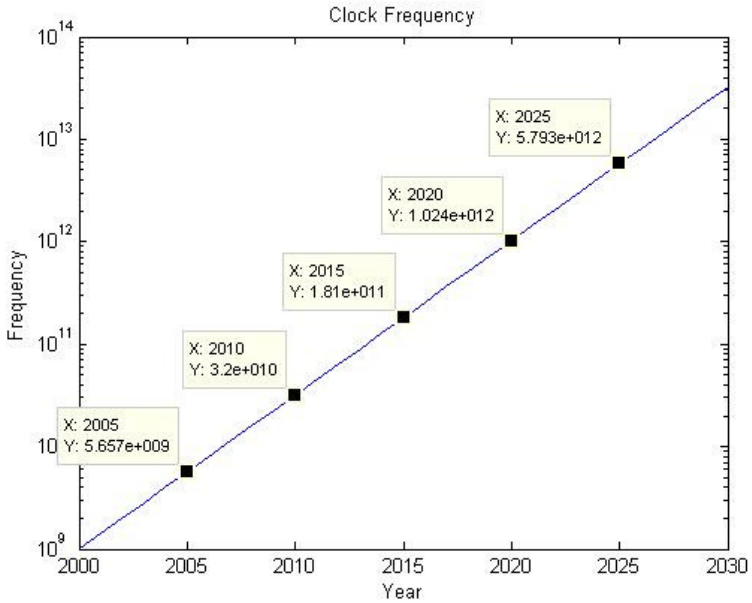
*Starting with* $1GHz$ *in* $2000$,

@2010 $\rightarrow n = 10, y = 1 * 10^9(2)^{\frac{10}{2}} \cong 3.2 * 10^{10}\ Hz$

@2015 $\rightarrow n = 15, y \cong 1.810 * 10^{11}\ Hz$

@2020 $\rightarrow n = 20, y \cong 1.024 * 10^{12}\ Hz$

@2025 $\rightarrow n = 25, y \cong 5.7 * 10^{12}\ Hz$



From lecture 1 slide #15, the average number of transistors on a single die in year 2009 is approx. 10 billion. On slide #10 it is approx. 2 to 2.6 billion. Our prediction is approx. 4 billion transistors in 2010 which is in the same range as the data. Moore's law for integration complexity is fairly accurate.

On the other hand, clock frequencies have saturated at around 3 to 5 GHz, no longer following Moore's law. A continued increase in clock rate will cause digital systems to dissipate unacceptable amount of power. Additionally, the overhead and cost to reliably deliver clock signals is too high at extremely high frequencies. To compensate for the saturating clock frequency, microprocessor's throughput is usually maintained by adding additional processing cores.

1.2

$Number\ of\ DRAM\ bits\ assumes\ growth\ of\ 2x\ (r = 1) every\ 18 months\ as\ on\ page\ 7\ of\ Rabaey.$

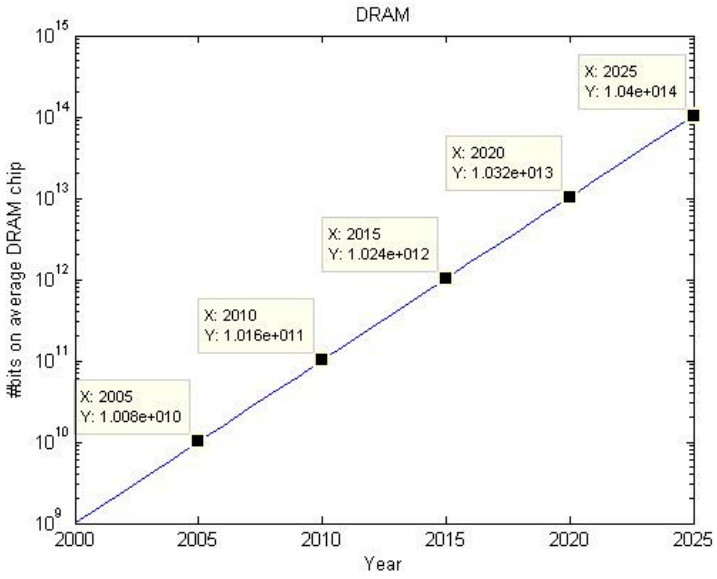
$Starting\ with\ 1\ Gb\ in\ year\ 2000,$

$@2010 \rightarrow n = 10, y = 1 * 10^9(2)^{\frac{10}{1.5}} \cong 100Gb$

$@2015 \rightarrow n = 15, y \cong 1000Gb = 1Tb$

$@2020 \rightarrow n = 20, y \cong 10Tb$

$@2025 \rightarrow n = 25, y \cong 100Tb$




From lecture 1 slide #11, we see the number of bits in a DRAM chip is about 64 Gb in 2009, our prediction is 100Gb in 2010. Moore's law for DRAM is accurate.

# 2.Quality Metrics

There is no "right" answer to this problem. What is considered a priority is almost entirely dependent on what the target application is, as well as how your company wishes to market its product(s).

All of these metrics can also influence each other. Pretend we are designing a processor to go into the next generation of cell phones. Power might be our #1 priority to enable the phone to run a long time without charging. We could lower the clock frequency (performance), remove support for some functions (robustness/functionality), or even add dedicated circuitry (cost) all of which are capable of reducing power. But as with all of engineering, nothing comes for free.

# 3. MOS Transistor

3.1 The electrical channel length is shorter than the drawn channel length due to lateral diffusions of the source and drain underneath the drawn gate (p.92 Rabaey). An equation which models this difference is given below, where $Ld$ indicates the drawn channel length, ΔL gives the total diffusion difference, and $Xd$ gives the diffusion difference of one side of the channel. Note that this effect is always on, and differs from pinching off of the channel.

$$Ld = L - \Delta L = L - 2Xd$$

3.2 1) NMOS: VGS=1.8V, VDS=1.8V -> Saturation
PMOS: VGS=-1.1V, VDS=-50mV -> Triode/Linear

$$I_{d,nmos} = \frac{(350 * 10^{-6} * 4)}{2}(1.8 - 0.7)^2(1 + 0.05 * 1.8) = 923uA$$

$$I_{d,pmos} = (150 * 10^{-6} * 4)\left[\big(-1.1 - (-0.8)\big)(-0.05) - \frac{(-0.05)^2}{2}\right] = 8.25uA$$

2) NMOS: VGS=0.9V, VDS=1.8V -> Saturation
PMOS: VGS=-2.5V, VDS=-1.0V -> Triode/Linear

$$I_{d,nmos} = \frac{(350 * 10^{-6} * 4)}{2}(0.9 - 0.7)^2(1 + 0.05 * 1.8) = 30.5uA$$

$$I_{d,pmos} = (150 * 10^{-6} * 4)\left[\big(-2.5 - (-0.8)\big)(-1.0) - \frac{(-1.0)^2}{2}\right] = 720uA$$

3) NMOS: VGS=1.5V, VDS=0.4V -> Triode/Linear
PMOS: VGS=-1.8V, VDS=-1.6V -> Saturation

$$I_{d,nmos} = (350 * 10^{-6} * 4)\left[(1.5 - 0.7)(0.4) - \frac{0.4^2}{2}\right] = 336uA$$

$$I_{d,pmos} = \frac{(150 * 10^{-6} * 4)}{2}(-1.8 - (-0.8))^2(1 + 0.05 * (-1.6)) = 276uA$$

# 4. CMOS INVERTER

4.1 **Static CMOS, so $V_{OL} = 0, and\ V_{OH} = Vdd$**

$$k_R = \frac{k_n}{k_p} = \frac{\mu_n Cox\left(\frac{W}{L}\right)_n}{\mu_p Cox\left(\frac{W}{L}\right)_p} = \frac{250 \times 8}{100 \times 12} = \frac{5}{3} = 1.66 \ldots 67$$

$$V_M = \frac{V_{th,n} + \sqrt{\frac{1}{k_R}}}{1 + \sqrt{\frac{1}{k_R}}}\left(Vdd + V_{th,p}\right) = \frac{0.3 + 0.77\left(2.5 + (-0.35)\right)}{1 + 0.77} = \mathbf{1.105\ Volts}$$

To find the noise margins, we need $V_{IL}$ *and* $V_{IH}$

$$find\ V_{IL};\ V_{IL} = \frac{2V_{out} + V_{th,p} - Vdd + k_R V_{th,n}}{1 + k_R} = \frac{2V_{out} - 0.35 - 2.5 + 0.531}{2.67}$$

$$= \frac{2V_{out} - 2.319}{2.67}$$

$$\rightarrow V_{out} = 0.749V_{IL} + 0.868$$

*Now, equate the NMOS saturation current and PMOS linear current, we get*

$$\frac{k_n}{2}(V_{IN} - V_{TH,N})^2 = \frac{k_P}{2}\left(2\left(V_{IN} - V_{dd} - V_{TH,P}\right)(V_{OUT} - V_{dd}) - (V_{OUT} - V_{dd})^2\right)$$

*Plug in equation for* $V_{out}$

$$\rightarrow \frac{5}{3}(0.749V_{IL} + 0.568)^2 = 2(0.749V_{IL} - 1.282)(0.749V_{IL} - 1.632) - (0.749V_{IL} - 1.632)^2$$

$$\rightarrow \boldsymbol{V_{IL} = 0.829\ volts}$$

$$find\ \ V_{IH};\ V_{IH} = \frac{V_{dd} + V_{th,p} + k_R(2V_{out+}V_{th,n})}{1 + k_R} = \frac{2.5 - 0.35 + 1.67(2V_{out+}0.3)}{2.67}$$

$$\rightarrow V_{out} = 0.8V_{IH} + 0.494$$

*Now, equate the NMOS linear current and PMOS saturation current, we get*

$$\frac{k_n}{2}\left(2\left(V_{IH} - V_{TH,N}\right)V_{OUT} - {V_{OUT}}^2\right) = \frac{k_P}{2}\left(V_{IH} - V_{dd} - V_{th,p}\right)^2$$

*Plug in equation for* $V_{out}$

$$\frac{5}{3}(2(V_{IH} - 0.3)(0.8V_{IH} + 0.494) - (0.8V_{IH} + 0.494)^2) = (V_{IH} - 2.85)^2$$

$$\rightarrow \boldsymbol{V_{IH} = 1.4757\ volts}$$

$$\boldsymbol{NM_L = V_{IL} - V_{OL} = 0.829V}$$

$$\boldsymbol{NM_H = V_{OH} - V_{IH} = 2.5 - 1.4757 = 1.0243V}$$

4.2

$$1.4 = \frac{0.3 + \sqrt{\frac{1}{k_R}}}{1 + \sqrt{\frac{1}{k_R}}}(2.5 - 0.35)$$

$$1.1 = 0.75\sqrt{\frac{1}{k_R}}$$

$$\rightarrow k_R = \frac{250W_n}{100W_p} = 0.46$$

$$\rightarrow \frac{250W_n}{100W_p} = \frac{46}{100}$$

$$\rightarrow \frac{W_n}{W_p} = \frac{46}{250} = \frac{23}{125}$$

4.3

$$V_{TH,N,max} = 1.15 * 0.3 = 0.345\ Volts$$
$$V_{TH,N,min} = 0.85 * 0.3 = 0.255\ Volts$$

$$V_{TH,P,max} = 1.25 * -0.35 = -0.4375\ Volts$$
$$V_{TH,P,min} = 0.8 * -0.35 = -0.28\ Volts$$

$$V_{M,max} = \frac{V_{TH,N,max} + \sqrt{\frac{1}{k_R}}}{1 + \sqrt{\frac{1}{k_R}}}\left(Vdd + V_{TH,P,min}\right) = \frac{0.345 + \sqrt{\frac{3}{5}}}{1 + \sqrt{\frac{3}{5}}}(2.5 - 0.28) = \mathbf{1.166\ Volts}$$

$$V_{M,min} = \frac{V_{TH,N,min} + \sqrt{\frac{1}{k_R}}}{1 + \sqrt{\frac{1}{k_R}}}\left(Vdd + V_{TH,P,max}\right) = \frac{0.255 + \sqrt{\frac{3}{5}}}{1 + \sqrt{\frac{3}{5}}}(2.5 - 0.4375) = \mathbf{1.041\ Volts}$$

# 5. RING OSCILLATOR

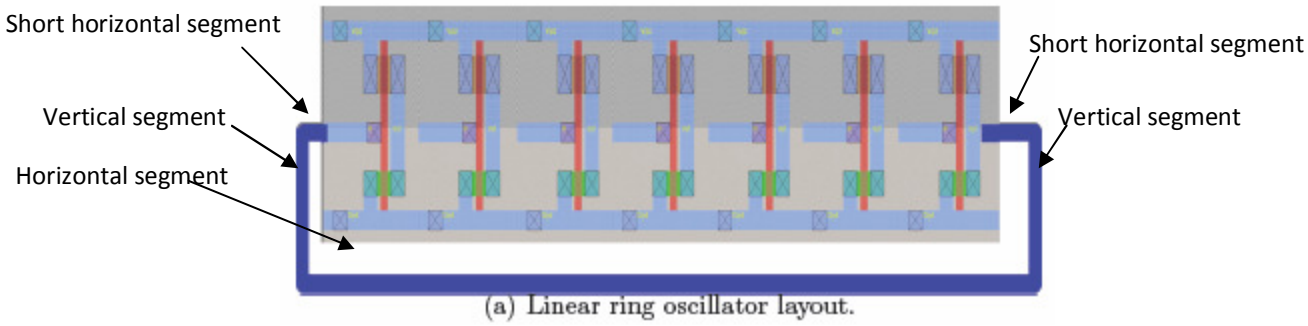
5.1 $AVERAGE\ GATE\ DELAY,\ \tau_{pd,gate} = \frac{T_{waveform}}{2N}$

$where\ T_{waveform}\ is\ the\ period\ of\ the\ observed\ waveform\ and\ N\ is\ the\ number\ of\ gates.$

5.2 $768ps = \frac{T_{waveform}}{2*7} \rightarrow T_{waveform} = 10752ps = 10.752ns;$

$$frequency_{waveform} = \frac{1}{T_{waveform}} \cong 93\ MHz$$

5.3 The delay can be estimated in the three methods below, each method more accurate than previous.



(a) Linear ring oscillator layout.

**Method 1:** $T_{ring\ osc.} = 7 * \tau_{pd,inverter} + 7\ horizontal\ segments * \frac{2um}{segment} * \frac{14ps}{um} = 5376 + 196 = 5572ps;$

$$f_{ring\ osc.} = \frac{1}{2 * T_{ring\ osc.}} = 89.7\ MHz$$

**Method 2:** $T_{ring\ osc.} = 7 * \tau_{pd,inverter} + 7\ horizontal\ segments * \frac{2um}{segment} * \frac{14ps}{um} + 2\ vertical\ segments * 3um * \frac{14ps}{um} = 5376 + 196 + 84 = 5656ps;$

$$f_{ring\ osc.} = \frac{1}{2 * T_{ring\ osc.}} = 88.4\ MHz$$

**Method 3:** $T_{ring\ osc.} = 7 * \tau_{pd,inverter} + 7\ horizontal\ segments * \frac{2um}{segment} * \frac{14ps}{um} + 2\ vertical\ segments * \frac{3um}{segment} * \frac{14ps}{um} + 2\ short\ horizontal\ segments * \frac{1um}{segment} * \frac{14ps}{um} = 5376 + 196 + 84 + 28 = 5684ps;$

$$f_{ring\ osc.} = \frac{1}{2 * T_{ring\ osc.}} = 87.9\ MHz$$

5.4 $T_{ring\ osc.} = 7 * \tau_{pd,inverter} + 3\ horizontal\ segments * \frac{1um}{segment} * \frac{14ps}{um} + 2\ vertical\ segments * \frac{5um}{segment} * \frac{14ps}{um} = 5376 + 42 + 140 = 5558ps;$

$$f_{ring\ osc.} = \frac{1}{2 * T_{ring\ osc.}} = 89.9MHz$$

5.5

Folded: Ring oscillator period = 5558*2=11116ps;

Straight: Ring oscillator period = 5684*2=11368ps;

As we can see, the folded layout gives a more accurate estimate of the true propagation delay. Wire delay in the straight layout is (308*2)/11368=5.4% of the total period, while wire delay in the folded layout is only (182*2)/11116=3.2% of the total period.

Ring oscillator period for the ring oscillator without wires is 10752ps. Percent error for the folded layout is (11116-10752)/10752 = 3.38% while percent error for the straight layout is (11368-10752)/10752 = 5.7%