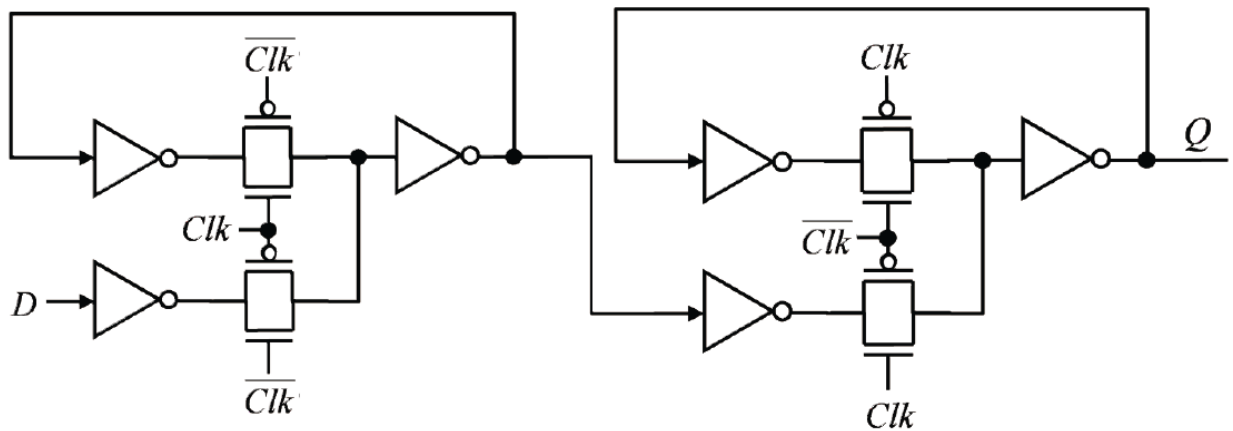# 1. Edge-Triggered Flip-Flop Design

1.1 and 1.2

The schematic of a positive edge-triggered flop-flop is below. The PMOS transistor in the inverters should be sized for equal rise and fall time at the inverter's output. The PMOS transistor in the transmission gates has the same size as the PMOS transistor in the inverters.

To size the inverters, we set the inverter's switching threshold to $\frac{V_{dd}}{2}$ and solve for W_p,

$$V_{th,inverter} = 0.9 = \frac{\left(V_{th,nmos} + \sqrt{\frac{1}{k_R}}\left(V_{dd} + V_{th,pmos}\right)\right)}{1 + \sqrt{\frac{1}{k_R}}} = \frac{0.5 + \sqrt{\frac{1}{k_R}}(1.8 - 0.55)}{1 + \sqrt{\frac{1}{k_R}}}$$

where $\sqrt{\frac{1}{k_R}} = \sqrt{\frac{\mu_p C_{ox}\left(\frac{W_p}{L_p}\right)}{\mu_n C_{ox}\left(\frac{W_n}{L_n}\right)}} = \sqrt{\frac{125\left(\frac{W_p}{180}\right)}{350\left(\frac{450}{180}\right)}} = 0.028\sqrt{W_p}$

$$0.9 = \frac{0.5 + 0.028\sqrt{W_p}(1.8 - 0.55)}{1 + 0.028\sqrt{W_p}}$$

$$0.9 + 0.0252\sqrt{W_p} = 0.5 + 0.028\sqrt{W_p}(1.8 - 0.55) = 0.5 + \sqrt{W_p}0.035$$

$$0.4 = 0.0098\sqrt{W_p}$$

$$W_p = 1665.97 \; nm \rightarrow 1620 \;\; nm \; or \; 1710 \; nm \; (integral \; multiple \; of \; 90nm),$$

$$and \; L_p = L_n = 180 \; nm, and \; W_n = 450 \; nm$$

1.3 The setup time is the time the D-input has to be stable before the active edge so that the D-input can propagate to the input of the slave stage and be held. In this case, the longest possible propagation delay will determine the setup time. Here, we assume $T_{p,HL} = T_{p,LH} = T_p$ because of equal rise and fall times.

$$\frac{W_n}{L_n} = \frac{450}{180} = 2.5$$

$$I_d(Vout = beginning \; of \; transition) = \frac{350\frac{uA}{V^2}}{2} 2.5 \, (1.8 - 0.5)^2 = 739uA$$

$$I_d\left(Vout = \frac{Vdd}{2}\right) = 350\frac{uA}{V^2} 2.5 \left((1.8 - 0.5)0.9 - \frac{0.9^2}{2}\right) = 669.375uA$$

$$I_{d,average} = 704.2uA$$

$$R_{on} = \frac{1}{2}\left(\frac{1.8}{739uA} + \frac{0.9}{669.375uA}\right) = \frac{1}{2}(2436 + 1345) = 1890.5 \; ohms$$

$$R_{eq,transmission \; gate} = \frac{1}{k_n(V_{dd} - V_{th,n}) + k_p(V_{dd} - |V_{th,p}|)}$$

$$= \frac{1}{875 * 10^{-6}(1.8 - 0.5) + 125 * 10^{-6} * \frac{1620}{180}(1.8 - 0.55)}$$

$$= \frac{1}{\frac{1137uA}{V} + \frac{1406.25uA}{V}} = 393.2 \; Ohms$$

Inverter's input capacitance: $= 2*C_g * (0.18 \; um * (1.620 \; um + 0.45 \; um)) = 10.05$ fF

Inverter's output capacitance: $= 2*C_d * (1.620 \; um + 0.45 \; um) = 55.89$ fF

Transmission gate's input capacitance: $= 2*C_s * (1.620 \; um + 0.45 \; um) = 55.89$ fF

Transmission gate's output capacitance: $= 2*C_d * (1.620 \; um + 0.45 \; um) = 55.89$ fF

The setup time is: $T_{su} = 0.69 * (393.2 * (2*55.89 + 10.05) + 1890.5 * (55.89 + 2 * 10.05) + 1890.5*(55.89+55.89)) = 0.69*(48 \text{ ps} + 143 \text{ ps} + 211.3 \text{ ps}) = \underline{\textbf{277 ps}}$

The clock to Q time is the time starting when the clock arrives (low to high transition), to the time output makes a transition.

The clock-q time is: $T_{c-q} = 0.69 * (393.2 * (2*55.89 + 10.05) + 1890.5 * (55.89 + 10.05)) = 0.69*(48 \text{ ps} + 124.6 \text{ ps}) = \underline{\textbf{119 ps}}$