



1.1 Parameters below apply to both source and drain.

Width = $1.5 + 2 + 1.5 = 5 \text{ lambda} = 450 \text{ nm}$

Length = $1.5 + 2 + 2 = 5.5 \text{ lambda} = 495 \text{ nm}$

Perimeter = $1 * \text{width} + 2 * \text{lengths} = 16 \text{ lambda} = 1440 \text{ nm}$

Area = $\text{Width} * \text{Length} = 27.5 \text{ squared lambda} = 222750 \text{ square nm} = 0.22 \text{ square um}$

1.2 PMOS with 3 times the width.

Parameters below apply to both source and drain.

New Width = $5 \text{ lambda} * 3 = 15 \text{ lambda} = 1350 \text{ nm}$

Length = 5.5 lambda – same as before = 495 nm

Perimeter = $1 * \text{New Width} + 2 * \text{lengths} = 26 \text{ lambda} = 2340 \text{ nm}$

Area = $\text{New width} * \text{Length} = 82.5 \text{ squared lambda} = 668250 \text{ square nm} = 0.67 \text{ square um}$

1.3 Doubling the length of a transistor will only change the length of the channel ($2 \text{ lambda} \rightarrow 4 \text{ lambda}$).

All parameters for the source and drain regions calculated in 1.1 and 1.2 above stay the same.