EEC 116 Fall 2011 Midterm

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October 31, 2011

This examination is closed book and closed notes. Some formulas which you may find useful are listed in the back of the exam. Calculators are allowed, however using the calculator's function memory to store course related material is NOT allowed and constitutes cheating on this exam.

For all problems, state any assumptions you make, show all work, and clearly mark your answers. Correct but unclear or ambiguous answers will not receive full credit.

Excerpts from the UC Davis Code of Academic Conduct state:

1. Each student should act with personal honesty at all times.
2. Each student should act with fairness to others in the class. This means, for example, that when taking an examination, students should not seek an unfair advantage over other classmates through cheating or other dishonest behavior.
3. Students should take group as well as individual responsibility for honorable behavior. This includes notifying the instructor or TA if you observe cheating.

I understand the honor code and agree to be bound by it.
Signature:
Name (printed): Solutions
Lab Section:

Grading:

Problem	Maximum	Score
1	15	
2	15	
3	30	
4	28	
5	12	
Total	100	

1 Transistor Biasing

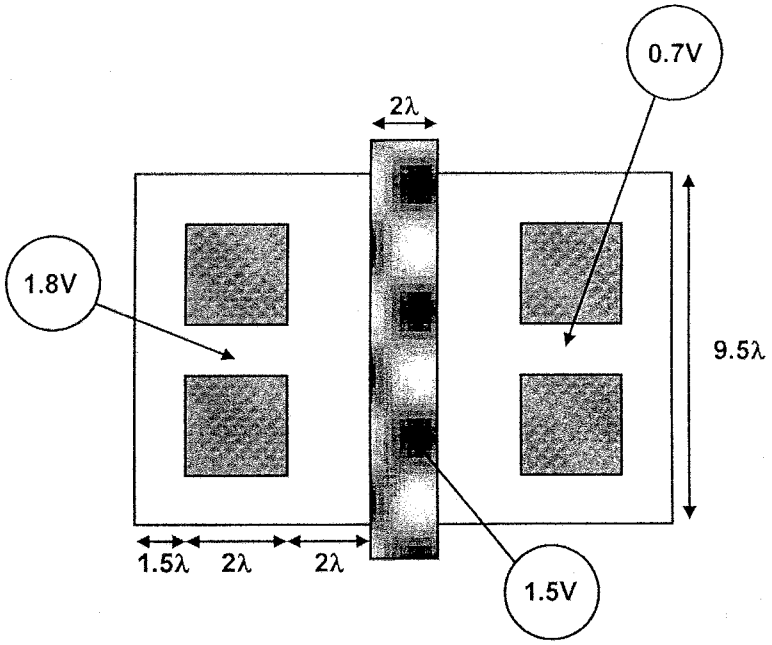
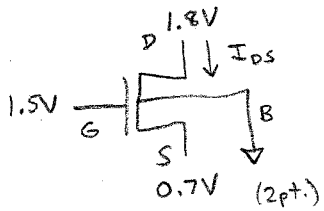


Figure 1: FET layout with bias voltages indicated.

Problem 1.1 (10 points) Consider the NMOS transistor layout and voltage biases shown in Figure 1. Suppose we know that for the NMOS under bias, $V_{T0,n} = 0.3$V, minimum feature size $2\lambda = 2 \times 90$nm, $\gamma = 0.27\text{V}^{1/2}$, channel length modulation factor $\lambda = 0\ \text{V}^{-1}$, $\mu C_{ox} = 299\ \mu\text{A/V}^2$, and $-2\Phi_F = 0.6$ V. Assume the bulk node of the transistor is at 0V. Find the drain-source current I_{DS}.

$V_G = 1.5V$ $V_D = 1.8V$ $V_S = 0.7V$ $V_B = 0V$



(2pt.)

$V_{SB} = 0.7V$ (1pt.)

$V_{Tn} = V_{Tn\phi} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$

$= 0.3V + (0.27\ V^{1/2})\left(\sqrt{|0.6V + 0.7V|} - \sqrt{0.6V}\right)$ (1pt.)

$= 0.3987\ V \approx 0.4V$ (1pt.)

$V_{GS} = 0.8V > V_{T,n} = 0.4V$ (1pt.)

$V_{DS} = 1.8V - 0.7V = 1.1\ V > V_{GS} - V_{Tn} = 0.4\ V$

sat (1pt.)

$I_{DS,n} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{T,n})^2(1 + \lambda V_{DS})$ (2pt.)

$= \frac{299\ \mu A/V^2}{2}\left(\frac{9.5}{2}\right)(0.8V - 0.4V)^2$ (1pt.)

$= 114.4\ \mu A$

$= \boxed{114\ \mu A}$ (1pt.)

Problem 1.2 (**5 points** Compute the total source/drain junction capacitance assuming a bottom junction capacitance per unit area of $C_{jB} = 17\text{fF}/\mu\text{m}^2$ and a sidewall (perimeter) junction capacitance per unit length of $C_{jSW} = 11\text{fF}/\mu\text{m}$. Assume C_{jB} and C_{jSW} are independent of voltage.)

$C_{SB} = C_{DB} = C_T = A C_{jB} + A_{SW} C_{jSW}$ (2 pt.)

$= (1.5+2+2)(9.5)(0.09\mu m)^2 (17 fF/\mu m^2)$ (1 pt.)

$+ (9.5+2(1.5+2+2))(0.09\mu m)(11 fF/\mu m)$ (1 pt.)

$= \boxed{27.5\ fF}$ (1 pt.)

2 Logic Gate

Figure 2 shows a circuit model for a one input CMOS logic gate. Assume all transistor W/L ratios are as shown in Figure 2 and the following transistor and supply voltage characteristics:

$V_{DD} = 5$ V

$\lambda_n = 0.02$ V^{-1}	$\lambda_p = -0.02$ V^{-1}
$V_{T0,n} = 0.8$ V	$V_{T0,p} = -0.8$ V
$\gamma_n = 0.33$ V$^{1/2}$	$\gamma_p = 0.33$ V$^{1/2}$
$\mu_n C_{ox} = 350 \times 10^{-6}$ A/V^2	$\mu_p C_{ox} = 100 \times 10^{-6}$ A/V^2
$W_{min} = 2$	$L_{min} = 1$

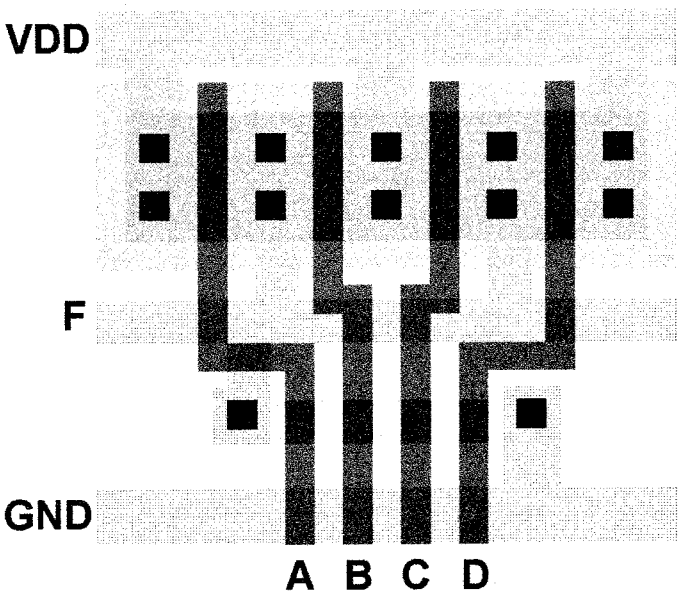
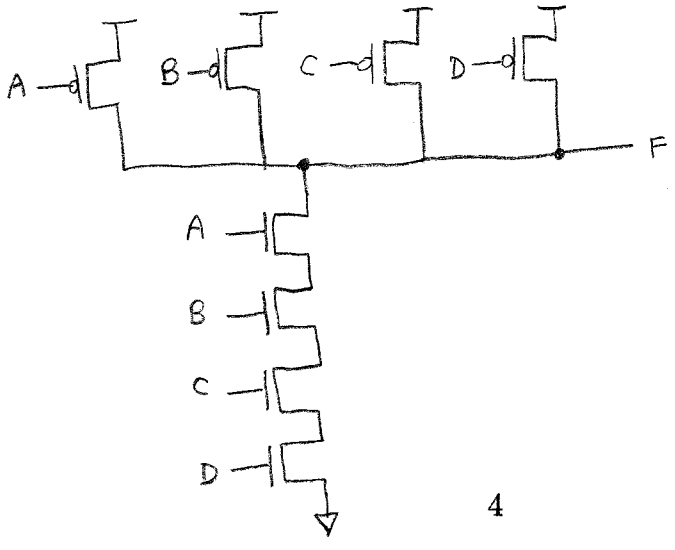


Figure 2: Layout for a logic gate.

Problem 2.1 (5 points) Draw a transistor-level circuit schematic which corresponds to the layout shown in Figure 2.



Problem 2.2 (2 points) What Boolean logic function is implemented by the circuit in Figure 2?

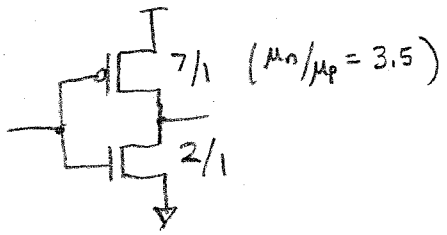
$F = \overline{A \cdot B \cdot C \cdot D}$

Problem 2.3 (6 points) Assuming all PMOS and NMOS transistors are the same width, find W_P and W_N such that the **worst case** rise and fall times of the circuit in Figure 2 are equal to a minimum-sized inverter. Be sure to minimize the total transistor area. Justify your answers below.

(1 pt. value, 2 pt. explain)

- $W_P =$ 7 (worst case same as min. inverter)
- $W_N =$ 8 (equivalent inverter has 4 NMOS in series, so need 4x width)

min. inverter



Problem 2.4 (2 points) Given your sizes from Problem 2.3 above, what are V_{OH} and V_{OL} for the circuit in Figure 2? Justify your answers.

- $V_{OH} =$ V_{DD} = 5V (1pt.)
- $V_{OL} =$ 0V (1pt.)

3 Static CMOS Logic Design

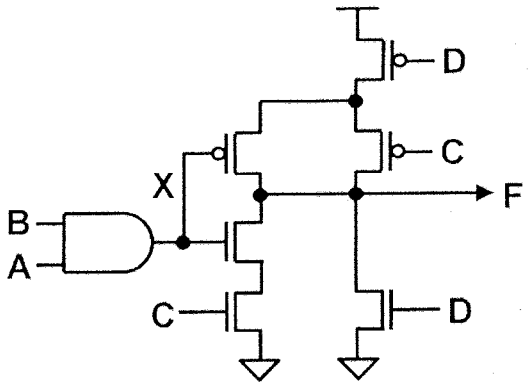


Figure 3: Logic gate network.

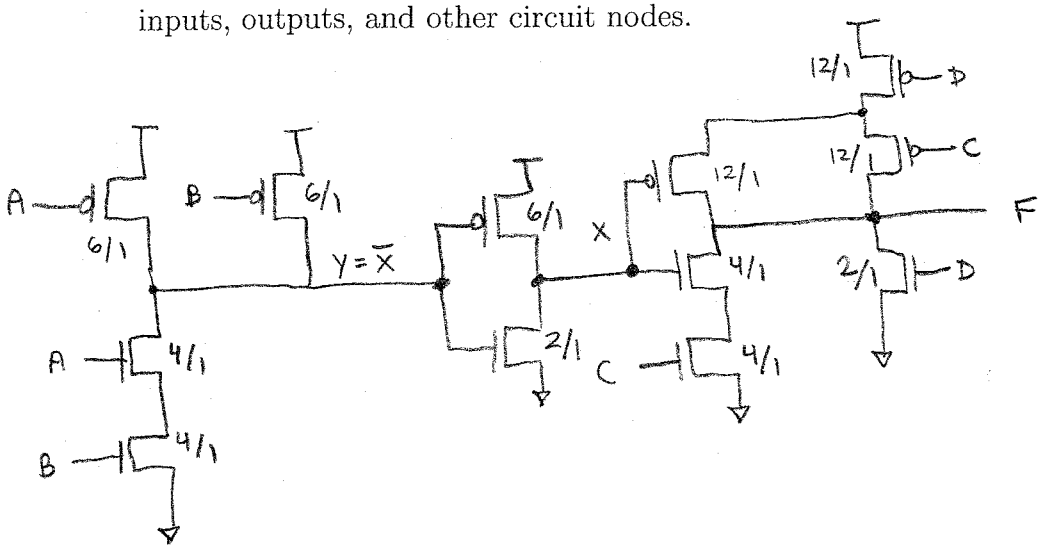
Problem 3.1 (2 points) Write a Boolean expression for the logic function F in terms of inputs A, B, C, and D implemented by the logic gate network in Figure 3.

$X = A \cdot B$

$F = \overline{D + X \cdot C} = \overline{D + A \cdot B \cdot C}$

Problem 3.2 (~~12~~ 10 points) Draw a transistor-level schematic for the circuit in Figure 3 using static CMOS circuits for any logic gates represented by a logic symbol. Be sure to label all inputs, outputs, and other circuit nodes.

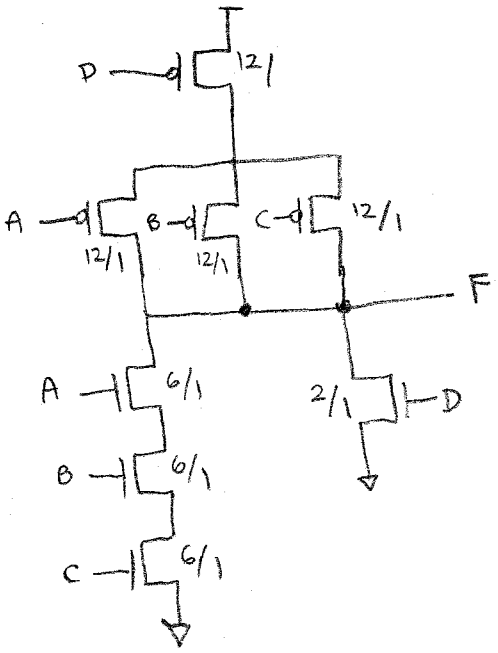
0.5 pt / transistor
6 pts labels



Problem 3.3 (**6 points**) Assume a minimum-sized inverter has PMOS ratio $W_P/L = 6/1$ and NMOS ratio $W_N/L = 2/1$. Choose appropriate W/L ratios for the transistors in your circuit of Problem 3.2 such that the worst case rise and fall times at any logic gate output are the same as a minimum-sized inverter. Indicate the sizes in your schematic above. Be sure to minimize the total area of the transistors. (0.5pt/size)

Problem 3.4 (**8 points**) Replace the multiple-gate logic network of Figure 3 with a circuit that implements F which consists of a single multiple input CMOS logic gate.

(0.5pt/transistor)
(0.5pt/label)



other solutions possible...

Problem 3.5 (**4 points**) Choose appropriate W/L ratios for the transistors in your circuit of Problem 3.4 such that the worst case rise and fall times are the same as the minimum-sized inverter in Problem 3.3. Indicate the sizes in your schematic above. Be sure to minimize the total area of the transistors. (0.5pt/size)

4 Adder Design

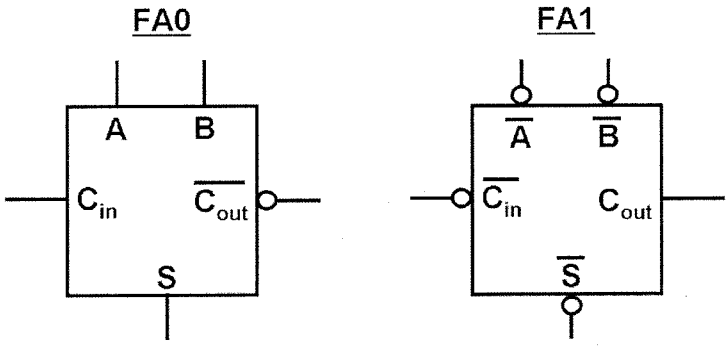
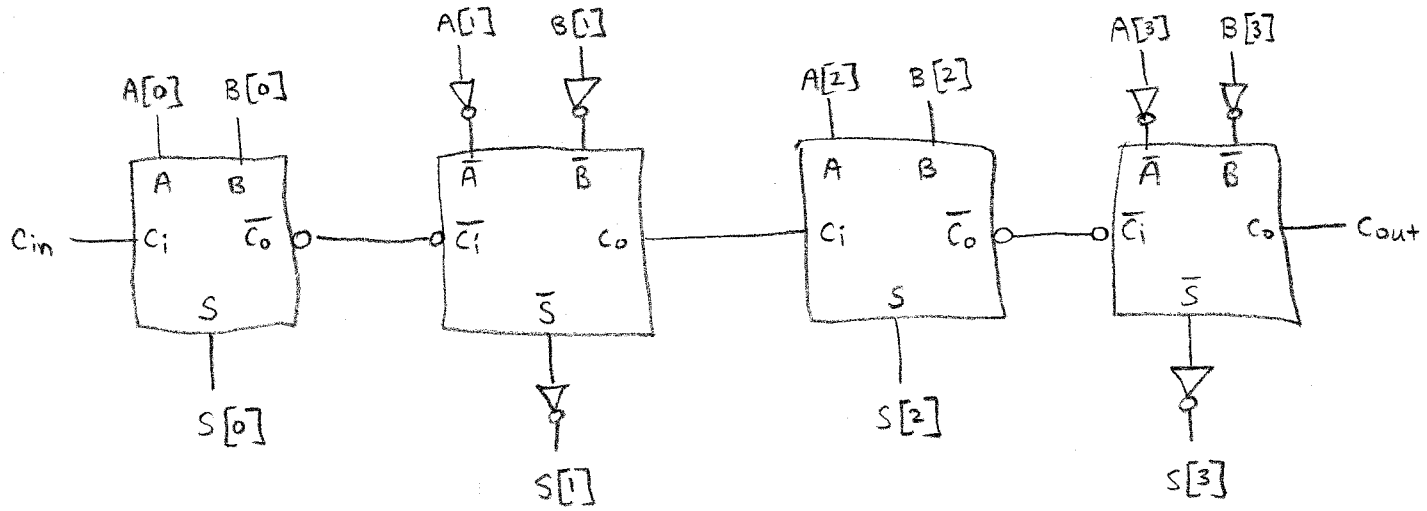


Figure 4: Full adder cells.

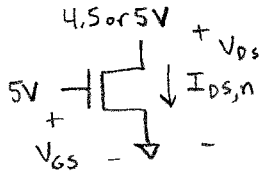
Problem 4.1 (17 points) Design a **fast** 4 bit ripple-carry adder using the two full adder cells shown in Figure 4 and CMOS inverters. Label the inputs $A[3:0]$, $B[3:0]$, C_{in} and the outputs $S[3:0]$ and C_{out}. Assume the delay through an inverter $t_{INV} = 4$ps, the delay from any input to the full adder carry output is $t_{Co} = 7$ps and to the sum output is $t_S = 10$ps. What is the worst case delay through the adder for your design?

- Worst Case Delay = $3t_{Co} + t_S + t_{INV} = 21 + 10 + 4 =$ **35 ps** (2 pts.)



10 pts circuit
5 pts. labels

Problem 4.2 (7 points) Suppose the equivalent inverter resistance for the NMOS device is $R_n = 12\text{k}\Omega$ in the carry out path of the full adder and was measured by measuring the resistance at the beginning of a **worst case fall time** measurement. Find the W/L of the equivalent NMOS device given $V_{DD} = 5$ V, $V_{T0,n} = 1.0$ V, $\mu_n C_{ox} = 300 \times 10^{-6}$ A/V^2, $\gamma_n = 0.0$ V$^{1/2}$, $\lambda_n = 0.0$ V^{-1}.



$R_n = \dfrac{V_{DS}}{I_{DS,n}}$

$I_{DS,n} = \dfrac{\mu_n C_{ox}}{2}\left(\dfrac{W}{L}\right)(V_{GS} - V_{T\phi,n})^2(1 + \lambda \cancel{V_{DS}}^{\,0})$ (2pt.)

$V_{DS} = V_{GS} > V_{T\phi,n}$

sat (1pt.)

$$R_n = \frac{V_{DS}}{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{T\phi n})^2} \quad \text{(2pt.)}$$

$$\Rightarrow \left(\frac{W}{L}\right) = \frac{V_{DS}/R_n}{\frac{\mu_n C_{ox}}{2}(V_{GS} - V_{T\phi n})^2} = \frac{5\text{V}/12\text{k}\Omega}{\frac{300\mu\text{A/V}^2}{2}(5\text{V} - 1\text{V})^2} = \frac{25}{144} = \boxed{0.174} \quad \text{(1pt.)}$$

(1pt.)

$$= \frac{4.5\text{V}/12\text{k}\Omega}{\frac{300\mu\text{A/V}^2}{2}(5\text{V} - 1\text{V})^2} = \boxed{0.156}$$

Problem 4.3 (2 points) Assuming the resistance for the equivalent inverter NMOS device is $R_n = 12\text{k}\Omega$ as in Problem 4.2 and $t_{Co} = 7$ps as in Problem 4.1, what is the capacitance at the carry output assuming a switch-RC model for the delay?

$$t_{co} = 0.69 R_n C_o \Rightarrow C_o = \frac{t_{co}}{0.69 R_n} = \frac{7\text{ps}}{(0.69)(12\text{k}\Omega)} = \boxed{0.845\text{ fF}} \quad \text{(1pt.)}$$

(1pt.)

Problem 4.4 (2 points) Suppose the adder has a total capacitance of 89fF, $V_{DD} = 5$V, and is operated at 1GHz. What is the adder's dynamic power dissipation?

$$P = CV_{DD}^2 f = (89\text{fF})(5\text{V})^2(1\text{GHz}) = \boxed{2.23\text{ mW}} \quad \text{(1pt.)}$$

(1pt.)

or

$$= \alpha CV_{DD}^2 f = (1/2)(89\text{fF})(5\text{V})^2(1\text{GHz}) = \boxed{1.1125\text{ mW}}$$

5 Latch

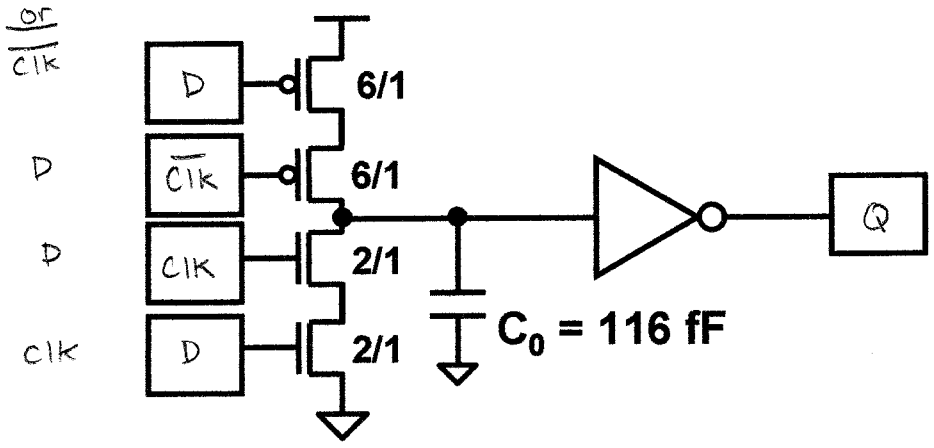


Figure 5: Latch schematic.

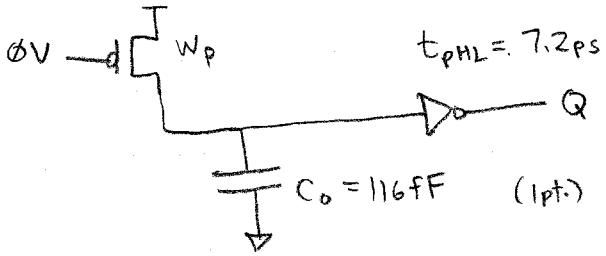
Problem 5.1 (5 points) For the latch circuit shown in Figure 5, label the boxes D, CLK, $\overline{CLK}$, Q such that the circuit works as a **positive transparent** noninverting latch.

Problem 5.2 (2 points) Is the circuit in Figure 5 a static or dynamic latch (circle one)? Justify your answer.

- Static
- Dynamic — No positive feedback, data stored on C_ϕ

Problem 5.3 (5 points) Suppose the latch is used as the slave stage of an edge-triggered flip-flop and that capacitor C_0 in Figure 5 is initially at 0V. Assuming R_p = 2.9kΩ for a PMOS device with W/L = 1/1 and R_n = 0.8kΩ for an NMOS device with W/L = 1/1, and t_{pHL} for the inverter is 7.2ps, estimate the clock-to-Q delay assuming the data input is steady for the latch using the switch RC model for the transistors.

Problem 5.3 (cont.)



$$t_{CQ} = t_{pLH}(C^2MOS) + t_{pHL}(INV) \quad (2pt.)$$
$$= (0.69)(R_p)(C_o) + 7.2ps$$
$$= (0.69)(R_p)(116fF) + 7.2ps \quad (1pt.)$$

if $R_p = \frac{2\,(2.9K\Omega)}{6/1}$, then $t_{CQ} = \boxed{84.6\ ps}$ (two PMOS model) (1pt.)

if $R_p = \frac{2.9K\Omega}{6/1}$, then $t_{CQ} = \boxed{45.9ps}$ (one PMOS, virtual V_{DD} model) (1pt.)