EEC 116 Fall 2011 Prelab #1

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Reading: Rabaey Chapters 1, 2, A, 5, Section 6.2.1 [1].
Reference: Brunvand Chapters 1-3 [2].

1 CMOS Inverter Sizes

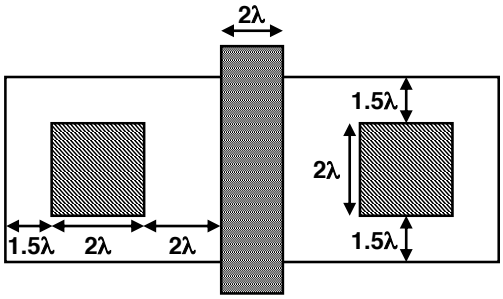

Figure 1: NMOS minimum-sized transistor layout.

Sizing: In any VLSI design, the dimensions of transistors are generally constrained to be integer multiples of a minimum unit dimension. Wire dimensions are also constrained, although they may be referenced to a different minimum unit. For EEC 116, the layout contraints are simplified such that all dimensions, for both wires and transistors, are constrained to the same unit dimension. All transistor sizes (widths and lengths) must be in **integer** numbers of the minimum dimension $\lambda = 90$nm. The minimum transisor length is 2λ. Figure 1 shows the layout for a minimum-sized NMOS device for computing the width, source/drain area, and source/drain perimeter, based on the DEEP submicron rules for scalable CMOS supplied by the MOSIS foundry service. Note that 5λ is the minimum width allowed by our design style - narrower devices have unreliable characteristics due to excessive manufacturing variations. If you need a W/L ratio smaller than 5/2, you can use a greater than minimum channel length for the transistor.

Problem 1.1 NMOS Dimensions (6 points). Compute the width, length, and areas and perimeters for the source and drain junctions for the NMOS transistor shown in Figure 1 (six dimensions total) assuming λ as above. Think carefully about how to compute the perimeters in particular.

Problem 1.2 PMOS Dimensions (6 points). In Static Complementary CMOS design, the PMOS transistors are typically wider than the NMOS devices by the ratio of the electron mobility to the hole mobility. This equalizes their active current flow. Compute the width, length, and areas and perimeters for the source and drain junctions for a PMOS transistor whose width is three times the width of the NMOS device above and whose gate length is the same (six dimensions total), assuming λ as above.

Problem 1.3 Nonminimum Length (3 points). If you were to double the length of the transistors above, which of the dimensions you computed would change? You don't need to recompute the values, just list which ones. You want to make sure you understand how the device physical design changes as you adjust size parameters before you begin the layout in the lab.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] E. Brunvand, *Digital VLSI Chip Design with Cadence and Synopsys CAD Tools*, 1st ed. San Francisco: Addison-Wesley, Inc., 2010.