EEC 116 Fall 2011 Lab #2:
Analog Simulation Tutorial

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Reading: Rabaey Chapters 1, 5, Section 6.2 [1].
Reference: Kang and Leblebici Chapters 1, 6, 7.3-4 [2], Brunvand Chapters 1-3 [3].

1 OBJECTIVE

The objective of this lab is to create a test bench schematic and verify your standard cells developed in Lab 1 using an analog circuit simulator.

2 TOOL SETUP

No additional setup should be required for this lab.

3 TESTBENCH SCHEMATIC AND SIMULATION

Just as you need an infrastructure to test circuits in the lab (a bench, test equipment such as multimeters and oscilloscopes, probes, etc.), you need to create an infrastructure in simulation to verify your circuit design. This can be done using a circuit schematic, as in this part of the lab, or using code, as in the second part.

Part 1 Inverter Voltage Transfer Characteristic Create a new schematic cell view using the Library Manager for a new cell called `lab2pt1_tb`. In this schematic, you will instantiate your *devices under test*, or *DUTs*, as well as additional components for testing them. The first task is to simulate the voltage transfer characteristic (VTC) for an inverter. Add a DC voltage source (`vdc`) and a piecewise linear (PWL) voltage source (`vpwl`). Edit their properties (select the component and invoke Edit→Properties→Objects... from the menu or use the "q" hotkey). Set the DC Voltage property on the `vdc` component to 1.8. This source will generate the power supply for your DUTs. Connect its negative terminal to a `gnd` component and its positive terminal to a `vdd` component. For the PWL source, fill

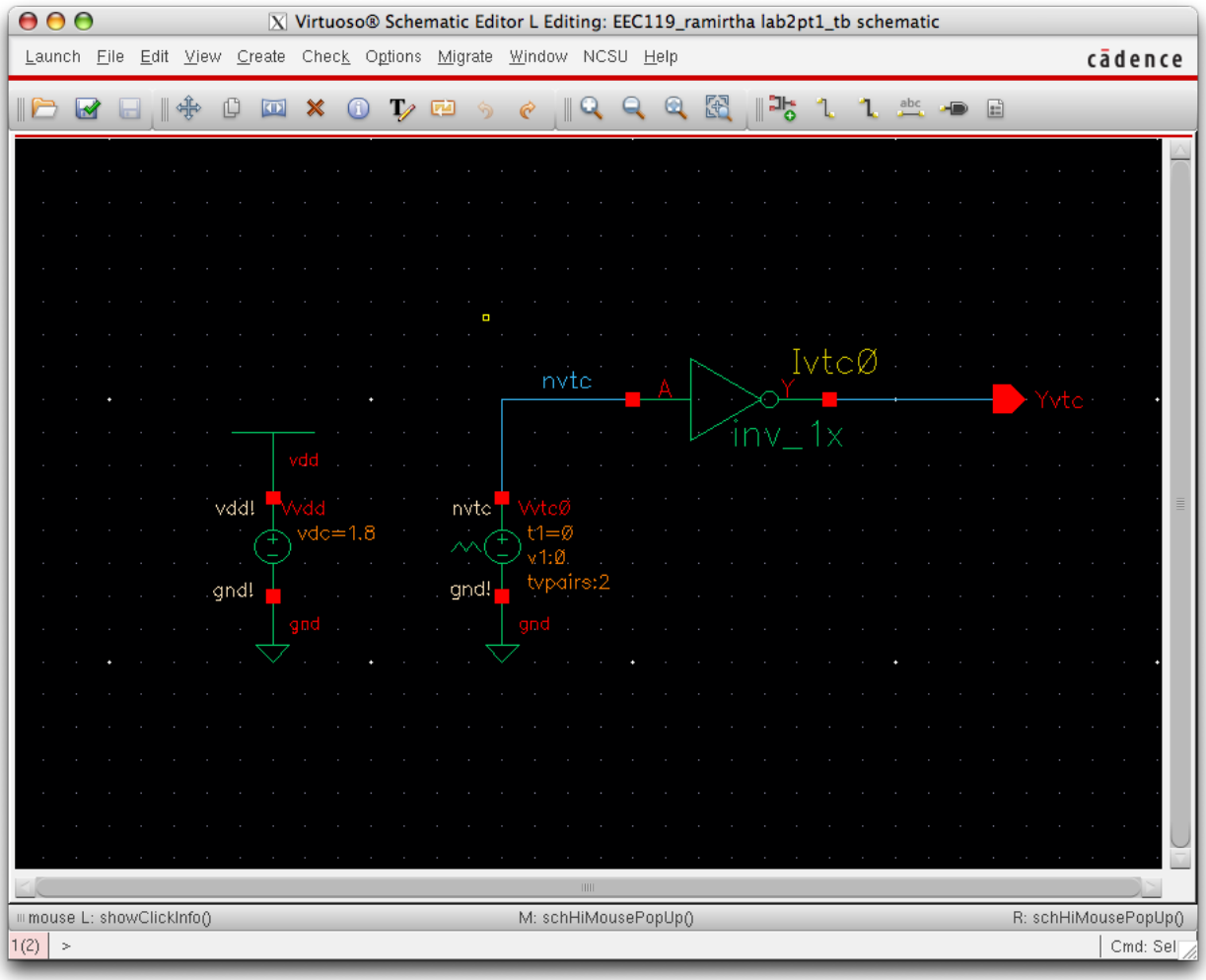


Figure 1: Inverter voltage transfer characteristic testbench schematic.

in 0 for the Time 1 and Voltage 1 properties and 100n (for 100ns) and 1.8 for the Time 2 and Voltage 2 properties, respectively. This should create a linear voltage ramp vs. time to apply to the input of your inverter. If you ever need more pairs of points for a more complex PWL waveform, you can change the Number of pairs of points property to a different desired value. Complete the schematic as shown in Figure 1. Be sure to label any wires to make debugging easier. Check and save your schematic and correct any errors.

Next, Choose Launch→ADE L. A What's New window may pop up (close it) along with the Virtuoso **Analog Design Environment** or **ADE** window. This window is the GUI to controlling the analog simulation tool (Spectre) which we will use in this lab. Spectre is similar to SPICE and other transistor-level analog circuit simulators, although its syntax and other features are slightly different. If you look in the CIW, you may see various warnings about licenses - ignore them. They should not interfere with this lab. In the ADE window, choose Setup→Simulator/Directory/Host... and fill in the Project Directory field with `/project/<username>/simulation`. This will cause the simulator to write all its data to that directory. Hit OK. In the Linux shell, `cd` to that directory and you should see a subdirectory named `lab2pt1_tb`. Look around in the directory tree to familiarize yourself with the locations where ADE will write its data.

Choose Setup→Model Libraries... Fill in the model file or navigate to

`/project/ncsu-cdk-1.6.0.beta/models/spectre/PTM/PTM180nm_bulk.scs`

We are using the freeware models from the Predictive Technology Model Group [4, 5]. Click through the rest of the menus under the Setup tab to get an idea of all the parameters that can be controlled when setting up a simulation (for example, check that the temperature is set to a reasonable value like 27°C). Next, go to Analysis→Choose to configure the type of simulation to be done. Turn on transient analysis (`tran`) in the Choosing Analyses popup window and enter 100n in the Stop Time field. Choose conservative for Accuracy Defaults. It is usually a good idea to run the simulation as conservatively as possible unless it is too slow - this guarantees that you will have the most accurate results that time affords. Many other options can be set which you can find by following the Options... popup.

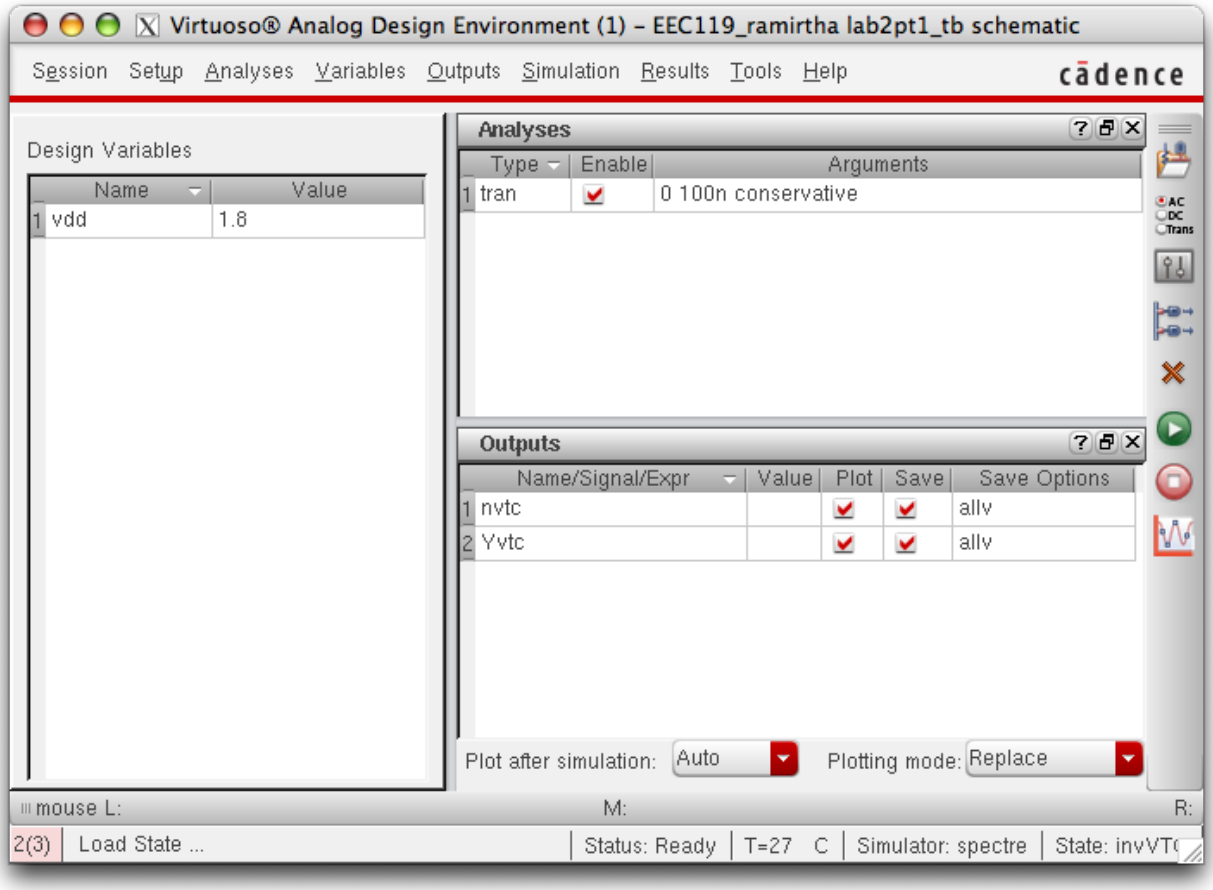


Figure 2: Analog Design Environment window.

In the ADE window, go to Outputs→To be plotted→Select on schematic... and click on the input and output wires of your inverter. Hit Esc to get out of the output selection mode. You should now have an ADE window which looks like Figure 2 (ignore the Design Variables frame for now). Click the Save boxes under the Outputs frame to save your results. Next, choose Simulation→Netlist and Run from the menu or click on the green play button to start the simulation. The simulation requires two steps. First, a *netlist* is created by translating the circuit schematic to a text file written in Spectre syntax. Second, ADE launches the Spectre program to simulate the circuit. A window should pop up displaying the simulator

output log followed by a second which looks a little like an oscilloscope window that shows the signal waveforms versus time. Print the waveform plot to turn in. Also, measure the key points on the curve such as V_{OH}, V_{OL}, V_{IH}, V_{IL}, and the inverter switching threshold V_M. Calculate the noise margins as well. Use tools under the Marker menu tab or the waveform calculator (the calculator icon in the toolbar) to measure these points. Record your answers in Table 3 attached to this lab handout.

Design Variables Sometimes it is useful to store particular commonly used constants or parameters in design variables, for example the power supply voltage of 1.8 in this simulation. In the ADE window, go to Variables→Edit... and create a variable with Name `vdd` and Value 1.8. Click OK. Then, edit the properties of your voltage sources to include the variable name. Check and save your schematic. Re-netlist and re-run the simulation to confirm that everything works as expected.

Saving Simulation State Setting up all the simulation options every time you want to run a test is not efficient. You can save your ADE setup by choosing Session→Save State... in the ADE window menu. Change the directory field to `/project/<username>/.artist_states` and choose a meaningful name for the state in the Save As field. The next time you launch ADE for this cell, load that state to initialize the simulator GUI with your settings.

Part 2 Ring Oscillators Ring oscillators made up of inverters or other gates are a common test structure used to characterize a process for things like gate delay. Edit your `lab2pt1_tb` cell schematic to instantiate a fanout-of-4 (FO4) 11-stage ring oscillator as shown in Figure 3. Note that there are several inverters whose outputs are floating. These inverters are there to present a standard load which has been empirically determined to be typical of logic gates in many integrated circuits. A simple way to implement this load is to use a *vector* of instances (sometimes called *iterated*) instances. Editing the Instance Name property of the inverter to include the syntax `<yy:xx>` will create a number of copies of that cell when the circuit netlist is created. In this way, a schematic can be made less cluttered while still capturing all the testbench information for simulation. In order to avoid floating output warnings, `noConn` cells were added to the outputs of the load inverters so that the schematic checker knows the outputs were intentionally left disconnected. The `noConn` instances have to be vectors as well to avoid connectivity warnings.

A ring oscillator has positive feedback and such circuits sometimes give simulators difficulties, especially when the initial state of the circuit nodes must be determined at the beginning of a transient simulation. To help this process, known as *convergence*, you can set some circuit nodes to specific voltages at time $t = 0$ns. In the ADE window, choose Simulation→Convergence Aids→Initial Condition... In the popup, leave the Node Voltage field at 0 and click *one* of the nodes in the ring oscillator schematic. You should see the node in the popup and also see it labeled with a "0" in the schematic. Hit Esc to get out of the initial condition mode. Select one or two of the ring oscillator nodes to be plotted and run the simulation again.

Plot the ring oscillator waveforms in a strip chart format and hand it in with your lab report. Also, measure and report the 10-90% rise and fall times and the propagation delay

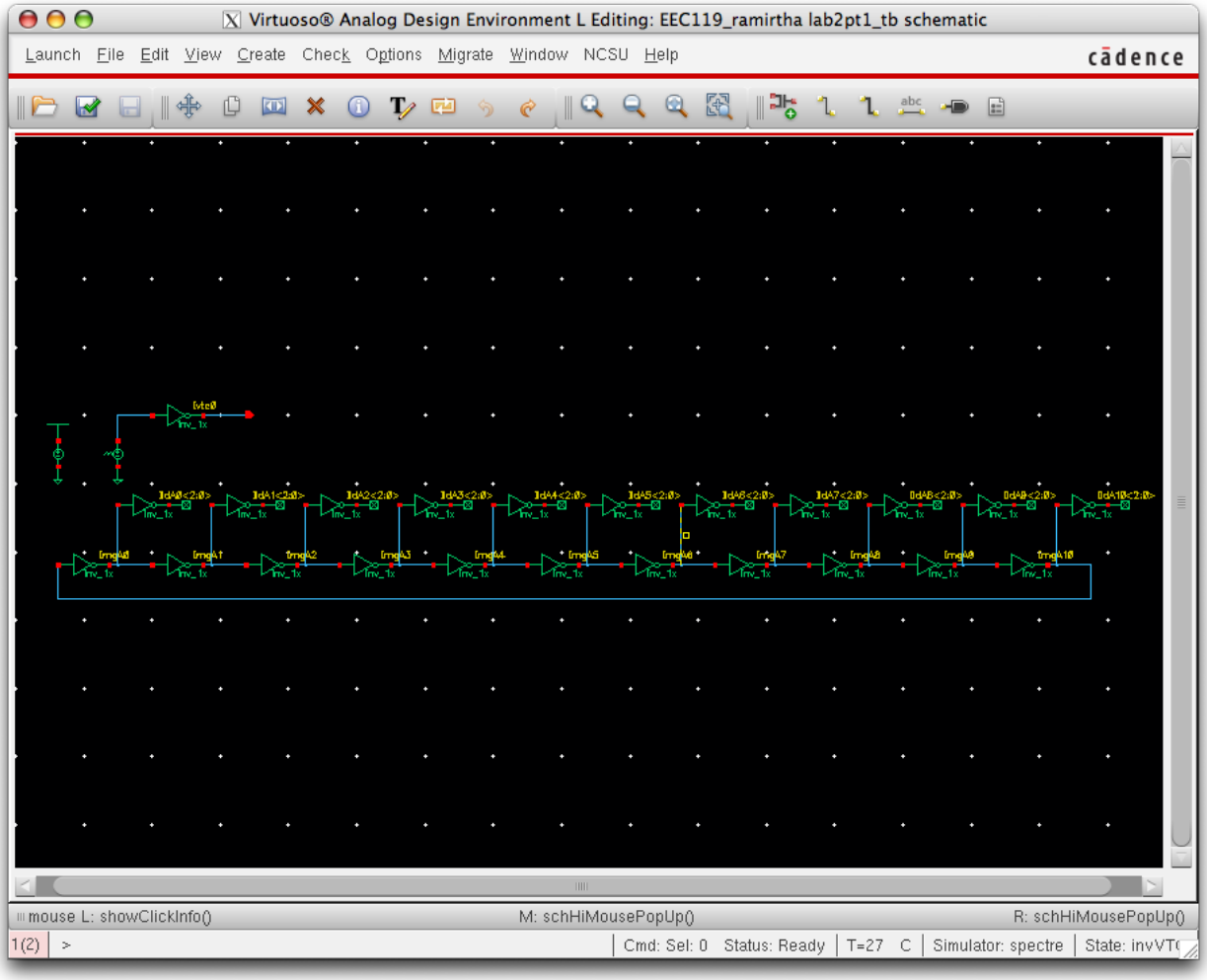


Figure 3: Inverter ring oscillator testbench schematic.

(t_{PD}) through a single inverter. Document how the ring oscillator period is related to the propagation delay in your report.

Create 11-stage ring oscillators for both the NAND and NOR gates you designed in Lab 1. You can neglect the FO4 load and simply tie both inputs of the gates to the output of the preceding gate. Your final schematic should look like Figure 4. You can download a picture of the final schematic (`ThreeRingOscillatorSchematic.png`) from the class SmartSite if you want to zoom in and see more details. Be sure to set initial conditions on the other two oscillators to ensure that convergence occurs quickly. Plot the ring oscillator waveforms in a strip chart format and hand it in with your lab report. Also, measure and report the 10-90% rise and fall times and the propagation delay (t_{PD}) through a single NAND and NOR gate.

Part 3 Simulating with Extracted Parasitics So far we have been using somewhat idealized circuits. However, any physical realization of a logic gate is likely to include extra *parasitic* effects which will degrade performance. The most important of these is the additional capacitance presented by wires and transistor junctions. These capacitances can only be accurately quantified after layout. To generate a cell view which can be used to simulate these parasitic effects accurately, you need to run extraction on your layout. Open the `layout` view for your inverter cell. Choose Verify→Extract... Select Set Switches and choose

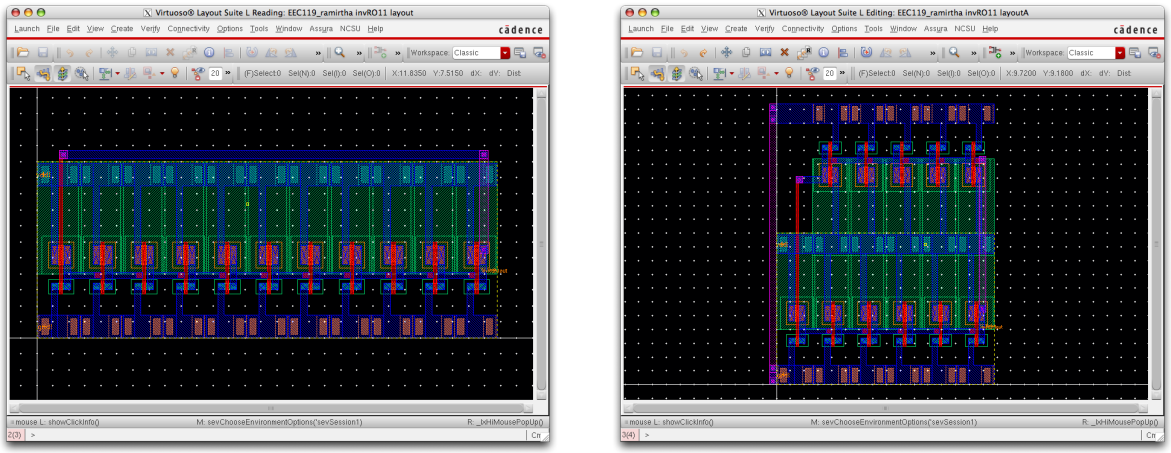
Figure 4: Three ring oscillator testbench schematic.

`Extract_parasitic_caps` and `Keep_labels_in_extracted_view`. Open the `extracted` cell view and you should see (although it may be difficult because of clutter) some capacitors as well as transistors along with the extracted layout geometry. In the ADE window, invoke Setup→Environment... and edit the Switch View List field to add `extracted` as the first element in the list of views. This tells the netlister to look for an extracted view first to generate a netlist for a given circuit. Click OK. Re-netlist and re-simulate your ring oscillator schematic. You should find the delay of the inverter has changed slightly due to more accurate parasitic capacitance. Repeat the extraction and simulation for the NAND and NOR circuits and record the new delays for those gates as well.

Part 4 Simulating Hierarchy with Extracted Parasitics In Part 3, you simulated ring oscillators with parasitic capacitances extracted for the individual logic gates. In this part, you will lay out a ring oscillator to gauge the impact of the wiring on the period of the oscillator. Create a schematic cell view named `invRO11` and place a ring oscillator with 11 inverter stages. You do **not** need to include the FO4 loads. Create two layout views for the oscillator (you can copy the cell to another cell with a different name). One layout should have all the inverters in a single row as shown in Figure 5(a). The second should have all the inverters placed in two rows as in Figure 5(b). Verify both layouts. Simulate the schematic and both layouts with extracted capacitive parasitics and record the average propagation delay for the inverter in Table 3.

Checkoff

Show your final completed schematic and all waveform plots to the TA for checkoff.



(a) Single row. (b) Double row.

Figure 5: Eleven-stage inverter ring oscillator layout alternatives.

Report

You must hand in a **typewritten** report to receive credit for this lab. Your report can be brief, but must include the following sections in addition to the completed summary sheet attached at the end of this lab. The summary sheet will be the cover page of your lab.

1. Overview: Describe in one paragraph the objectives of the lab. State what you were testing and what data you expected to gather as a result of your experiments.

2. Procedure: Briefly document your methodology for acquiring the data you describe in the Overview. Mention how you measured the points on the transfer characteristic, the delay of the cells, rise and fall times, etc. Write a mathematical expression for relating the ring oscillator period to the individual gate delay. Someone reading this section should be able to easily duplicate your results by following the methodology described in this section.

3. Results and Discussion: Describe succinctly the results captured in the completed summary sheet tables. Do the results make intuitive sense? If not, explain why they might contradict your intuition.

Acknowledgments

Parts of this lab were inspired by lab exercises developed by Prof. David Money Harris and others at Harvey Mudd College for the class E158: Introduction to CMOS VLSI Design.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.

[3] E. Brunvand, *Digital VLSI Chip Design with Cadence and Synopsys CAD Tools*, 1st ed. San Francisco: Addison-Wesley, Inc., 2010.

[4] Nanoscale Integration and Modeling (NIMO) Group, Arizona State University. (2006, December) Predictive technology model (ptm). latest.html. [Online]. Available: http://www.eas.asu.edu/ ptm/

[5] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45 nm early design exploration," *IEEE Trans. Electron Devices*, vol. 53, no. 11, pp. 2816–23, November 2006.

EEC 116 Fall 2011 Lab #2 Summary

Name:

Grading:

Part	Checkoff	TA Initials	Date
1 Inverter VTC Plot			
2 Inverter Ring Oscillator Waveform Plot			
2 NAND Gate Ring Oscillator Waveform Plot			
2 NOR Gate Ring Oscillator Waveform Plot			
2 Three Ring Oscillator Testbench Schematic			
2 `invRO11` Schematic			
2 `invRO11` Layout (one row)			
2 `invRO11` DRC (one row)			
2 `invRO11` LVS (one row)			
2 `invRO11` Layout (two rows)			
2 `invRO11` DRC (two rows)			
2 `invRO11` LVS (two rows)			

Inverter Voltage Transfer Characteristic:

Parameter	Value
V_{OL}(V)	
V_{OH}(V)	
V_{IL}(V)	
V_{IH}(V)	
V_M(V)	
NM_L(V)	
NM_H(V)	

Gate Delay Characteristics:

Parameter	Inverter (FO4)	NAND	NOR
t_r(ps)			
t_f(ps)			
t_{pd}(ps)			
t_{pd}(ps) extracted			

Eleven Stage Ring Oscillator Delay Characteristics:

Parameter	Inverter
t_{pd}(ps) (schematic)	
t_{pd}(ps) (one row layout)	
t_{pd}(ps) (two row layout)	