EEC 116 Fall 2011 Homework #5

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Reading: Rabaey Chapters 4 and 9 [1].
Reference: Kang and Leblebici Sections 6.5 and 6.6 [2].

For **all** problems in this homework assignment, assume we are using enhancement-type NMOS and PMOS transistors which have the characteristics shown in Table 1, unless otherwise specified. Also, assume **minimum** length devices unless otherwise specified.

Parameter	NMOS	PMOS
V_{T0}	0.6 V	-0.6 V
μC_{ox}	300 μA/V^2	150 μA/V^2
γ	0	0
L_{min}	0.250μm	0.250μm
λ	0.0 V^{-1}	0.0 V^{-1}
V_{DD}	2.5 V	

Table 1: Assumed Transistor Parameters.

1 Calculating Interconnect Parameters

For this problem, we will calculate the resistance and capacitance (including data dependence) for a simple three bit bus, which consists of three signal lines (A, B, and C) shielded by two outside ground lines and driven by three edge-triggered flip-flops as shown in Figure 1.

Problem 1.1 Figure 2 shows a cross-section (not to scale) of the wires in the bus. Compute the capacitance per unit length to ground (c_L) and the coupling capacitance per unit length (c_C) assuming the following dimensions: $W = 0.4\mu$m, $S = 0.6\mu$m, $H = 0.4\mu$m, and $T = 0.6\mu$m. Assume a silicon dioxide dielectric and use the relative permittivity from Table 4-1 (p. 140) of the Rabaey text. Include the parallel plate and fringing field terms for both c_L and c_C. Note that Equation 4.2 may have an error (depending on which printing of the book you have), so use the formula as shown on Slide 11 in the Lecture 8 notes.

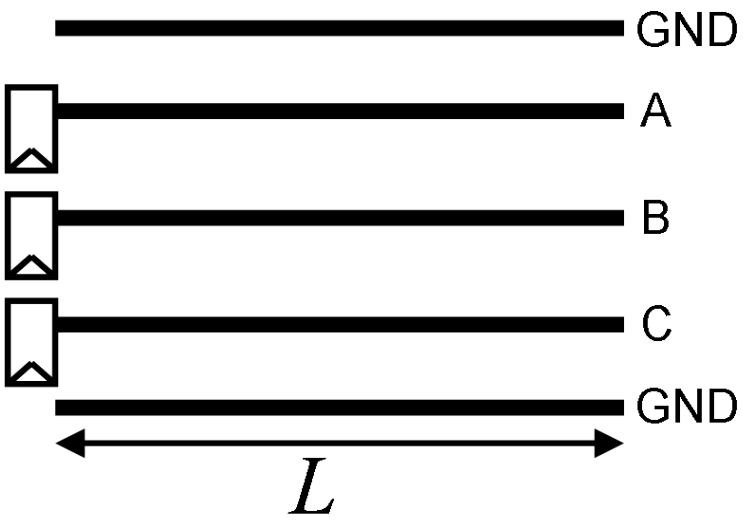

Figure 1: Three bit bus.

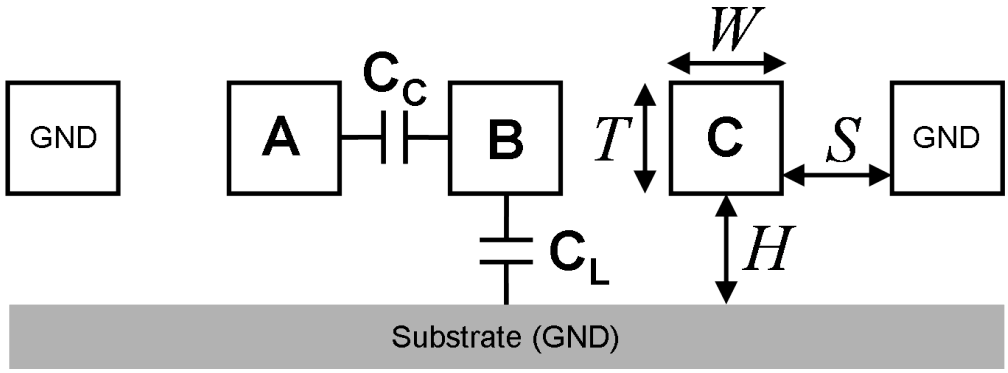

Figure 2: Three bit bus wire dimensions.

Problem 1.2 Is the approach to computing c_L and c_C used in Problem 1.1 optimistic or pessimistic? Justify your answer.

Problem 1.3 What is the **worst case** total capacitance per unit length for the middle signal B and under what circumstances does it occur (i.e., what are the waveforms on A, B, and C which result in this worst case total capacitance per unit length)?

Problem 1.4 What is the **best case** total capacitance per unit length for the middle signal B and under what circumstances does it occur (i.e., what are the waveforms on A, B, and C which result in this worst case total capacitance per unit length)?

Problem 1.5 Compute the resistance per unit length r using the dimensions of the wires shown in Figure 2 assuming aluminum wires and the resistivity shown in Table 4-4 (p. 145) in the book.

Problem 1.6 Suppose the bus wires have length $L = 1.0$mm. Using the Elmore delay approximation, what are the best and worst case delays for the signal B wire?

2 Inverter and Wire Delay

For this problem, use the device parameters in Table 1.

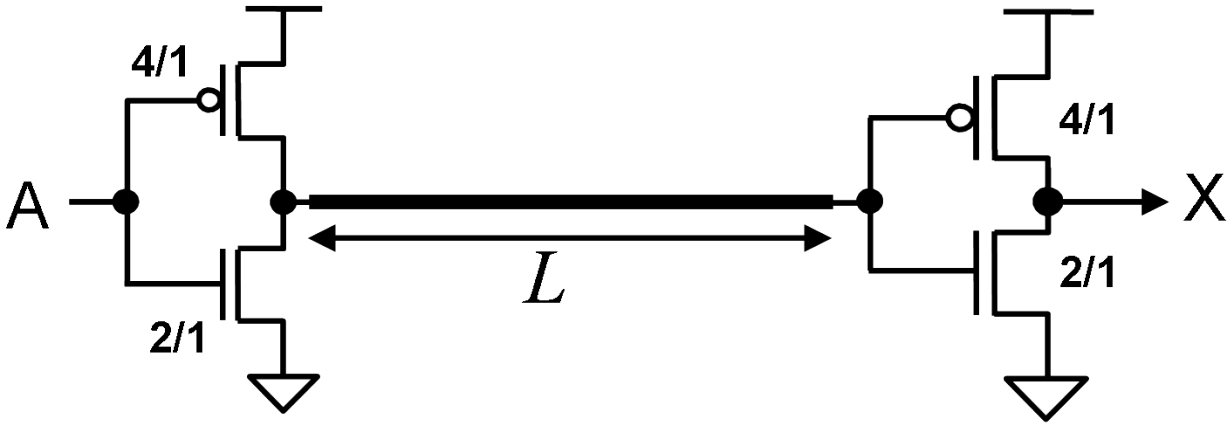

Figure 3: Inverter transmitter and receiver connected by a long wire.

Problem 2.1 Figure 3 shows two identical inverters separated by a wire of length L. Suppose $L = 0$mm. Calculate the propagation delay from input A to output X by first computing t_{pd} for each inverter using the switch RC approximation where R is computed by averaging the currents at the beginning and end of the relevant output transition and the total capacitance to ground at each inverter output is 4fF.

Problem 2.2 Suppose the wire has width $W = 1\mu$m and a sheet resistance $R_{sq} = 75\text{m}\Omega$/sq. What is the longest length L which results in an Elmore delay that is equal to the A-to-X propagation delay you calculated in Problem 2.1? Assume area and fringing capacitance values for Al1 over Field as shown in Table 4-2 (p. 143) of the textbook.

Problem 2.3 How long could the wire be given the same constraints as Problem 2.2 if it was routed on the Al5 layer over Field? Use the same Table 4-2 to find the capacitance parameters.

3 H-Tree Clock Network

Problem 3.1 An H-tree network is often used to distribute a low-skew clock from the center of a large chip to all sequential elements distributed over its area. Assume the H-tree in Figure 4 is routed in the Al5 layer over Poly (Table 4-2) with $W = 2.5\mu$m, $L = 1$cm, and $R_{sq} = 50\text{m}\Omega$/sq. Calculate the Elmore delay from the clock injection node S to nodes 1, 2, and 3.

Problem 3.2 What is the minimum hold time we would need to specify for a flip-flop which could be placed anywhere on the clock network from node 1 to node 3?

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.

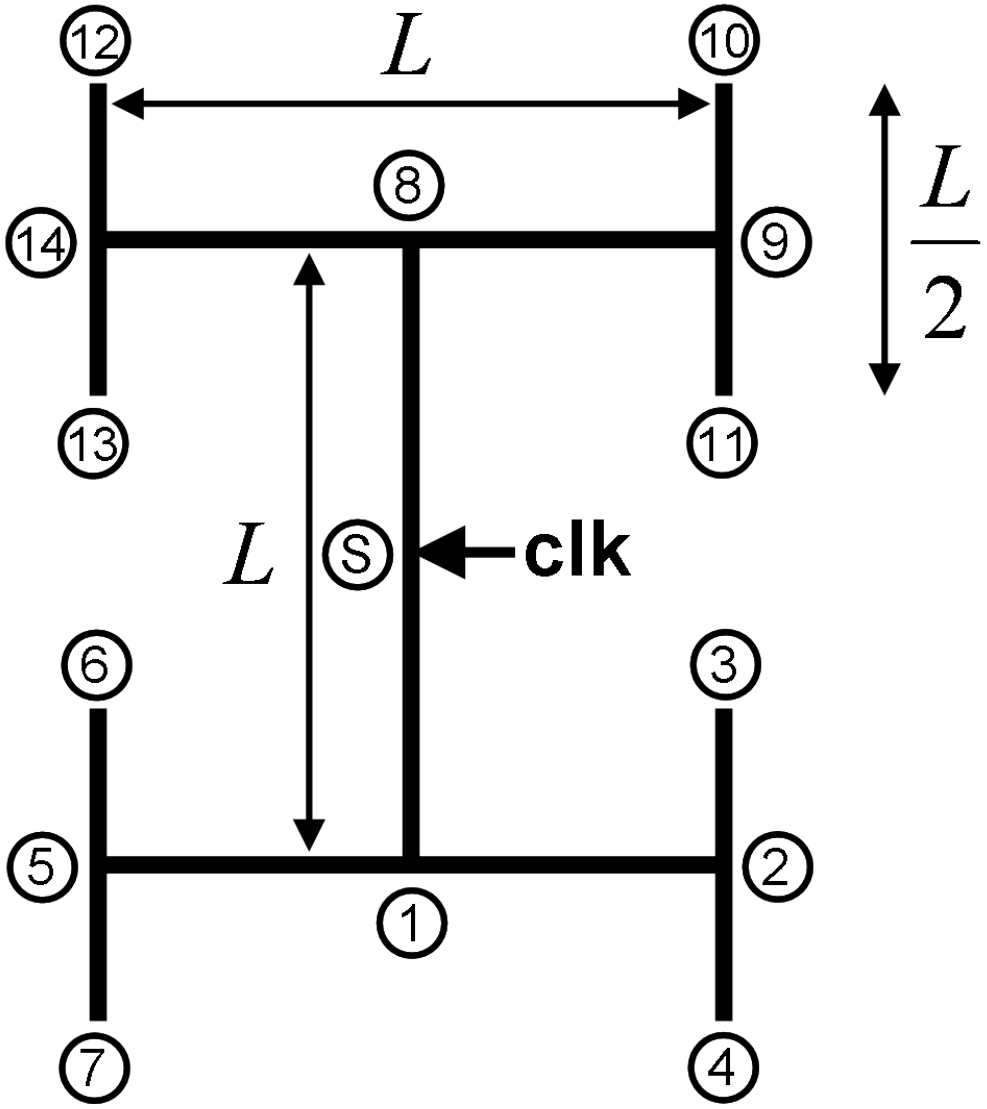

Figure 4: H-tree clock network for minimizing skew.