EEC 116 Fall 2011 Homework #4

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Reading: Rabaey Chapters 6.2 and 7.1-7.3 [1].
Reference: Kang and Leblebici Chapters 7 and 8 [2].

For **all** problems in this homework assignment, assume we are using enhancement-type NMOS and PMOS transistors which have the characteristics shown in Table 1, unless otherwise specified. Also, assume **minimum** length devices unless otherwise specified.

Parameter	NMOS	PMOS
V_{T0}	0.6 V	-0.7 V
μC_{ox}	300 μA/V^2	100 μA/V^2
γ	0	0
L_{min}	0.180μm	0.180μm
λ	0.0 V^{-1}	0.0 V^{-1}
V_{DD}	1.8 V	

Table 1: Assumed Transistor Parameters.

1 Transparent Latch

For this problem, use the device parameters in Table 1. Assume that all PMOS devices have $W/L = 1.44\mu$m$/0.180\mu$m and all NMOS devices have $W/L = 0.450\mu$m$/0.180\mu$m.

Problem 1.1 Redraw the schematic of Figure 1 and label the D, clk, $\overline{clk}$, and Q signals on the schematic such that the circuit operates as a static positive transparent latch.

Problem 1.2 Ignoring the feedback circuit in Figure 1, find the low to high propagation delay t_{pLH} from the input to the output assuming all inputs switch simultaneously using the average current method. Use at least two appropriate points in the output transition to compute the average current. Assume for the inverter that $t_{pLH} = t_{pHL} = 45$ ps, ideal voltage steps for the inputs, and that there is no capacitance other than C0.

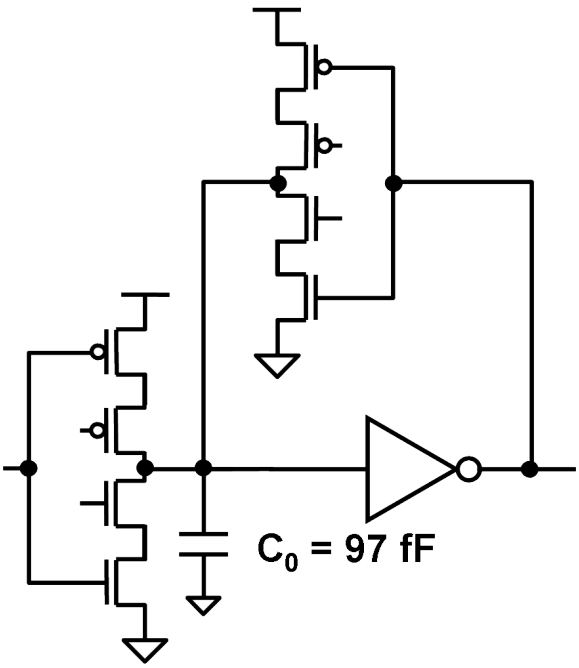

Figure 1: Transparent Latch.

Problem 1.3 Find the high to low propagation delay t_{pHL} from the input to the output using the same approach and making the same assumptions as in Problem 1.2.

Problem 1.4 Suppose a negative edge-triggered flip-flop uses the latch of Figure 1 as its master stage latch. What is a reasonable estimate of the setup time t_{setup} of the flip-flop?

2 Flip-Flop

For this problem, use the device parameters in Table 1.

Problem 2.1 Figure 2 shows the schematic for a positive edge-triggered flip-flop with an active-low clear. Is this a synchronous or an asynchronous clear? Justify your answer.

Problem 2.2 Find the switching threshold voltage V_M for the output inverter N5/P5. Is the switching threshold for the C^{2}MOS latch formed by transistors P1, P2, N1, and M2 different? Why or why not?

Problem 2.3 Calculate the clock-to-Q delay t_{CQ} for a high-to-low transition on the output Q using the average current method. Assume the setup time constraint is met and that the clock has an infinitely fast transition at each edge. Use the average current method outlined in Problem 1.2 and assume a transistor with dimensions 1.4/0.6 has a gate capacitance to ground (i.e., ignore the Miller effect) of 15fF and a source/drain capacitance of 10fF.

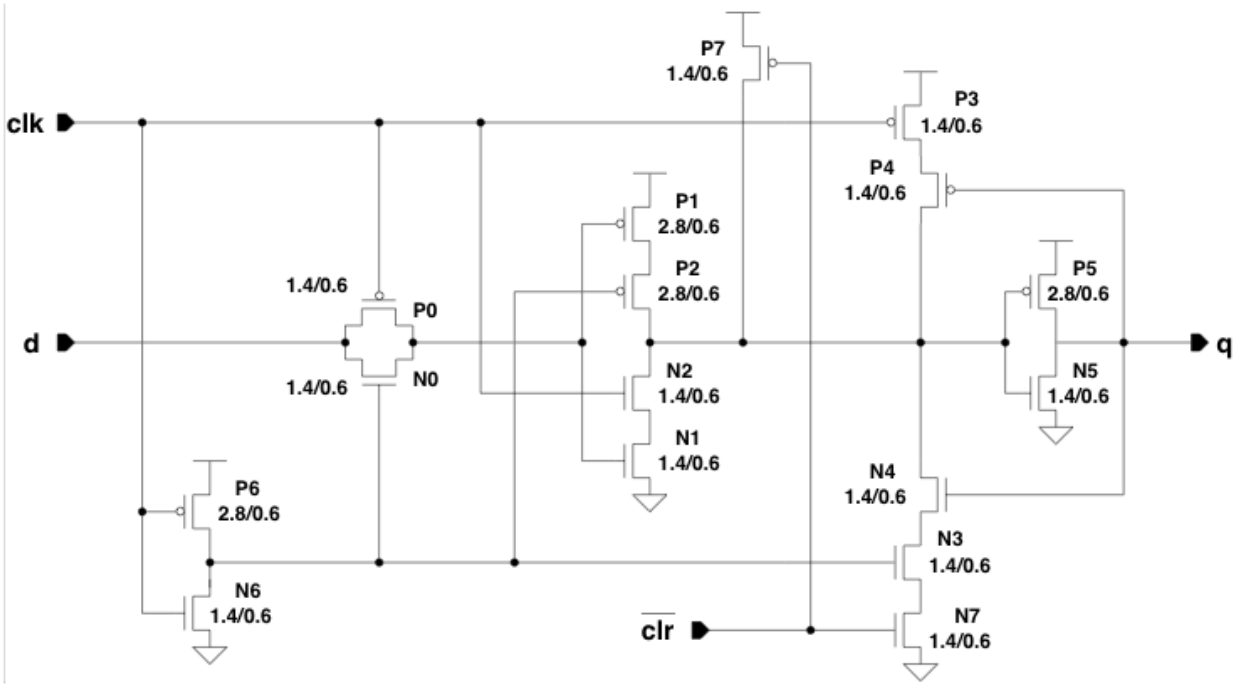

Figure 2: Flip-Flop. All dimensions in microns.

3 Mixed Combinational and Sequential Logic

Problem 3.1 A useful trick for highly optimized logic design is to fold a combinational CMOS circuit into a sequential circuit such as a latch. Modify the master stage latch circuit shown in Figure 7-26 in Rabaey to incorporate the logic function $F = A \cdot (B + C)$. Size the transistors such that the pullup and pulldown networks for the equivalent inverter have equal rise and fall times. Assume the mobility ratio $\mu_n/\mu_p = 2.5$, $V_{T0,n} = |V_{t0,p}|$, and a minimum sized device has $W/L = 5/1$. Write your answer in terms of the W/L ratios for the PMOS and NMOS devices. Hint: See Figure 7-31.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.