EEC 116 Fall 2011 Homework #3

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Reading: Rabaey Chapter 11, 5 [1].
Reference: Kang and Leblebici Chapter 5 [2].

1 Mirror Adder Delay Parameters

For this problem, consider the mirror adder schematic and transistor aspect ratios as shown in Figure 11-6 on p. 567 of the Rabaey textbook. Assume the units for the widths W in the figure are microns. Use the following device parameters for the transistors:

- NMOS: $V_{T0} = 0.4\text{V}$, $L = 0.8\mu\text{m}$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 300\mu\text{A/V}^2$
- PMOS: $V_{T0} = -0.5\text{V}$, $L = 0.8\mu\text{m}$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 150\mu\text{A/V}^2$

and assume the power supply voltage V_{DD} is 1.8 V.

Problem 1.1 Worst Case Delay Timing Diagram. Draw a timing diagram showing inputs A, B, and C_i and output $\overline{C}_o$ which result in the **worst** case propagation delays t_{pLH} and t_{pHL}.

Problem 1.2 Best Case Delay Timing Diagram. Draw a timing diagram showing inputs A, B, and C_i and output $\overline{C}_o$ which result in the **best** case propagation delays t_{pLH} and t_{pHL}.

Problem 1.3 Propagation Delay. Calculate the best and worst case low-to-high and high-to-low propagation delays (four delay values in total) using the average current method. Assume ideal voltage step inputs and average the current at the beginning and midpoint of the transition. Assume the capacitance at $\overline{C}_o$ is 4.8fF.

Problem 1.4 Rise and Fall Times. Calculate the best and worst case 10%-90% rise and fall times (four transition time values in total) using the switch RC model. Assume ideal voltage step inputs and that the resistance is fixed from the beginning of the transition. Assume the capacitance at $\overline{C}_o$ is 4.8fF.

2 Power Dissipation Components

Frequency	P_{tot}
10 MHz	101.3μW
20 MHz	190.4μW
30 MHz	279.5μW
40 MHz	368.6μW
50 MHz	457.7μW
60 MHz	546.8μW
70 MHz	635.9μW
80 MHz	725.0μW
90 MHz	814.1μW
100 MHz	903.2μW

Table 1: Problem 2 Measured Power Dissipation Values.

Table 1 shows measured total power consumption for an integrated circuit versus clock frequency. Assume the power supply voltage $V_{DD} = 1.8$V and that direct path (short-circuit current) power $P_{dp} = 0$.

Problem 2.1 Load Capacitance. Find the load capacitance C_L of the integrated circuit.

Problem 2.2 Leakage Current. Find the leakage current I_{leak} for the integrated circuit.

3 Floorplanning and Layout Optimization

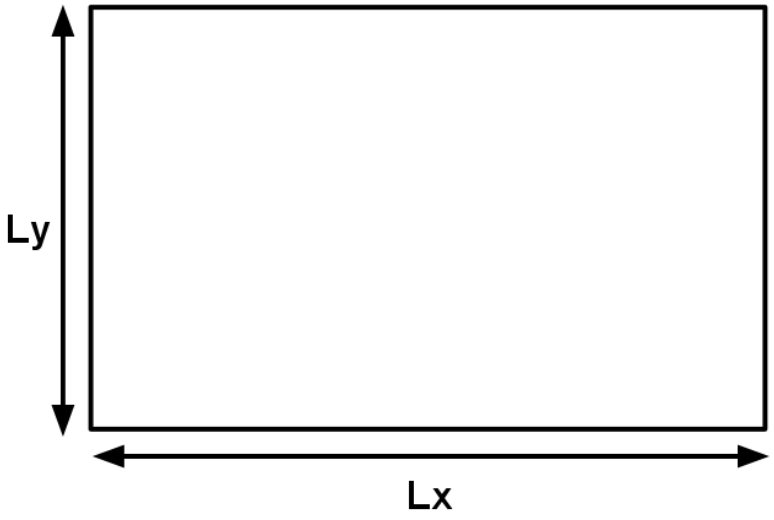

Figure 1: Adder cell layout with dimensions.

Figure 1 shows the horizontal and vertical dimensions of a full adder cell which will be used to implement an N bit adder. In this problem, you will find analytical results for the minimum area and perimeter of the adder as a function of its floorplan defined as its aspect ratio, i.e. the adder will be laid out in y rows each of which contain x cells. The adder floorplan is therefore a rectangular array of y rows and x columns.

Problem 3.1 Minimum Area. Find the values of x and y which minimize the N bit adder area and derive the minimum area A_{min} of the adder as a function of L_x, L_y and N. **Hint:** Use the method of Lagrange multipliers to show that your solution is optimal.

Problem 3.2 Minimum Perimeter. Sometimes you are more concerned with minimizing the perimeter of a design than its area, for example if you want to reduce interference with wiring tracks on different metal layers. Find the values of x and y which minimize the N bit adder perimeter and derive the minimum perimeter P_{min} of the adder as a function of L_x, L_y and N.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.