EEC 116 Fall 2011 Homework #2

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Reading: Rabaey, Chapters 3, 5, and 11 [1].
Reference: Kang and Leblebici, Chapters 3 and 5 [2].

1 FET Capacitances

An NMOS transistor is fabricated with the following physical dimensions and dopant concentrations:

- $t_{ox} = 200$Å
- $W = 10\mu$m
- $L_d = 1.5\mu$m
- $x_d = 0.25\mu$m
- $L_S = 5\mu$m
- $x_j = 0.4\mu$m
- $N_D = 10^{20}\text{cm}^{-3}$
- Substrate Doping $N_A = 10^{16}\text{cm}^{-3}$
- Channel Stop Implant Doping $N_A^+ = 10^{19}\text{cm}^{-3}$

Problem 1.1 Determine the drain diffusion capacitance for $V_{DB} = 5$V and 2.5V.

Problem 1.2 Calculate the overlap capacitance between gate and drain.

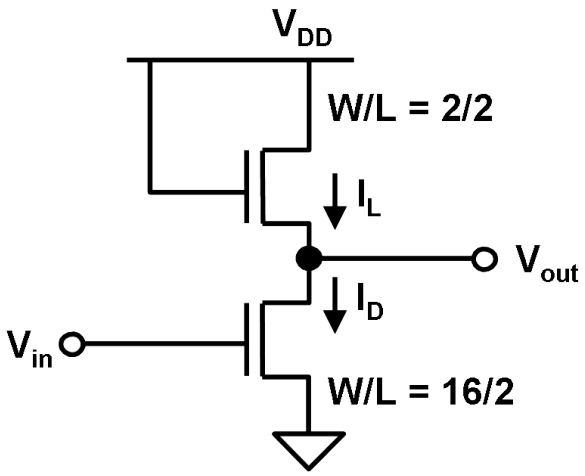

Figure 1: NMOS enhancement load inverter.

2 Enhancement Load Inverter

Consider the NMOS inverter circuit shown in Figure 1 which consists of two enhancement-mode NMOS transistors with the following parameters: $V_{T0} = 0.8\text{V}$, W/L ratios as shown in the figure, $\gamma = 0.38\text{V}^{1/2}$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 45\mu\text{A/V}^2$, $-2\Phi_F = 0.6\text{V}$, and $V_{DD} = 5\text{V}$.

Problem 2.1 Calculate values for V_{OH} and V_{OL}. Note that the substrate-bias effect for either or both devices must be taken into consideration.

Problem 2.2 Interpret your results for Problem 2.1 in terms of noise margins and static (DC) power dissipation.

Problem 2.3 Calculate the steady-state current which is drawn from the DC power supply when the input is a logic "1", i.e. when $V_{in} = V_{OH}$.

3 Two Input CMOS NOR Gate

Problem 3.1 Calculate V_{OL}, V_{OH}, V_{IL}, V_{IH}, NM_L, and NM_H for a two input CMOS NOR gate. Assume for the transistors the following parameters: $V_{T0,n} = 0.7\text{V}$, $V_{T0,p} = -0.7\text{V}$, $(W/L)_n = 1/1$, $(W/L)_p = 4/1$, $\mu_n C_{ox} = 40\ \mu\text{A/V}^2$, $\mu_p C_{ox} = 20\ \mu\text{A/V}^2$. Neglect γ and λ. $V_{DD} = 5\text{V}$. Assume that all inputs switch simultaneously.

4 Two Input CMOS NAND Gate

Problem 4.1 Assume that a two input CMOS NAND gate drives a total load capacitance of 0.1pF. All devices have $W = 10\mu\text{m}$, but the effective length for NMOS devices $L_{eff} = 1\mu\text{m}$ while for the PMOS devices $L_{eff} = 2\mu\text{m}$. Given that $k_n' = 20\mu\text{A/V}^2$, $k_p' = 10\mu\text{A/V}^2$, $V_{T,n} = 1.0\text{V}$, $V_{T,p} = -1.0\text{V}$, and $V_{DD} = 5\text{V}$, approximate t_{pLH} and t_{pHL}.

5 Logic Circuit

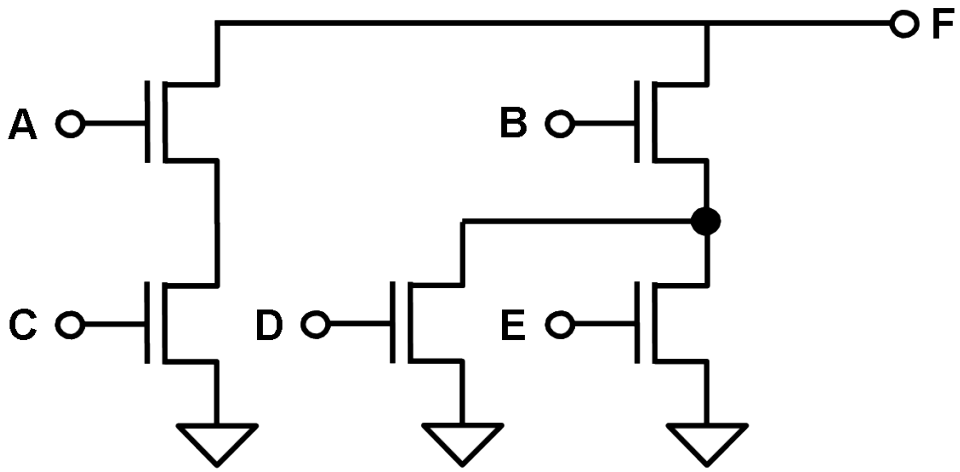

Figure 2: CMOS complex gate pulldown network.

For the CMOS logic you will be designing in this problem, assume the following transistor parameters:

- Pull-up transistor minimum $W/L = 10/5$
- Pull-down transistor minimum $W/L = 10/5$
- $V_{T0,n} = 1.0\text{V}$
- $V_{T0,p} = -1.0\text{V}$
- $\lambda = 0.0\text{V}^{-1}$
- $\mu_n C_{ox} = 300\mu\text{A/V}^2$
- $\mu_p C_{ox} = 100\mu\text{A/V}^2$
- $\gamma = 0.4\text{V}^{1/2}$
- $|2\phi_F| = 0.6\text{V}$

Problem 5.1 Write a Boolean expression for the output F as a function of the inputs.

Problem 5.2 Complete the gate schematic starting with the pulldown network shown in Figure 2. Choose sizes W/L for each NMOS and PMOS transistor such that the worst case pullup and pulldown paths have the same resistance as a minimum-sized NMOS pulldown transistor. .

Problem 5.3 Draw a stick diagram for the layout of the gate. Label all input and output nodes, both power supplies, and include the transistor dimensions. Include a key so that it is clear which layers the colors refer to.

6 Ripple Carry Adder Delay

Problem 6.1 Compute the worst case adder delay t_{adder} for a 16 bit ripple carry adder assuming the following delays: for the carry, $t_{pLH} = 3.2$ns, $t_{pHL} = 4.5$ns and for the sum, $t_{pLH} = 3.0$ns, $t_{pHL} = 3.9$ns. Justify your answer.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.