# EEC 116 Fall 2011 Homework #1

Rajeevan Amirtharajah
Dept. of Electrical and Computer Engineering
University of California, Davis

Issued: September 26, 2011
Due: October 5, 2011, 4 PM in 2131 Kemper.

**Reading:** Rabaey, Chapters 1, 2, A, 3, and 5 [1] and Moore [2].
**Reference:** Kang and Leblebici, Chapters 1 and 3 [3].

## 1 IC Trends

**Problem 1.1 Moore's Law for Microprocessors**. Figure 1 shows a plot of transistor count for microprocessors through 2008 [4]. Based on the evolutionary trends described in Chapter 1 of Rabaey, predict the integration complexity and the clock speed of a microprocessor in the years 2010, 2015, 2020, and 2025. How does your 2010 prediction compare to the data in the Moore's Law graph from lecture (which runs through 2011)?

**Problem 1.2 Moore's Law for DRAM**. Determine also how much DRAM should be available on a single chip at those points in time, if Moore's law would still hold.

## 2 Quality Metrics

**Problem 2.1 Metrics Priority**. Consider the four quality metrics described in Chapter 1: cost, functionality and robustness, performance, and power. If you were managing an IC design team, how would you rank these metrics from most important to least important for your product? Justify your answer.

## 3 MOS Transistor

**Problem 3.1 Channel Length**. Describe the relationship between the drawn channel length $L_d$ and the electrical channel length $L$. Are they identical? If not, how would you express $L$ in terms of $L_d$ and other device parameters?

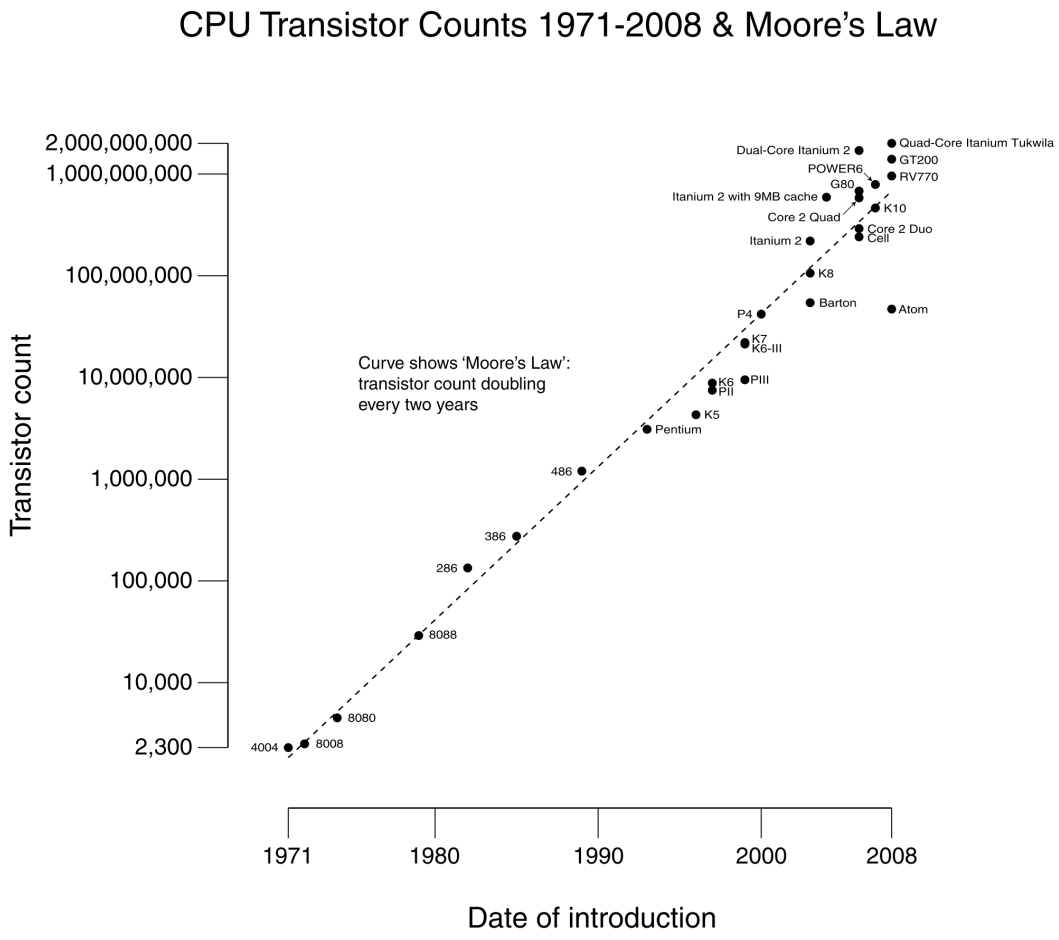



Figure 1: Moore's Law [4].

**Problem 3.2 Biasing**. Draw and label an NMOS and PMOS transistor with source, drain, and gate terminals clearly labeled S, D, and G respectively. Assume $V_{SB} = 0$V. Find the mode of operation (cutoff, linear, or saturation) and drain current $I_D$ for each of the applied biases given below. Assume for the NMOS that $V_{T0} = 0.7$V, $W/L = 4/1$, $\gamma = 0.35\text{V}^{1/2}$, $\lambda = 0.05$ V$^{-1}$, $\mu C_{ox} = 350$ $\mu$A/V$^2$, and $-2\Phi_F = 0.6$ V. Assume identical parameters for the PMOS except $V_{T0} = -0.8$V and $\mu C_{ox} = 150$ $\mu$A/V$^2$. Ignore velocity saturation and subthreshold conduction.

1. NMOS: $V_{GS} = 1.8$V, $V_{DS} = 1.8$V; PMOS: $V_{GS} = -1.1$V, $V_{DS} = -50$mV
2. NMOS: $V_{GS} = 0.9$V, $V_{DS} = 1.8$V; PMOS: $V_{GS} = -2.5$V, $V_{DS} = -1$V
3. NMOS: $V_{GS} = 1.5$V, $V_{DS} = 0.4$V; PMOS: $V_{GS} = -1.8$V, $V_{DS} = -1.6$V

# 4 CMOS Inverter

Consider a CMOS inverter with the following transistor parameters:

- NMOS: $V_{T0} = 0.3$V, $W/L = 8$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 250\mu\text{A/V}^2$
- PMOS: $V_{T0} = -0.35$V, $W/L = 12$, $\lambda = 0.0\text{V}^{-1}$, $\mu C_{ox} = 100\mu\text{A/V}^2$

Assume $V_{DD} = 2.5$V.

**Problem 4.1** Calculate the noise margins and the switching threshold ($V_M$) of this circuit.

**Problem 4.2** For this problem and the next, assume the channel length of both transistors is 0.8$\mu$m. Determine the $W_P/W_N$ ratio so that the switching threshold of the inverter is $V_M = 1.4$V.

**Problem 4.3** The CMOS fabrication process used to manufacture this inverter allows a variation in the NMOS threshold voltage $V_{T0,n}$ of $\pm 15\%$ around its nominal value of 0.6V, and a variation in the PMOS threshold voltage $V_{T0,p}$ of $\pm 20\%$ around its nominal value of -0.7V. Assuming that all other device parameters always retain their nominal values, find the upper and lower limits of the switching threshold $V_M$ of the circuit you designed in Problem 4.2.

# 5 Ring Oscillator

**Problem 5.1** A ring oscillator configuration shown in Figure 2 is often used to measure the average propagation delay time of an individual logic gate. Derive a formula which relates the average delay time to the period of the waveform observed at the output of any of the gates in an oscillator of $N$ total gates.

**Problem 5.2** Suppose the average propagation delay through an inverter in a seven inverter ring oscillator is 768ps. What are the period $T$ and frequency of the oscillation $f$?

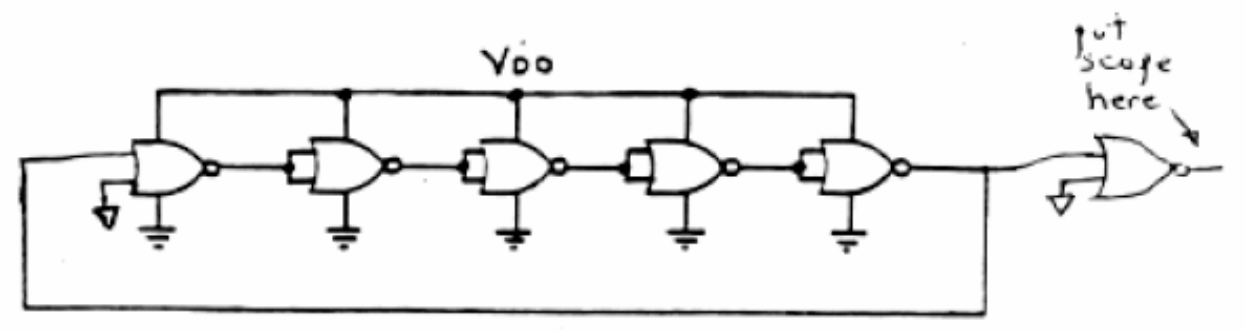
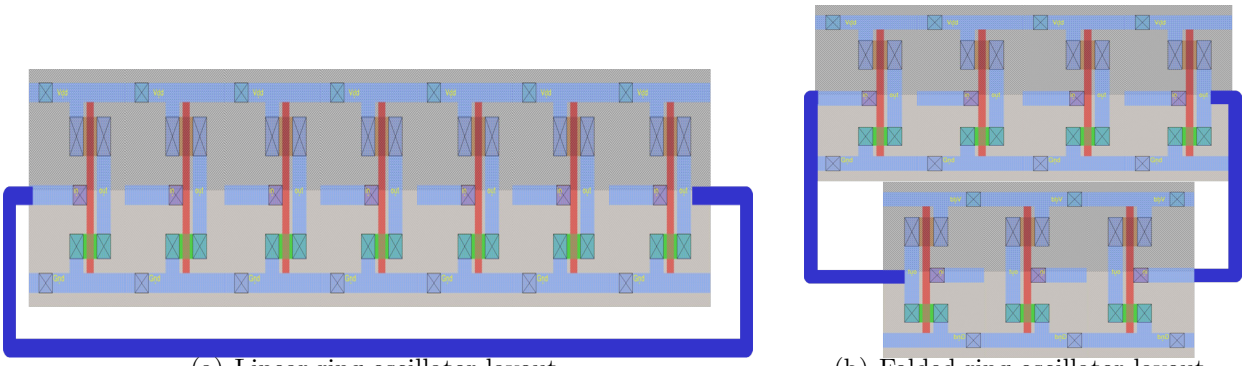



Figure 2: Connections for NOR gate ring oscillator.



(a) Linear ring oscillator layout. (b) Folded ring oscillator layout.

Figure 3: (a) Seven stage inverter ring oscillator laid out in a straight line with feedback wire. (b) Folded layout.

**Problem 5.3** Figure 3(a) shows a ring oscillator laid out in a straight line with a single wire for feedback from the output of the last inverter to the input of the first. Assume the inverters have the same delay as in Problem 5.2. Furthermore, assume that each inverter cell is 5$\mu$m high and 2$\mu$m wide and that each micron of wire length contributes 14ps of delay. Estimate the period $T$ and frequency of oscillation $f$ for the ring oscillator including the contribution of the wire.

**Problem 5.4** Figure 3(b) shows a ring oscillator laid out in two rows with two wires for feedback from the output of the end inverters in each row to the input of the beginning inverter in the other row. Assume the inverters and wires have the same delay properties as in Problem 5.3. Estimate the period $T$ and frequency of oscillation $f$ for the ring oscillator including the contribution of the wires.

**Problem 5.5** Which layout (straight line or folded) would give a more accurate estimate of the true propagation delay of each gate within the ring oscillator? Quantify the error by comparing the oscillation periods you derived in Problems 5.3 and 5.4 with the period from Problem 5.2 (which neglected the delay contribution of the wires).

# References


[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

[2] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–7, April 19 1965.

[3] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. San Francisco: McGraw-Hill, Inc., 2003.

[4] (2010, March) Moore's law. Wikimedia Foundation, Inc. [Online]. Available: http://en.wikipedia.org/wiki/Moore's_law