EEC 116 Lecture: Transmission Gate Logic

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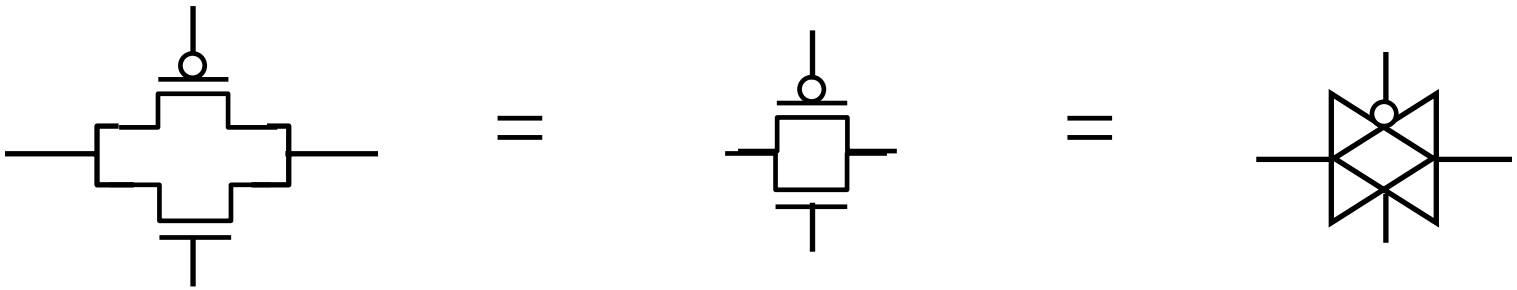
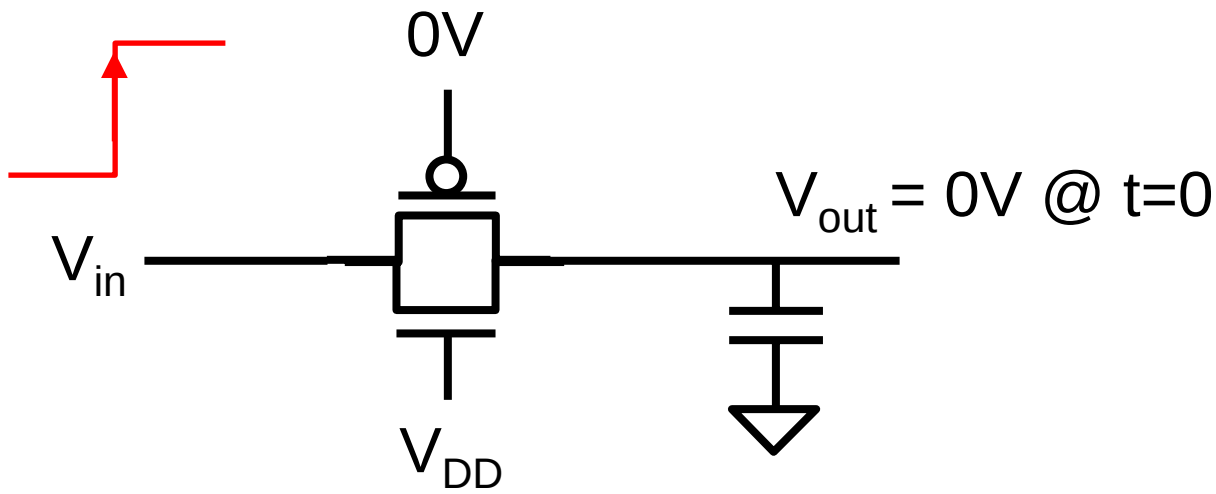
Transmission Gate Logic



- **NMOS and PMOS connected in parallel**
- **Allows full rail transition – ratioless logic**
- **Equivalent resistance relatively constant during transition**
- **Complementary signals required for gates**
- **Some gates can be efficiently implemented using transmission gate logic (XOR in particular)**

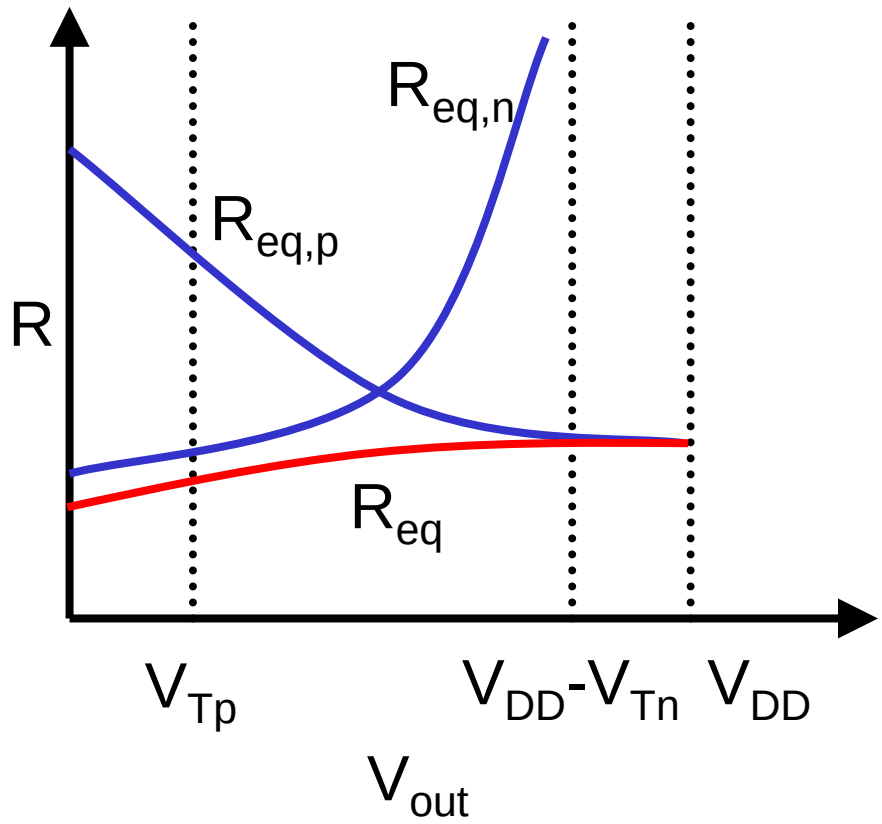
Equivalent Transmission Gate Resistance



- **For a rising transition at the output (step input)**
  - NMOS sat, PMOS sat until output reaches $|V_{TP}|$
  - NMOS sat, PMOS lin until output reaches V_{DD}-V_{TN}
  - NMOS off, PMOS lin for the final $V_{DD} – V_{TN}$ to V_{DD} voltage swing

Equivalent Resistance

- **Equivalent resistance R_{eq} is parallel combinaton of $R_{eq,n}$ and $R_{eq,p}$**
- **R_{eq} is relatively constant**



Resistance Approximations

- **To estimate equivalent resistance:**
  - Assume both transistors in linear region
  - Ignore body effect
  - Assume voltage difference (V_{DS}) is small

$$R_{eq,n} \approx \frac{1}{k_n\left(V_{DD} - V_{tn}\right)} \qquad R_{eq,p} \approx \frac{1}{k_p\left(V_{DD} - \left|V_{tp}\right|\right)}$$

$$R_{eq} \approx \frac{1}{k_n\left(V_{DD} - V_{tn}\right) + k_p\left(V_{DD} - \left|V_{tp}\right|\right)}$$

Equivalent Resistance – Region 1

- **NMOS saturation:**

$$R_{eq,n} = \frac{\left(V_{DD} - V_{out}\right)}{\frac{1}{2} k_n \left(V_{DD} - V_{out} - V_{tn}\right)^2}$$

- **PMOS saturation:**

$$R_{eq,p} = \frac{\left(V_{DD} - V_{out}\right)}{\frac{1}{2} k_p \left(-V_{DD} - V_{tp}\right)^2}$$

Equivalent Resistance – Region 2

- **NMOS saturation:**

$$R_{eq,n} = \frac{\left(V_{DD} - V_{out}\right)}{\frac{1}{2} k_n \left(V_{DD} - V_{out} - V_{tn}\right)^2}$$

- **PMOS linear:**

$$R_{eq,p} = \frac{2\left(V_{DD} - V_{out}\right)}{k_p \left(2\left(V_{DD} - \left|V_{TP}\right|\right)\left(V_{DD} - V_{out}\right) - \left(V_{DD} - V_{out}\right)^2\right)}$$

$$= \frac{2}{k_p \left[2\left(V_{DD} - \left|V_{TP}\right|\right) - \left(V_{DD} - V_{out}\right)\right]}$$

Equivalent Resistance – Region 3

- **NMOS cut off:**

$$R_{eq,n} = \infty$$

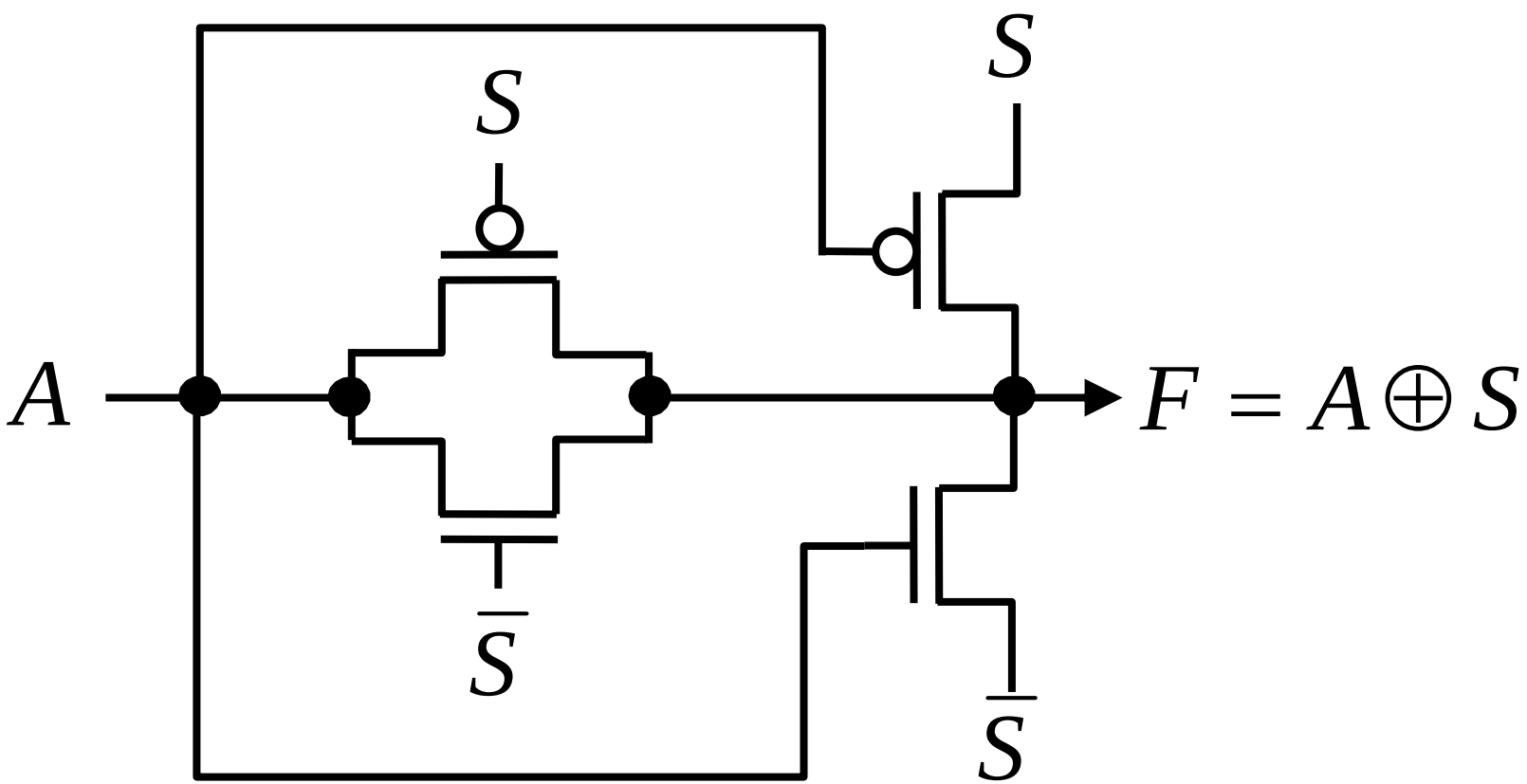
- **PMOS linear:**

$$R_{eq,p} = \frac{2}{k_p\left[2\left(V_{DD} - \left|V_{TP}\right|\right) - \left(V_{DD} - V_{out}\right)\right]}$$

Transmission Gate Logic

- **Useful for multiplexers (select between multiple inputs) and XORs**
- **Transmission gate implements logic function F = A if S**
  - If S is 0, output is floating, which should be avoided
  - Always make sure one path is conducting from input to output
- **Only two transmission gates needed to implement $A\overline{S} + \overline{A}S$**
  - Transmission Gate 1: A if $\overline{S}$
  - Transmission Gate 2: $\overline{A}$ if S

Transmission Gate XOR



- **If S = 0, F = A and when S = 1, F = ~A**

Transmission Gate Multiplexer