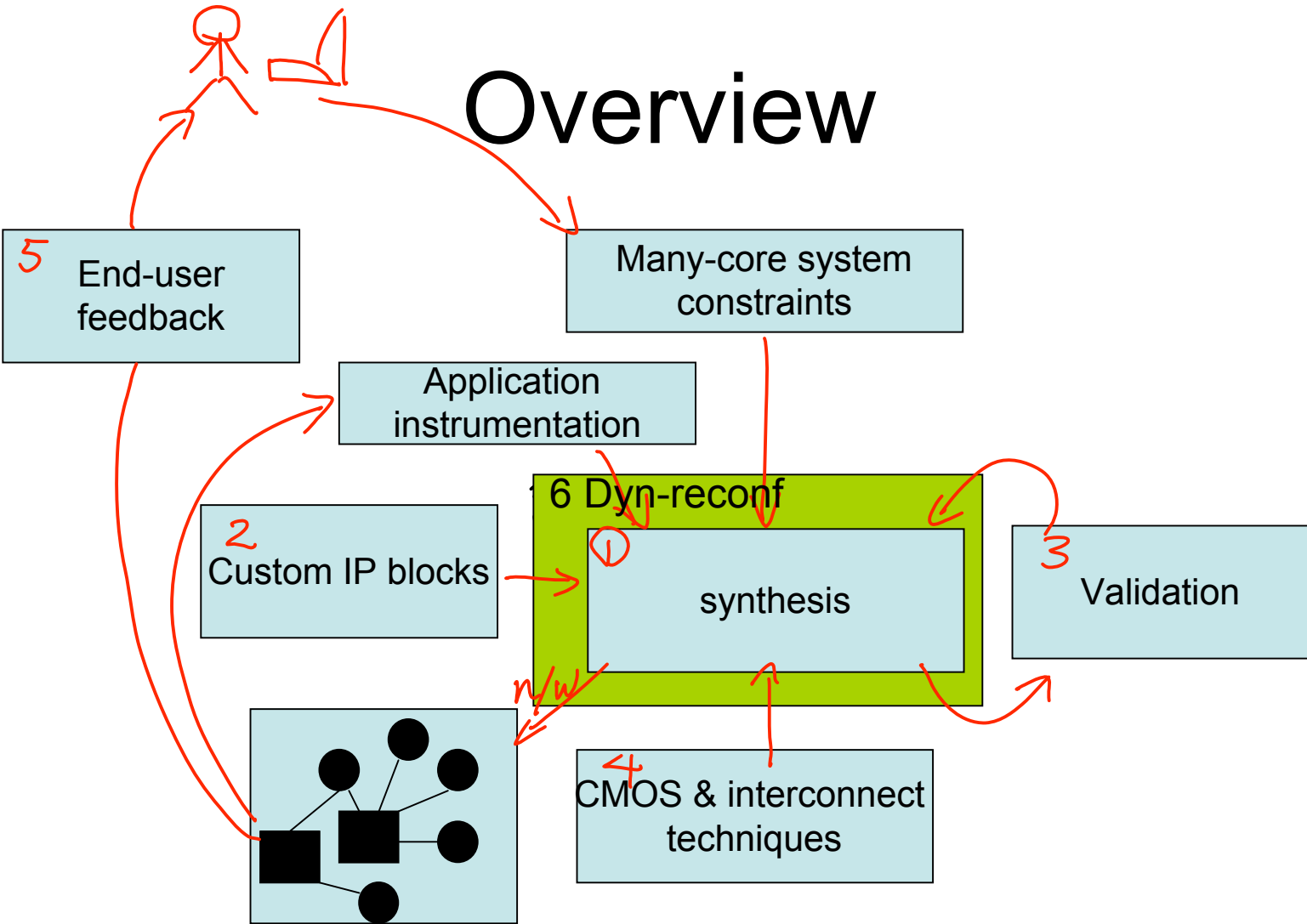# CAD and Design Tools for On-Chip Networks

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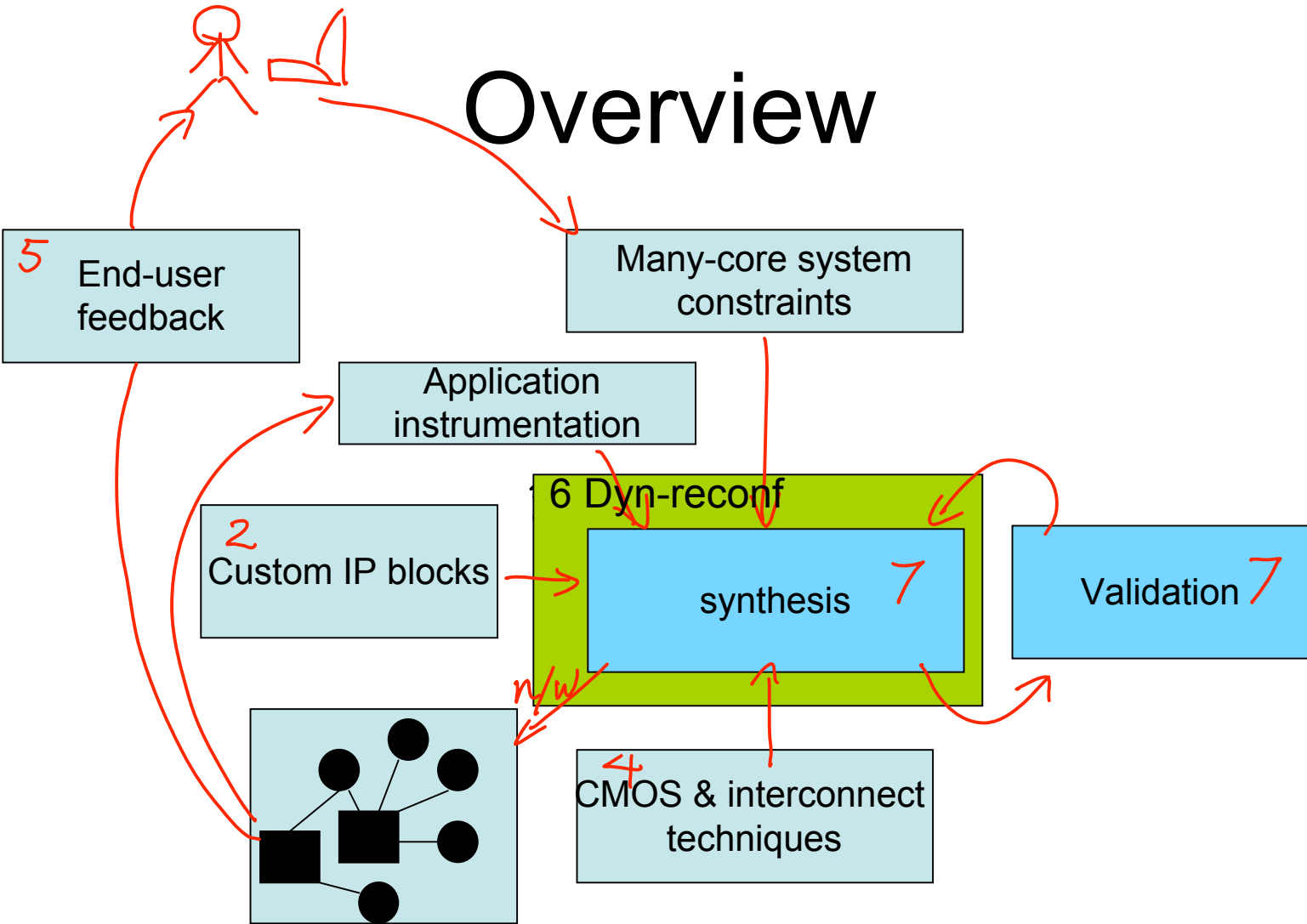
Research Challenges

1. Network synthesis' interface with system-level constraints and design
2. Hybrid custom and synthesized tool flow
3. Design validation
4. Impact of CMOS scaling and new interconnect technologies (e.g. 3D integration, optical)
5. End-user feedback design toolchain
6. Dynamic reconfigurable network tools
7. Beyond simulation

Overview

End-user feedback

Many-core system constraints

Application instrumentation

6 Dyn-reconf

Custom IP blocks

synthesis

Validation

CMOS & interconnect techniques

n/w

Overview

End-user feedback

Many-core system constraints

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Network synthesis challenges with many-core chips

- Interface with system-level constraints and requirements
- Traffic modeling
- High-performance yet standard network interface with a variety of processor cores?
- Network synthesis and design can influence and shape communications at the system level
- Synthesis tool has to take into account both on-chip and off-chip networks
- Specification of hard vs soft constraints; Sensitivity analysis

Hybrid custom and synthesized tool flow

- How hard custom-designed blocks can be readily synthesized

- What are the leaf cells for network synthesis?

- Specialized libraries for networks?

  – E.g. optimized crossbar?

  – Specialized high-performance link macros?

  – Implications for entire EDA tool flow.

Network validation

- How to make sure the designs are robust
- Made tougher in the face of process variations, run-time management
- Over-designing for robustness may lead to high cost
- Validation cost -> input to synthesis chain
- Variability may be higher

Impact of CMOS scaling and new interconnect technologies

- New timing, area, power, thermal, reliability models
- High-level physical design retooling
- New network design space
- CMOS scaling may require more co-synthesis

End-user feedback design toolchain

- E.g. rewrite FPGA design for different apps
- Run-time monitoring and optimization
- Feedback of network traffic to end users
- Specialized chips make network feedback and monitoring more important.
- Can learn from Internet and sensor networks instrumentation and monitoring tools
- Monitoring needs to track at the system-level, e.g. contention at a single sink, e.g. memory port

Dynamic network reconfiguration toolchain

- Soft router cores
- Configured on-the-fly
- Similar to JIT compilation
- Reconfiguring between circuit and packet switched networks

Beyond simulation

- Formal methods
- Queuing analysis
- Unique:
  - Physical challenges
  - Link-level flow control vs. end-to-end
  - Scale of on-chip networks vs. off-chip ones

Broader Impacts

- All challenges will critically impact MPSoC industry
- Challenges 2, 3, 4, 5 will be relevant to the general-purpose computing industry
- Enables complex, correct designs that will otherwise be impossible
- Design automation can facilitate the adoption of on-chip networks (by easing entry)
- Interactions with other working groups
  - Technology & Circuits (Challenge 4 – Impact of technology)
  - Evaluation and Driving Applications (Enabling Technology for these)
  - System Architecture (Challenge 1 – Interface with system constriants)
  - Microarchitecture (Challenge 2 – Custom IP blocks)