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Jitter Analysis of Current-Mode Logic Frequency Dividers

Ph.D. Research Proposal

Table of Contents

Section 1:

Introduction

As the signaling rates in today's communication systems grow and are now measured by tens of Gbps, timing uncertainty of signals (i.e. timing jitter) is becoming a bigger issue. Unfortunately, jitter does not scale down with the signal period and it can cause serious problems during data recovery at reception. In wireless systems, imperfect timing of the carrier signal causes interference between channels. As a result, jitter specifications for high-speed communication systems over copper, optical fiber or air, have to be very stringent.

A lot of research is being done in the area of phase noise and jitter analysis of high-performance clock and carrier signal generators, which are most commonly implemented using phase-locked loops (PLL). Most of the work is focusing on the analysis of voltage-controlled oscillators (VCO), which are parts of every PLL. VCO is definitely the most significant contributor to the PLL output jitter, since its output is at the same time the output of the PLL. However, it is not the only jitter source. As will be shown in this work, frequency divider (FD), another inevitable component of a GHz-range PLL, can also contribute significantly to the PLL output jitter. Yet, FD jitter and phase noise analysis has not received much attention, and not much work has been done in that area.

In this proposal, an analytical model which allows estimation of jitter generated by the frequency divider is presented. Having an analytical model for jitter is important for several reasons: amount of jitter generated by the circuit can be known before fabrication

and it allows determining whether the design meets the specifications in the early stages of the design process. Also, the model gives insight in dependence of jitter on circuit parameters, which allows minimizing jitter by appropriate design. Since design technique of choice in RF integrated circuits is the low-swing differential current-mode logic (CML), which allows high speed at low cost, this work focuses on jitter analysis of CML frequency dividers.

The proposal is organized as follows: Section 2 gives definitions of jitter used throughout the proposal. Section 3 investigates effects of FD noise on PLL output jitter and illustrates importance of studying and minimizing jitter generated by FD. Section 4 studies general characteristics of FD jitter, without analyzing mechanisms of jitter generation by the FD circuits. The most important part of the proposal is Section 5, which proposes an analytical model for transformation of FD device noise into jitter. Section 6 presents plans for the future work and emphasizes the contributions of this research.

Section 2:

Jitter definitions

Jitter is a variation of signal period from its nominal value. It can also be defined as a variation of zero-crossing times of the signal. The latter definition is usually used in context of differential signals: zero-crossing times refer to time instances when differential signal crosses the zero value. Jitter is a time-domain uncertainty of a periodic signal that is caused by device noise or interferences (power supply ripple, cross-talk, radiation etc). Due to these factors, duration of each cycle of a periodic signal is different. This variation of signal period from its nominal value, τ, often is modeled to have a Gaussian distribution, with a mean value of zero (on average, period of the signal is equal to the nominal, specified period), as shown in Fig. 2.1. Since jitter has a probabilistic nature, it is characterized by its root-mean-square (RMS) value, rather than its amplitude or peak-to-peak value. Jitter RMS value is also the standard deviation of jitter distribution, σ_τ. Square of the RMS value, σ_τ^2 is referred to as jitter power.

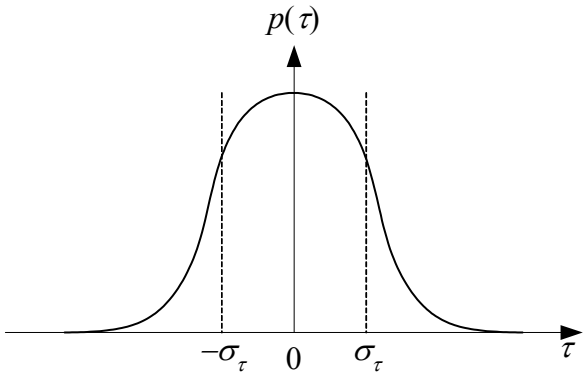


Fig. 2.1. Distribution of period variations of a realistic, periodic signal

Depending on the time interval over which jitter is measured, several definitions of jitter can be established: we can distinguish absolute, cycle, and cycle-to-cycle jitter. In the literature, different authors offer different definitions, but in this work, definitions from [Herz99] will be adopted, and in some cases somewhat modified.

2.1. Absolute jitter

Absolute jitter is measured over a long period of time, i.e. a large number of signal cycles. Therefore, absolute jitter is also referred to as long-term jitter. Jitter can be measured using an instrument such as Tektronix Communication Signal Analyzer (CSA) [McNe97], which is shown in Fig. 2.2. CSA operates as follows: after the arrival of the trigger signal, the device records the distribution (mean value and standard deviation) of the signal under test period, over the time interval specified by the value ΔT. For absolute jitter measurements, ΔT has to be equal to NT, where N is an integer, and T is the nominal period of the signal under test. As shown in [McNe97], in case of free-running oscillators, jitter measured this way depends on the measurement interval, ΔT, i.e. absolute jitter increases with measurement time. The reason for this is that uncertainty of the signal in the current cycle affects all the following transitions and its effects accumulate [Haji99, McNe97].

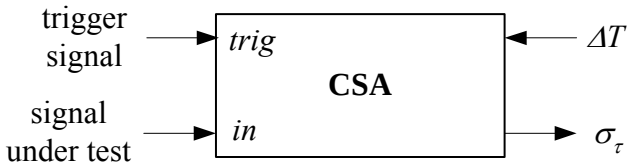


Fig. 2.2. Jitter measurement using communication signal analyzer

The following definition for absolute RMS jitter, σ_τ^{abs}, is a modified definition from [Herz99]:

$$\sigma_\tau^{abs} = \sigma_\tau^{abs}(N) = \lim_{M\to\infty} \sqrt{\frac{1}{M}\sum_{m=1}^{M}\left(NT_m - NT\right)^2} \tag{2.1}$$

Absolute RMS jitter depends on the measurement interval, i.e. number of cycles observed, N, and it is obtained from a large number of measurements, M (ideally $M\to\infty$). In (2.1), NT_m signifies the end of the N^{th} cycle of the signal under test, in the m^{th} measurement (Fig. 2.3). NT is the end time of the N^{th} cycle of the nominal signal (i.e. N nominal signal periods). Absolute RMS jitter can be found using (2.1).

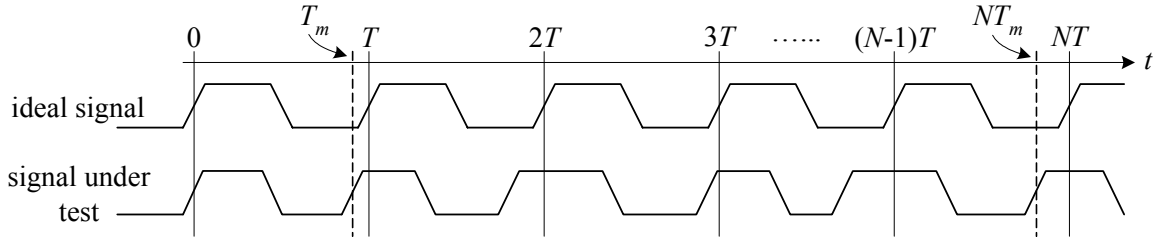


Fig. 2.3. Jitter measurements (time diagrams in the m^{th} measurement)

In [Herz99], definition of the absolute jitter is the following:

$$\Delta T^{abs}(N) = \sum_{n=1}^{N}(T_n - T)$$

In the equation above, T_n signifies the signal period in the n^{th} cycle and T is the nominal period. This definition gives a value for jitter from only one measurement. As mentioned above, jitter is a random process, and therefore, we are more interested in its mean value and standard deviation, than its instantaneous value. For this reason, in this work, we will use definition (2.1) for absolute jitter.

2.2. Cycle jitter

Cycle jitter definition is taken from [Herz99]. Cycle RMS jitter, σ_τ^{cyc}, can be found by the following expression:

$$\sigma_\tau^{cyc} = \lim_{M\to\infty} \sqrt{\frac{1}{M}\sum_{m=1}^{M}(T_m - T)^2} \tag{2.2}$$

In the equation above, T_m is the period of the signal under test, in the m^{th} measurement, and T is the nominal signal period (Fig. 2.3). (2.2) can be obtained from (2.1), by substituting N=1. Cycle RMS jitter shows standard deviation of one signal period from its nominal value. In the literature, when a RMS jitter value is reported, it usually refers to the cycle jitter unless specified otherwise.

2.3. Cycle-to-cycle jitter

Cycle-to-cycle jitter definition is taken from [Herz99]. Cycle-to-cycle jitter shows a variation of signal period between two consecutive signal cycles:

$$\sigma_\tau^{c-c} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N}(T_{n+1} - T_n)^2} \tag{2.3}$$

In the equation above, T_n signifies the measured signal period, n cycles from the start of the measurement. Cycle-to-cycle jitter will not be used in this work, but definition (2.3) is given for completeness.

It is important to understand the difference between cycle and cycle-to-cycle jitter: cycle jitter is the difference between signal period and the nominal period, while cycle-to-cycle jitter shows variation of the signal period in two consecutive signal cycles.

It should be noted that some authors refer to (2.2) as cycle-to-cycle jitter [Haji99, Demi00], and (2.3) as inter-cycle jitter. In this work terminology from [Herz99] was

adopted. Therefore, cycle and cycle-to-cycle jitter are defined as in (2.2) and (2.3), respectively.

2.4. Jitter specifications and peak-to-peak jitter

Jitter specifications for digital systems are usually expressed using the RMS value of jitter, σ_τ. Knowing σ_τ, we know that about 67% of the time, jitter amplitude falls within the range of [0, σ_τ]. Peak-to-peak jitter is the maximum jitter amplitude that can occur in a system. Since jitter has a probabilistic nature, it is hard to determine the real value of peak-to-peak jitter. However, knowing that more than 99% of the jitter amplitude falls within [0, $3\sigma_\tau$], a number α (usually greater than 3) can be found depending on the application, and peak-to-peak jitter can be defined as $\alpha\sigma_\tau$ [MaxiAN].

It should also be noted that both RMS jitter and peak-to-peak jitter are usually expressed relative to the nominal signal period (unit interval, UI, e.g. 0.01UI).

2.5. Phase noise

As mentioned before, jitter represents a variation of signal period from its nominal value; therefore, it is a time-domain figure of merit. The signal uncertainty can also be expressed in the frequency domain and then, it is referred to as phase noise. Phase noise is usually expressed as relative power of a spectral component at the offset frequency f_m from the carrier (nominal frequency), with respect to the carrier signal power. Power of the spectral component at the offset frequency f_m is measured in the bandwidth of 1Hz. Definition of phase noise is:

$$L(f_m) = 10\log\frac{P(f_m)}{P_0} \tag{2.4}$$

Phase noise is expressed in dBc (decibels below carrier): as an example, a 10GHz oscillator can have phase noise of -90dBc at the offset frequency of 1kHz (Fig. 2.4). Ideally, spectrum of a periodic signal consists of components at integer multiples of the fundamental (nominal) frequency (Fourier series of a periodic signal). In this case, $L(f_m \neq 0)=0$. However, due to noise, spectral content of the signal around carrier (at nominal frequency) will look as in Fig. 2.4 (taken from [Poor01]):

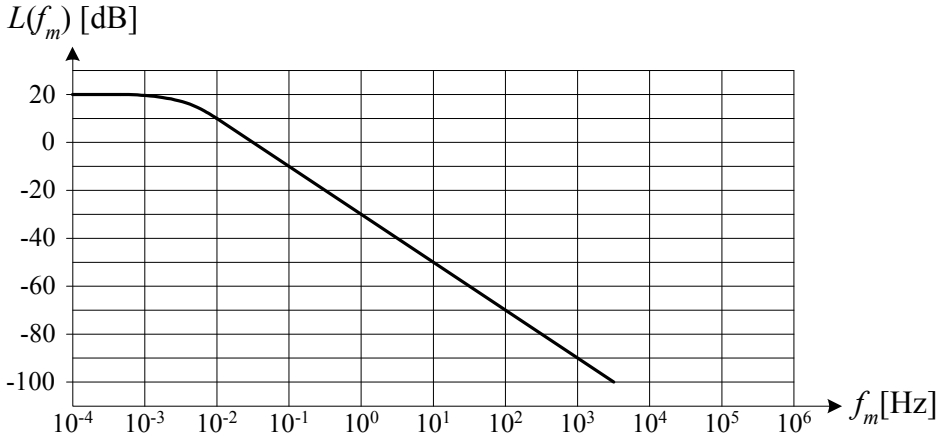


Fig. 2.4. Typical oscillator phase noise plot

Phase noise characteristic can be approximated with a Lorentzian spectrum [Demi00, Poor01]:

$$\frac{P(f_m)}{P_0} = \frac{1}{\pi}\frac{\pi f_0^2 c}{(\pi f_0 c)^2 + f_m^2} \tag{3.2}$$

In the equation above, f_0 is the nominal frequency of oscillation, f_m is the offset frequency and c is a constant which represents a characteristic of the oscillator.

It should be emphasized that phase noise can be described by (3.2) and a plot as the one in Fig. 2.4, only when colored noise sources (e.g. 1/*f* or burst noise) are not present in the circuit, i.e. when noise sources are uncorrelated.

2.6. Relationship between jitter and phase noise

When only white noise is present in the oscillator circuit, phase noise characteristic can be approximated by (3.2). This equation contains the coefficient *c* which is a figure of merit of the oscillator and depends on circuit topology, as well as noise parameters of the circuit. As shown in [Demi00], when only white noise is present in the circuit, absolute jitter power of the oscillator is proportional to the product of *c* and measurement time:

$$\sigma_{\tau,abs}^2 = ct \tag{3.3}$$

Therefore, a relationship between phase noise and cycle jitter can be established using (3.2) and substituting $t=1/f_0$ in (3.3):

$$\sigma_{\tau,cyc}^2 = \frac{f^2 L(f_m)}{f_0^3}$$

It is very important to emphasize that, this relationship between jitter and phase noise holds only when all the noise sources in the circuit are white. When colored noise sources are present, there is no unique relationship between phase noise and jitter. The reason for this is the difficulty of approximating oscillator spectrum by a closed-form expression [Haji97, Poor97].

Section 3:

Effects of frequency divider noise on PLL output jitter

As mentioned in the introductory section, there is a lot of research going on in the area of jitter and phase noise analysis of RF circuits. However, most of that work focuses on the VCO noise. We will now show that the FD noise can also contribute to the jitter at the PLL output, illustrating the importance of FD jitter analysis.

3.1. PLL basics

Block-diagram of a PLL with a charge pump, which is commonly used for clock signal generation in Gbps transceivers, is shown in Fig. 3.1 [Best03]. Frequency divider FD outputs a signal v_{FD} whose frequency is N times lower than frequency of the PLL output signal v_{out}. Phase-frequency detector PFD compares phases (and frequencies) of v_{FD} and v_{ref}. v_{ref} is a reference signal with a high spectral purity, usually obtained from a crystal oscillator. Charge pump generates an output current I_{CP} whose average value is proportional to the phase difference, with a proportionality coefficient K_P. High-frequency components of I_{CP} are eliminated by the loop filter LP with a low-pass transfer function $F(s)$. Output of the filter is a low-frequency voltage V_C which controls the frequency of the VCO output signal, v_{out}. Frequency of v_{out} is proportional to V_C with a proportionality coefficient K_O.

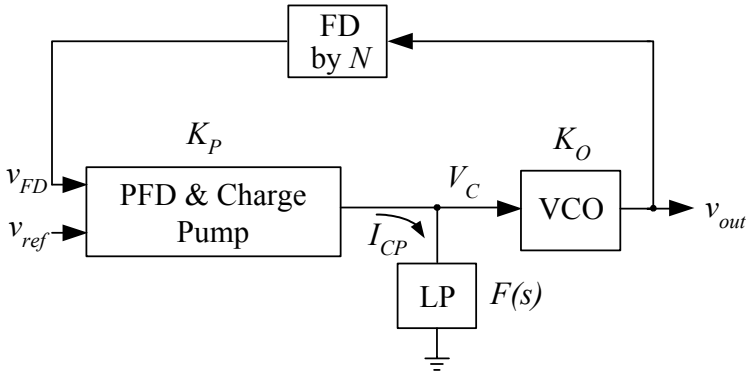


Fig. 3.1. Block-diagram of a PLL with a charge pump

Negative feedback in the PLL from Fig. 3.1 will attempt to neutralize any phase (and frequency) difference between signals v_{FD} and v_{ref} and adjust the VCO control voltage V_C so that, when PLL is locked, frequency of v_{out} will be exactly N times higher than frequency of the reference v_{ref}.

When locked, PLL from Fig. 3.1 can be represented by a linear model shown in Fig. 3.2. Input and output signals in this PLL diagram are phase offsets, (e.g. Φ_{FD} is the Laplace transform of ϕ_{FD}, where ϕ_{FD} is the time-domain phase offset of the FD output signal: $v_{FD}=W_{FD}(2\pi f_{in}t+\phi_{FD})$. In this equation, f_{in} is the nominal frequency of the FD output signal and $W_{FD}(x)$ is a 2π-periodic function representing the FD output). This model gives insight in dynamic behavior of the PLL around the locked state (i.e. response of the PLL on small variations in phase and frequency of v_{ref}).

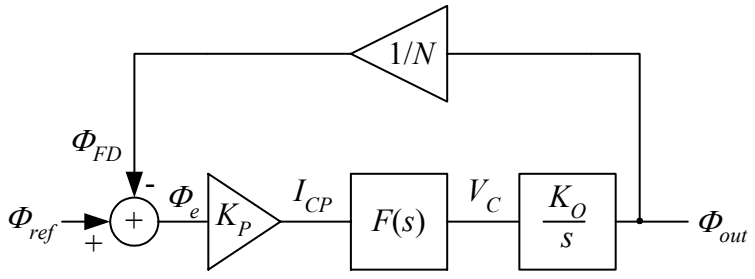


Fig. 3.2. Linear model of a PLL

Transfer function of the PLL from Fig. 3.2, $H(s)$, is given as

$$H(s) = \frac{\Phi_{out}}{\Phi_{ref}} = \frac{NK_P K_O F(s)}{Ns + K_P K_O F(s)}$$

or, for natural frequencies, f (by substituting $s=j2\pi f$ in the above equation):

$$H(jf) = \frac{NK_P K_O F(jf)}{jNf + K_P K_O F(jf)}. \tag{3.1}$$

$H(jf)$ is a low-pass transfer function with a DC value $|H(j0)|=N$. Exact shape of the magnitude characteristic of the PLL transfer function depends on the loop filter transfer function $F(s)$, but a typical plot of $|H(jf)|$ is sketched in Fig. 3.3. Frequency at which magnitude $|H(jf)|$ reaches $1/\sqrt{2}$ of its DC value is called PLL loop bandwidth, B_{PLL}. Now, we can mention that the linearized model in Fig. 3.2, more closely represents the PLL from Fig. 3.1 when $B_{FD} << f_{in}$ (i.e. when dynamics of the loop is slower than dynamics of the signals)

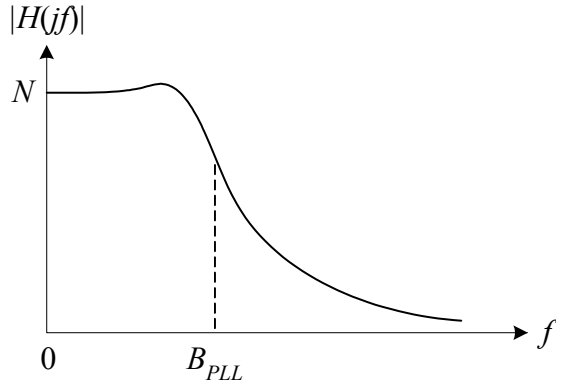


Fig. 3.3. Magnitude of PLL transfer function

As mentioned above, PLL transfer function describes the frequency-domain response of a PLL on small variations in phase and frequency of the reference signal v_{ref}. Knowing the PLL frequency response is also important for jitter and phase noise analysis, since phase noise is nothing else but unwanted variations of signal phase or frequency.

3.2. Propagation of FD jitter through PLL

To study effects of the frequency divider jitter (phase noise) on PLL output jitter, we need to assume that all other components of the PLL are ideal (i.e. noiseless) and that frequency of the reference signal v_{ref} is constant (i.e. phase noise of v_{ref} is zero). Without loss of generality, we can assume that Φ_{ref} in Fig. 3.2 is Φ_{ref}=0. The only noisy element is the FD, so all the jitter that occurs at the PLL output comes from the frequency divider. Our goal is to find the portion of the FD-generated jitter that is passed through from FD output to the PLL output.

Ideally, when there are no noise sources present in the PLL, signal v_{FD} will have a constant frequency f_{in}, and the zero-crossing of v_{FD} will always occur at time instants $t=nT_{in}$, where T_{in} is the nominal period of v_{FD} (and v_{ref}), and n is an integer. Let us assume that the FD contains only white, uncorrelated noise sources (e.g. only thermal noise of the resistors used in the circuit) and that the equivalent noise bandwidth of the FD circuit is B_{FD} (in Hz). These noise sources cause zero-crossing times of v_{FD} to vary from nT_{in} by a value τ. τ represents jitter and is a random variable, whose distribution we will assume to be Gaussian, with a mean of zero and a standard deviation (RMS value) of σ_τ, as was shown in Fig. 2.1. RMS value of FD jitter, σ_τ, can be obtained through measurements, when FD is out of the PLL. Using results of [McNe97] which indicate that the power spectral density (PSD) of jitter is proportional to the PSD of device noise, and approximating the FD with an ideal low-pass transfer characteristic with bandwidth B_{FD}, we assume that the single-sided PSD of τ, $S_\tau(f)$, looks as depicted in Fig. 3.4.

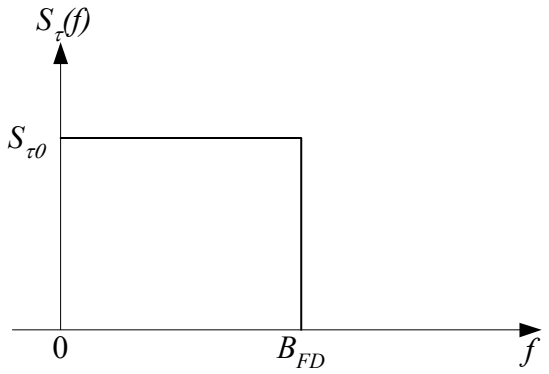


Fig. 3.4. Jitter power spectral density

According to Parseval's theorem, power of jitter has to be the same in the time- and frequency-domain; therefore, from Fig. 3.4:

$$S_\tau(0)B_{FD} = \sigma_\tau^2 . \tag{3.2}$$

Let us now try to relate jitter and phase noise so that we can use the linearized PLL model from Fig. 3.2 and the transfer function (3.1) to find PLL output jitter. Variations of zero-crossing time (i.e. variations of T_{in}) cause variations of signal phase. Therefore, jitter can also be represented as phase noise, using the relationship:

$$\frac{\Delta T_{in}}{T_{in}} = \frac{\Delta\phi}{2\pi} \Rightarrow \Delta\phi = \frac{2\pi}{T_{in}}\Delta T_{in} . \tag{3.3}$$

Using (3.3), PSD of phase noise $S_\phi(f)$ can be obtained as:

$$S_\phi(f) = \left(\frac{2\pi}{T_{in}}\right)^2 S_\tau(f) \tag{3.4}$$

and it has the same profile as jitter PSD in Fig. 3.4 with the DC value (at f=0):

$$S_\phi(0) = \left(\frac{2\pi}{T_{in}}\right)^2 S_\tau(0) = \left(\frac{2\pi}{T_{in}}\right)^2 \frac{\sigma_\tau^2}{B_{FD}} . \tag{3.5}$$

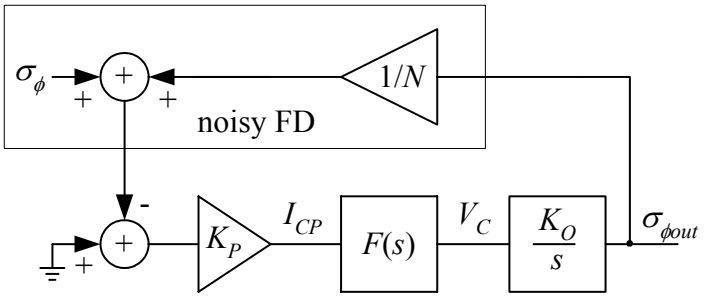
Noisy frequency divider from the linearized PLL model in Fig. 3.2 can be modeled as an ideal FD, with an additive phase noise source at its output, as shown in Fig. 3.5a. PSD of that phase noise source is $S_\phi(f)$, given in (3.4), and its power is

$$\sigma_\phi^2 = S_\phi(0) B_{FD} = \left(\frac{2\pi}{T_{in}}\right)^2 \sigma_\tau^2 \tag{3.6}$$

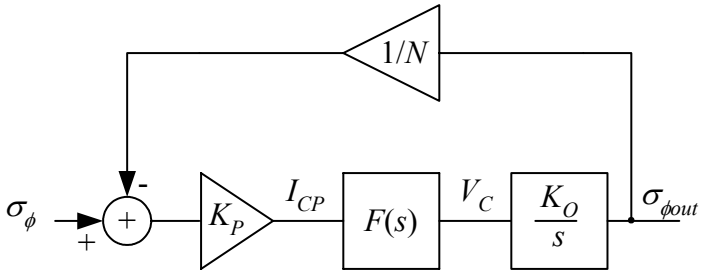
where σ_ϕ is the RMS value of the phase noise source. In Fig. 3.5a, $\sigma_{\phi out}$ is the PLL output RMS phase noise, caused by σ_ϕ. PSD of the PLL output phase noise $S_{\phi out}$ can be found as

$$S_{\phi out} = \left|H_a(jf)\right|^2 S_\phi \tag{3.7}$$

where $H_a(jf)$ is the transfer function from σ_ϕ to $\sigma_{\phi out}$ of the system in Fig. 3.5a, for natural frequencies, $s=j2\pi f$.



a)



b)

Fig. 3.5. Linear PLL with a noisy FD

Note that $H_a(jf) = -H(jf)$, where $H(jf)$ is the transfer function of the linearized PLL model from Fig. 3.2, defined in (3.1). Therefore, $|H_a(jf)|^2 = |H(jf)|^2$ and expression for the PLL

output phase noise PSD from (3.7) remains the same if the FD noise source σ_ϕ is moved to the PLL input, as shown in Fig. 3.5b. In other words, FD output noise is seen by the PLL as input noise.

Power of the output phase noise can now be found by substituting $H_a(jf)$ with $H(jf)$ in (3.7), and integrating (3.7) over all frequencies:

$$\sigma_{\phi out}^2 = \int_0^{+\infty} S_{\phi out}(f)df = \int_0^{+\infty} \left|H(jf)\right|^2 S_\phi(f)df = S_\phi(0)\int_0^{B_{FD}} \left|H(jf)\right|^2 df \ . \tag{3.8}$$

Output phase noise power can be expressed in terms of FD RMS jitter using (3.6):

$$\sigma_{\phi out}^2 = \left(\frac{2\pi}{T_{in}}\right)^2 \frac{\sigma_\tau^2}{B_{FD}} \int_0^{B_{FD}} \left|H(jf)\right|^2 df \ . \tag{3.9}$$

Finally, output phase noise power can be represented as the output jitter power, using an expression analogous to (3.6), but with T_{out} instead of T_{in}:

$$\sigma_{\phi out}^2 = \left(\frac{2\pi}{T_{out}}\right)^2 \sigma_{\tau out}^2 \ . \tag{3.10}$$

where $\sigma_{\tau out}$ is the RMS value of the PLL output jitter, and T_{out} is the nominal period of the PLL output signal v_{out} from Fig. 3.1 ($T_{in}=NT_{out}$).

Combining (3.9) and (3.10), a final expression which shows the relationship between PLL output jitter power and FD jitter power is obtained:

$$\sigma_{\tau out}^2 = \left(\frac{T_{out}}{T_{in}}\right)^2 \frac{\sigma_\tau^2}{B_{FD}} \int_0^{B_{FD}} \left|H(jf)\right|^2 df = \frac{1}{N^2} \frac{\int_0^{B_{FD}} \left|H(jf)\right|^2 df}{B_{FD}} \sigma_\tau^2 \tag{3.11}$$

or in terms of RMS jitter:

$$\sigma_{\tau out} = \frac{1}{N}\sqrt{\frac{\int_0^{B_{FD}} |H(jf)|^2 df}{B_{FD}}}\sigma_\tau \,. \tag{3.12}$$

Expression (3.12) shows that, in worst case, all the FD jitter can be passed through to the PLL output (when $B_{FD}<<B_{PLL}$, so that $|H(jf)|\approx N$ for frequencies [0, B_{FD}]). It also indicates that output jitter can be minimized by minimizing $|H(jf)|^2$, i.e. PLL loop bandwidth B_{PLL} (which in turn impairs dynamic characteristics of the PLL).

By dividing both sides of (3.12) by the nominal output period, T_{out}, an expression which shows relative RMS jitter, with respect to nominal input and output periods, can be found:

$$\frac{1}{T_{out}}\sigma_{\tau out} = \frac{1}{NT_{out}}\sqrt{\frac{\int_0^{B_{FD}} |H(jf)|^2 df}{B_{FD}}}\sigma_\tau \Rightarrow \frac{\sigma_{\tau out}}{T_{out}} = \frac{\sigma_\tau}{T_{in}}\sqrt{\frac{\int_0^{B_{FD}} |H(jf)|^2 df}{B_{FD}}}$$

and finally:

$$\sigma_{\tau out}[\%] = \sigma_\tau[\%]\sqrt{\frac{\int_0^{B_{FD}} |H(jf)|^2 df}{B_{FD}}} \,. \tag{3.13}$$

3.3. Example

As an example, consider a digital PLL whose linear model can be represented by the diagram in Fig. 3.2, with the following parameters [FLAPLL]:

K_P=5.03×10^{-6}A/rad

K_O=1.303×10^{10}Hz/V

N=16

$$F(s) = \frac{K_F(s+z)}{s(s+p)}$$

Parameters of the loop filter are:

K_F=1.97×10^{11}Ω

z=3.178×10^{6}rad/s

p=4.116×10^{7}rad/s

PLL transfer function is:

$$H(s) = \frac{NK_PK_OF(s)}{Ns + K_PK_OF(s)} = \frac{NK_PK_OK_F(s+z)}{N(s+p)s^2 + K_PK_OK_F(s+z)}$$

With these parameters, loop bandwidth of this PLL is about B_{PLL}=4.7MHz. Nominal frequency of the PLL input signal is f_{in}=100MHz (T_{in}=10ns) and, since N=16, frequency of the PLL output signal is f_{out}=1.6GHz (T_{out}=625ps). Plot of the PLL transfer function magnitude for natural frequencies, $|H(jf)|=|H(s)|_{s=j2\pi f}$, is shown in Fig. 3.6.

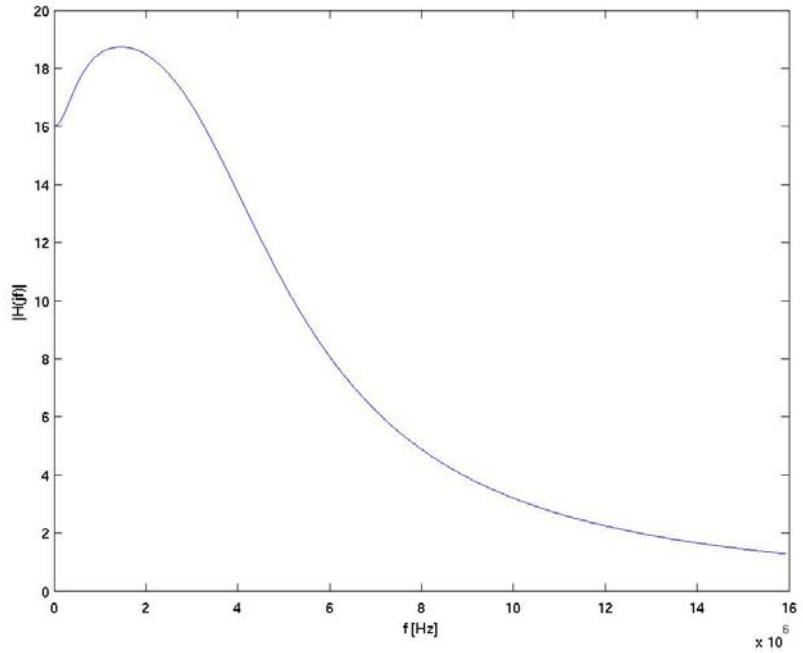


Fig. 3.6. Magnitude of the PLL transfer function from [FLAPLL]

Let us assume that the frequency divider inside the PLL generates jitter with a RMS value of σ_τ=100ps (1% of the nominal input period T_{in}, i.e. 0.01UI). The goal is to find the output RMS jitter caused by the FD, by using (3.12). If we assume that the bandwidth of the frequency divider is B_{FD}=200MHz (=$2f_{in}$), then by applying (3.12), output RMS jitter is $\sigma_{\tau out}$=20ps, or 3.2% of the nominal output signal period (i.e. 0.032UI).

We can see from this example, that even though the absolute amount of jitter at the PLL output is smaller than the amount of jitter generated by the FD, it occupies a larger portion of the output signal cycle. Therefore, we could say that there exists an "amplification" of the FD jitter by the PLL. When the FD division ratio N is high, which is the case in RF PLLs, this jitter amplification is even more pronounced. It should also be noted that the assumption that jitter and phase noise are uniformly distributed over a wide range of frequencies, [0, B_{FD}], is very optimistic. Noise will actually be concentrated around low frequencies (e.g. due to 1/f flicker noise), resulting in lower B_{FD}, which will, for the same σ_τ, cause increased $\sigma_{\tau out}$, according to (3.12). For these reasons, it is important to know the mechanisms by which FD generates jitter, as well as how to predict it and how to minimize it. Analytical model for FD jitter will help with these tasks and that is the main motivation for this research.

Section 4:

General properties of FD jitter

Before we start analyzing how device noise inside the CML frequency dividers transforms into jitter, let us study some general properties of FD jitter. These properties are not characteristic for CML implementation of FD only, but are common for a broad range of different FD implementations. Therefore, the analysis presented in this section is the analysis on the block-level, as opposed to the jitter analysis on the circuit-level, which will be presented in Section 5. Assuming that we know the amount of jitter generated by one FD stage (or one FD sub-block), we want to see how jitter propagates through a multi-stage FD, how each FD stage affects jitter of the adjacent stages, how jitter affects the maximum toggling rate of the FD etc. This analysis will give us an insight into methods for minimizing FD jitter on the FD block-level.

4.1. Jitter of asynchronous multi-stage FD

Current-mode logic (CML) frequency dividers are asynchronous counters. A block diagram of an asynchronous frequency divider by N is shown in Fig. 4.1. The frequency divider consists of n stages, each stage dividing frequency by two. Therefore, frequency division factor N is $N=2^n$.

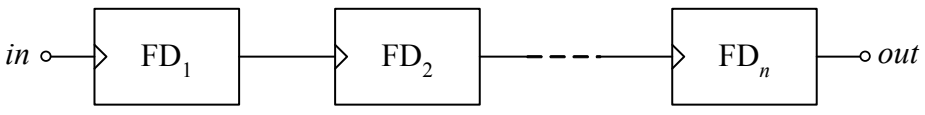


Fig. 4.1. Asynchronous frequency divider by N ($N=2^n$)

Let us first assume that all the stages FD_1 through FD_n are ideal and do not contain any noise sources, but input signal *in* contains jitter with the RMS value of $\sigma_{\tau in}$. Let us also assume that the FD output signal RMS jitter is $\sigma_{\tau out}$. FD stages cannot cause any jitter, therefore, jitter that occurs at the output must originate from the input. To find the portion of jitter that is passed through from the input to the output, let us observe one stage of the frequency divider, FD_i:

Each stage of the frequency divider is implemented as a T-flip-flop. Output of a T-flip-flop changes its state after an arrival of the active edge of the input signal (active edge can be either rising or falling edge). A transition of the output occurs a propagation delay time after the occurrence of the active edge of the input signal. If there are no noise sources in the flip-flop, the propagation delay time is constant. Therefore, if there is some jitter in the input signal, the same amount of jitter will be passed through to the output of the flip-flop. An equation which relates jitter powers at input and output of the i^{th} stage when that stage does not generate jitter can be written:

$$\sigma_{\tau i}^2 = \sigma_{\tau i-1}^2 \qquad i=1..n\text{-}1, \text{ with } \sigma_{\tau n}=\sigma_{\tau out} \text{ and } \sigma_{\tau 0}=\sigma_{\tau in}. \tag{4.1}$$

In the equation above, σ_τ is the RMS jitter.

If we now assume that each frequency divider stage contains noise sources which generate jitter with a RMS value of $\sigma_{\tau 1}$ at its output, then equation (4.1) needs to be modified. Now, output jitter power of the i^{th} stage is a sum of the input jitter and the jitter generated by the stage itself:

$$\sigma_{\tau i}^2 = \sigma_{\tau 1}^2 + \sigma_{\tau i-1}^2. \tag{4.2}$$

It was assumed in (4.2) that input jitter and jitter generated by the FD stage are not correlated. Therefore, their variances add rather than their RMS values.

Applying (4.2) on each stage of the frequency divider from Fig. 4.1, starting from the last, n^{th} stage, an equation which gives jitter power of the FD output signal is:

$$\sigma_{\tau out}^2 = \sigma_{\tau in}^2 + n\sigma_{\tau 1}^2 . \tag{4.3}$$

In this case, it was assumed that jitter generated by different FD stages is not correlated. An analysis similar to this was presented in [Egan91], but the signal uncertainties were represented as phase noise (phase- or frequency-domain uncertainty), rather than jitter (time-domain uncertainty).

In case when each stage of the frequency divider contributes to the output jitter with a different amount of jitter, equation (4.3) has to be modified:

$$\sigma_{\tau out}^2 = \sigma_{\tau in}^2 + \sigma_{\tau FD}^2 \tag{4.4}$$

where $\sigma_{\tau FD}$ is the effective output RMS jitter of the entire n-stage frequency divider. Equation (4.4) is more general than (4.3), and it holds for both asynchronous and synchronous frequency dividers.

From (4.3), it can be seen that the output jitter power increases linearly with the number of frequency divider stages. As an example, in PLLs used in 10Gbps transceivers, frequency dividers typically have n=6 stages in order to achieve ~10GHz PLL output frequency, using a ~150MHz crystal quartz oscillator as a reference signal (division factor is then $N=2^6=64$). A frequency divider with such a large number of stages can generate a significant amount of jitter [Haji01].

4.2. Cycle and absolute FD jitter

When deriving (4.4), we did not specify whether the jitter values that appear in the equation signify absolute (long-term) or cycle jitter. The equation holds for both types of

jitter, but we will now show that jitter that originates from the FD itself has the same value, whether it is observed as the absolute or cycle jitter. In other words, FD-generated RMS jitter $\sigma_{\tau FD}$ remains constant with time.

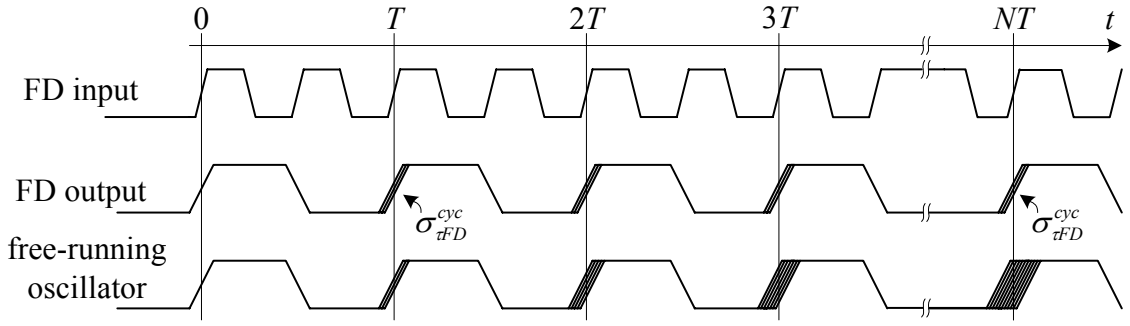


Fig. 4.2. Absolute jitter of a FD driven by an ideal input signal, and a free-running VCO

Let us observe a noisy frequency divider with an ideal input signal. Such input signal does not introduce any jitter to the system ($\sigma_{\tau in}$=0 in (4.4)), and all the jitter that occurs at the FD output comes from the FD itself. Definitions of absolute and cycle jitter were given in (2.1) and (2.2), respectively, but will be repeated here for convenience:

Absolute jitter: $$\sigma_\tau^{abs} = \sigma_\tau^{abs}(N) = \lim_{M\to\infty}\sqrt{\frac{1}{M}\sum_{m=1}^{M}\left(NT_m - NT\right)^2} \qquad (4.5)$$

Cycle jitter: $$\sigma_\tau^{cyc} = \lim_{M\to\infty}\sqrt{\frac{1}{M}\sum_{m=1}^{M}\left(T_m - T\right)^2} \qquad (4.6)$$

We will now show that (4.5) and (4.6) yield the same results for jitter, in case of a FD driven by an ideal input source:

The output of the FD switches only after a positive transition of the input signal, as illustrated in Fig. 4.2. The ideal input is a reference which does not allow the FD output to wander and it resets the timing of the output signal after every occurrence of the positive transition of the input. Therefore, when determining the absolute jitter at time $t=NT$ in (4.5), we can assume that the previous N-1 cycles of the FD output were ideal,

and only the last one is affected by FD noise. Then, arrival time of the N^{th} rising edge happens at

$$NT_m = (N-1)T + T_{m,N} \tag{4.7}$$

where $T_{m,N}$ is the duration of the N^{th} cycle of the FD output signal, in the m^{th} measurement. Applying (4.7) in (4.5), (4.5) reduces to (4.6) and therefore, we can conclude that the FD cycle and absolute jitter are the same (i.e. $\sigma_{tFD}^{abs} = \sigma_{tFD}^{cyc} = \sigma_{tFD}$).

As opposed to that of a frequency divider, absolute jitter of a free-running oscillator increases with time, since the system is autonomous, and there is no reference signal to adjust the timing. This is illustrated in Fig. 4.2, which shows jitter of a free-running oscillator, with the same output frequency as the frequency of the FD. Any uncertainty of the signal transition in the current cycle affects all the following transitions and its effects accumulate [Haji99, McNe97].

Absolute jitter of the frequency divider output signal can also increase with time, but only if that is caused by the FD input signal.

4.3. Effects of the FD structure on jitter

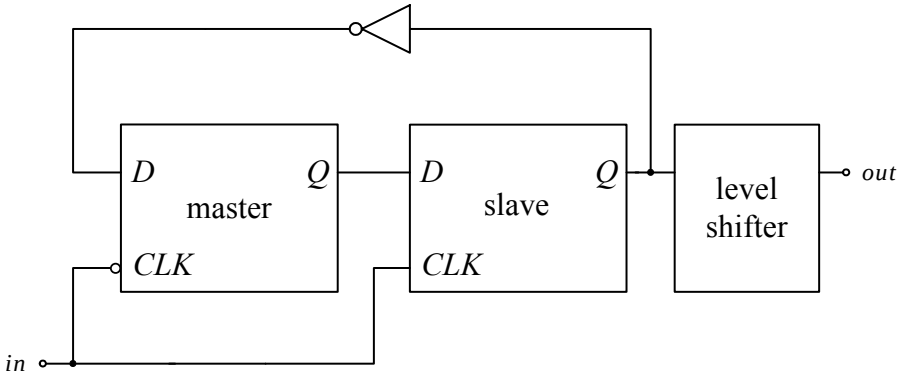


Fig. 4.3. Frequency divider by two (CML T-flip-flop)

Using the CML design technique, each frequency divider by two (i.e. T-flip-flop) in Fig. 4.1 is implemented using a master-slave latch whose inverted output is fed back to its input, and a level-shifter at the output, as shown in Fig. 4.3 (CML technique uses low-swing differential signaling, but only single lines are shown in Fig. 4.3 for simplicity. Also, inverter shown in the feedback path does not exist in the real implementation because signal inversion can be achieved by properly connecting differential input/output ports of the latches). In Fig. 4.3, master latch is transparent while input signal *in* is in its 'low' phase, and slave latch is transparent during the 'high' phase of the input. The level-shifter is needed to adjust the DC level of the output signal so that it can be used to clock the following stage (another divider by two). Output of the slave latch changes only after the rising edge of the input (i.e. rising edge is the active edge for this master-slave latch). Therefore, only jitter of the rising edge of the input signal will be passed through to the frequency divider output, while jitter of the falling edge will be suppressed by the frequency divider, as shown in Fig. 4.4. This fact needs to be accounted for when using (4.1) through (4.4) for multi-stage frequency dividers.

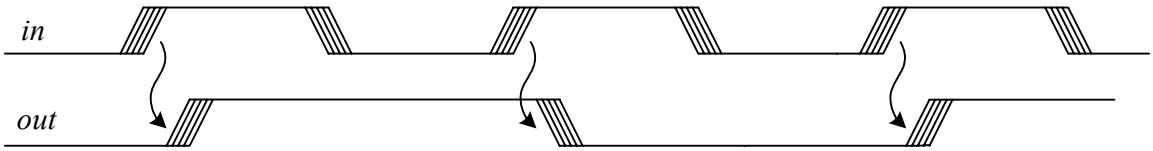


Fig. 4.4. Input and output waveforms of the frequency divider-by-two input

In order to confirm these conclusions, the following experiment was conducted:

An actual CML frequency divider stage was simulated in HSPICE. The arrival times of both rising and falling edges of the input signal (*in* from Fig. 4.3) were varied from their nominal values, and offset in the arrival time of the FD output signal *out* was measured. Results are shown in Fig. 4.5. Solid line shows that jitter of the rising (active) edge of the

input causes the same amount of output jitter (i.e. input-output jitter transfer function is one), while jitter of the falling edge of the input does not cause any jitter at the output, as shown by the dotted line (input-output jitter transfer function is zero). This experiment also confirms relationship (4.1).

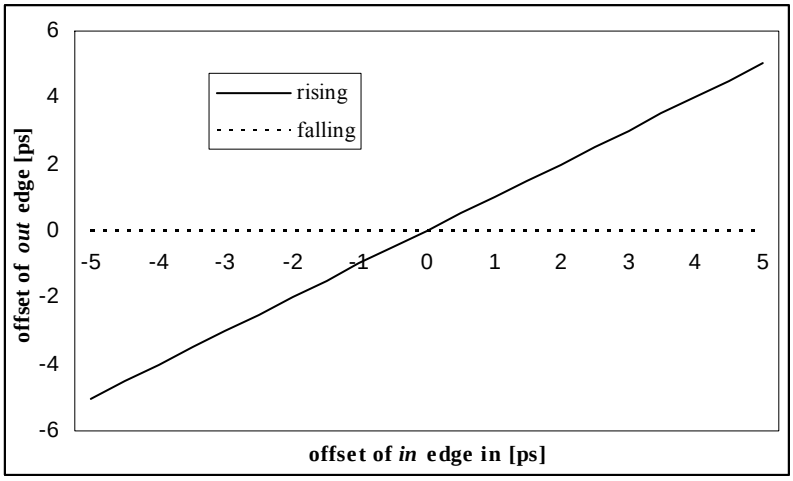


Fig. 4.5. Input jitter propagation

Another observation can be made by studying the structure of the FD by two in Fig. 4.3. First, it should be intuitively clear that device noise of a latch causes jitter only during transitions of the latch output signal (i.e. around the zero-crossing time of a differential signal). This will be studied in more details in Section 5 which proposes the analytical model for FD jitter. While output of the latch is stable (either 'low' or 'high'), noise causes small variations of the signal level, but these variations of the output voltage cannot be transferred into jitter. Fig. 4.6 shows output signals of the master and slave latches of the FD by two from Fig. 4.3. Master latch changes its value after every falling edge of the input signal *in*, and slave latch changes its state after every rising edge of *in*. It is assumed that noise sources exist only in the master latch, causing its output signal to be non-ideal. However, when slave latch samples the master output (at time instants $k \times t_S$,

k=1,2,…), master latch is either in the 'high' or 'low' state, and these states will be sampled correctly (level variations will be suppressed by the slave latch). Therefore, device noise in the master latch will not cause any jitter at the output of the slave latch, and hence, at the output of the FD.

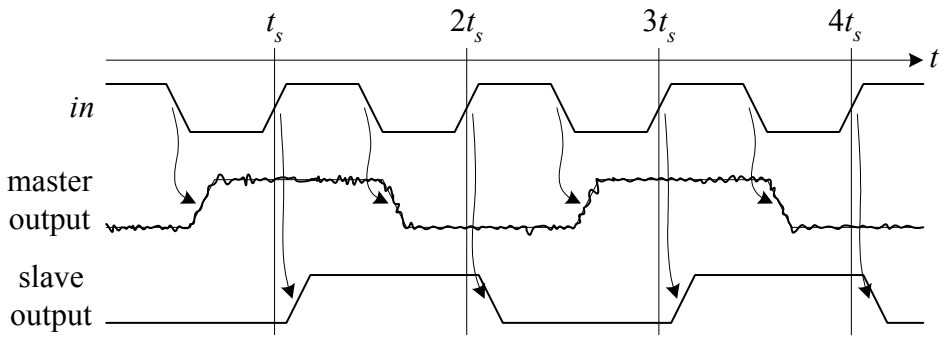


Fig. 4.6. Signal waveforms of the master-slave latch from Fig. 4.4.3

To prove these observations, another experiment was conducted:

One-stage FD without level-shifter was simulated in HSPICE, with two current sources, i_{nM} and i_{nS}, connected to the outputs of master and slave latches respectively, as shown in Fig. 4.7. These current sources simulate output-referred device noise of master and slave latches, respectively. Fig. 4.8 shows eye-diagrams of the *out* signal, when only i_{nS} is active (Fig. 4.8a), and when only i_{nM} is active (Fig. 4.8b). It can be seen from Fig. 4.8 that only i_{nS} (i.e. device noise from the slave latch) causes jitter at the FD output: there is a significant zero-crossing time variation in case when only i_{nS} is active, while zero-crossing time when only i_{nM} is active practically remains constant. It should be mentioned that in these simulations, sources i_{nM} and i_{nS} were sets of current pulses with variable arrival times, rather than real noise sources (this was the easiest way of simulating noise sources in HSPICE).

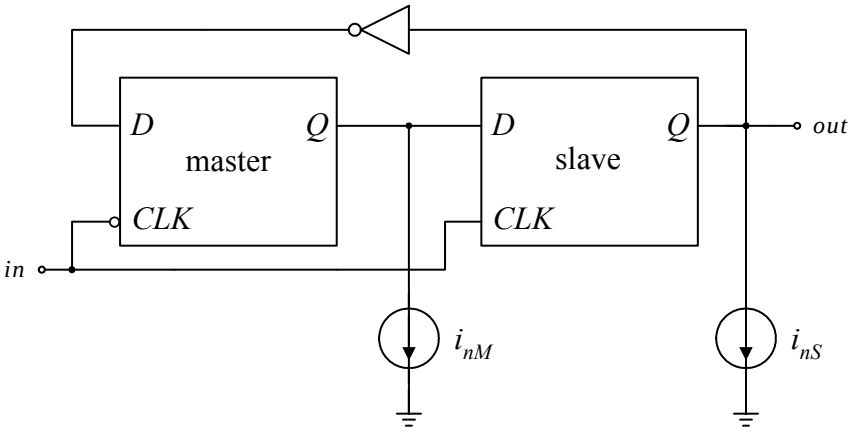


Fig. 4.7. Simulation setup for the analysis of jitter generation by master and slave device noise

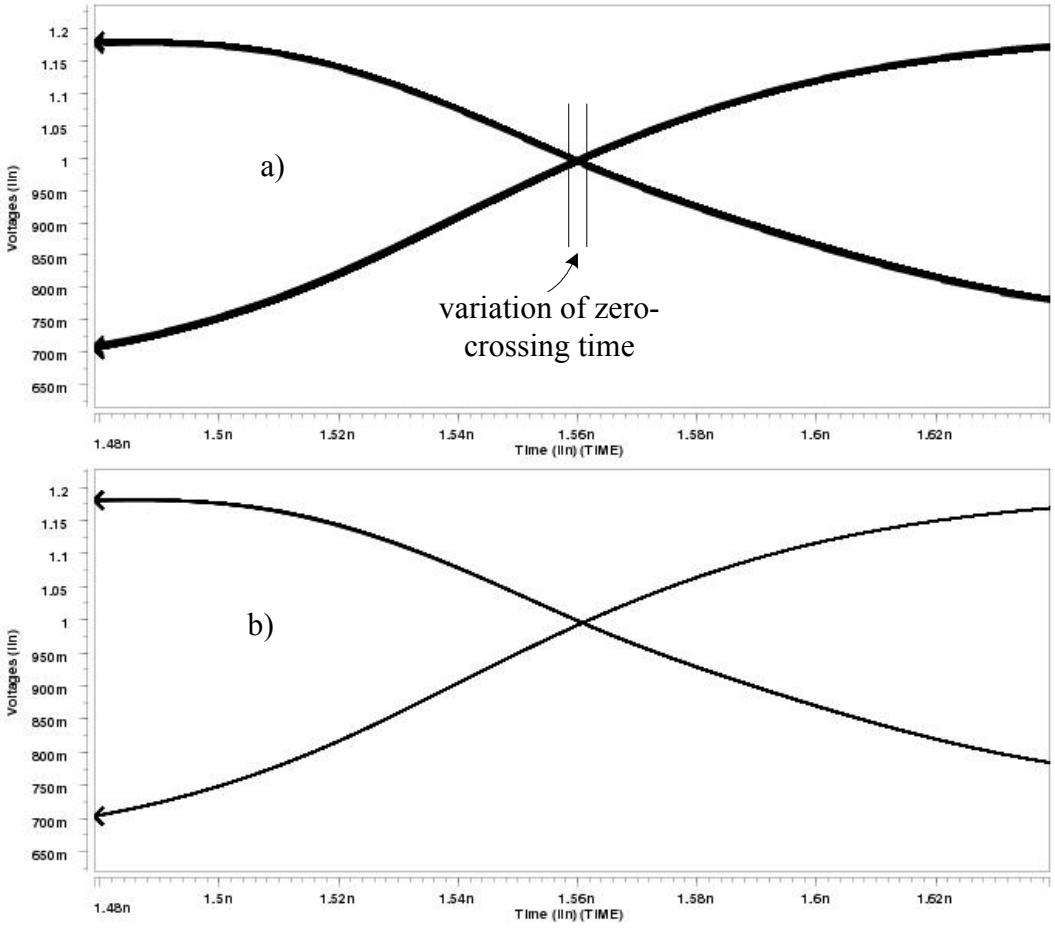


Fig. 4.8. Zoomed-in eye-diagram of the output of FD from Fig. 4.7:

a) when only noise in the slave latch is present (i_{nS} from Fig. 4.7 is active) and

b) when only noise the master latch is present (i_{nM} from Fig. 4.7 is active)

Level-shifter was not included in the circuit in Fig. 4.7. However, it also contributes to the FD output jitter. The level-shifter is usually a source-follower. If the RMS jitter generated by the master-slave latch (more precisely slave latch) is $\sigma_{\tau MS}$ and the RMS jitter generated by the level-shifter is $\sigma_{\tau LS}$, FD stage output jitter power is:

$$\sigma_{\tau out}^2 = \sigma_{\tau MS}^2 + \sigma_{\tau LS}^2 \tag{4.8}$$

which can be concluded from Fig. 4.3. It was assumed in (4.8) that noise sources in the slave latch and level-shifter are not correlated.

A consequence of these observations is that, when designing a FD stage, less attention can be paid to designing the master latch. On the other hand, slave latch and the level-shifter should be designed more carefully.

Finally, it should be noted that, even though the above analysis deals with the CML implementation of FD, results are more general because master-slave implementation of the T-flip-flop from Fig. 4.3 (but usually without the level-shifter) is applied when design techniques other than CML are used.

4.4. Impact of jitter on the maximum input frequency of a FD

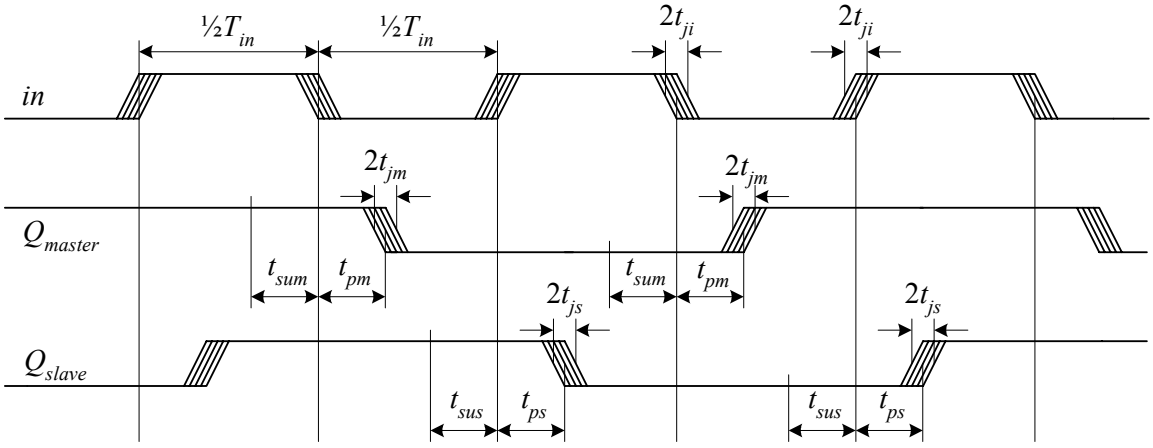


Fig. 4.9. Waveforms for determining maximum toggle frequency of the first frequency divider stage

The maximum frequency of the signal that can be applied to the inputs of the multi-stage frequency divider in Fig. 4.1 is limited by the characteristics of the first divide-by-two stage, since this stage toggles at the maximum rate. Jitter generated in this FD stage, in addition to the jitter of the input signal, will impose the margins to the minimum period of the input signal that can be applied. The first FD stage will fail when setup time violation of the master-slave latch occurs (setup time of a latch is the minimum time before the arrival of the active edge of the clock signal *CLK*, for which data input *D* has to be stable, in order for latch to capture the data input correctly [Stoj99], see Fig. 4.3). The minimum input period can be determined from the waveforms in Fig. 4.9. Parameters in Fig. 4.9 are the following: T_{in} is the period of the input signal; t_{ji} is the jitter of the input signal; t_{jm} and t_{js} are the total jitter values of the master and slave latches, respectively; t_{pm} and t_{ps} are the clock-to-output propagation delay times of the master and slave latches, respectively; t_{sum} and t_{sus} are the setup times for the master and slave latches, respectively. As shown in Fig. 4.9, it was assumed that the parameters are identical for both rising and falling edges of the signals, but they may differ for master and slave latch. Using the diagrams from Fig. 4.9, equation for the minimum period of the input signal can be set:

$$\tfrac{1}{2} T_{in}^{\min} = \max\left\{\left(t_{ji} + t_{ps} + t_{js} + t_{sum} + t_{ji}\right), \left(t_{ji} + t_{pm} + t_{jm} + t_{sus} + t_{ji}\right)\right\} \qquad (4.9)$$

In equation (4.9), the first expression under the ‘max’ operator is the condition which ensures that there is no setup time violation for the master latch, and the second expression ensures that there is no setup time violation for the slave latch. Therefore, when determining the minimum period of the input signal, jitter of the input signal as well as jitter generated by the master and slave latches should be known, in order to set

the margin for the minimum input period. The margins imposed by jitter are $2(2t_{ji}+t_{js})$ or $2(2t_{ji}+t_{jm})$, depending on which expression in (4.9) is critical.

4.5. FD jitter as a function of output capacitance

When frequency divider in Fig. 4.1 is implemented using standard CMOS process (which is the case when CML design technique is used), each stage of the FD sees the following stage as a capacitive load at its output. We will now show that jitter performance of the entire FD depends on the relative sizing of the FD stages, since jitter of each stage depends on the capacitive load introduced by the following stage.

In order to study dependence of FD output jitter on its output capacitance, we need to know the exact analytical model for the FD jitter. Therefore, this analysis will be revisited once the analytical model is derived. In this section, however, we will just try to introduce some general ideas how output capacitance affects jitter.

As mentioned in the previous section, device noise can affect output jitter only during the transitions of the output. When the output signal level is stable ('high' or 'low'), noise can vary the level of the signal, but this cannot affect the zero-crossing time and cause jitter. Only noise sources which act around the zero-crossing time (i.e. during output signal transitions) are going to generate jitter. As the output load capacitance of the FD stage increases, if the stage size (sizes of the devices in the FD stage) remains unchanged, transition time of the output signal will increase proportionally with the output capacitance. Therefore, time window in which the circuit is sensitive to noise increases, and jitter should also increase.

Results of an experiment which investigates dependence of the zero-crossing time variation on the FD output load are presented in Fig. 4.10. The test setup for this experiment was the same one from Fig. 4.7, but in this case, only source i_{nS} was active (since we concluded that i_{nM} does not contribute to output jitter). Also, FD stage was loaded with a variable capacitance C_{out}. As in the previous experiment, source i_{nS} was a set of current pulses with different arrival times, and the average variation of the zero-crossing time of the output signal was measured. Figure 4.10 shows normalized measurement results. As shown in Fig. 4.10, average zero-crossing time variation increases with the output load. For C_{out}=0, parasitic capacitances of the FD stage itself are dominant, and therefore, zero-crossing time variation is not zero.

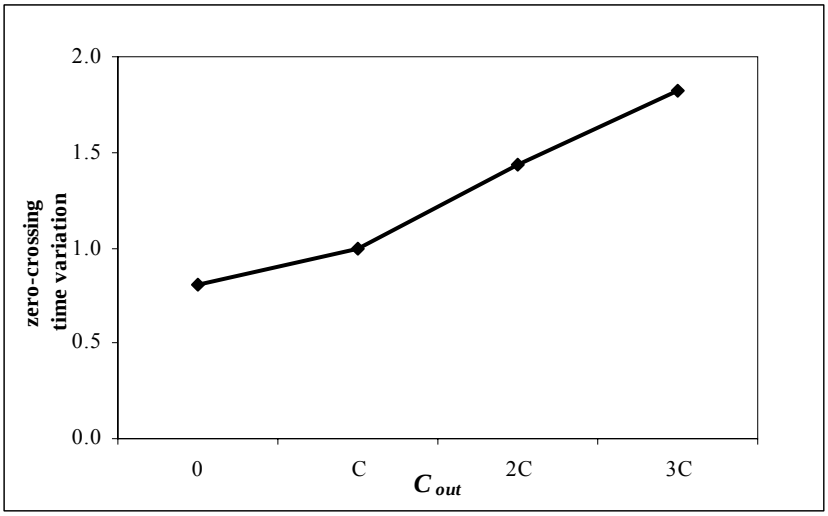


Fig. 4.10. Dependence of the average zero-crossing time on FD output load

Knowing effects of output load on FD jitter, a few conclusions can be drawn and some design implications can be given. First, as mentioned in the previous section, device noise in the master latch of a FD stage does not affect jitter and less attention can be paid to designing this latch. Moreover, master latch introduces a capacitive load to the slave latch output. Therefore, in order to reduce jitter at the FD output, a designer should minimize

the size of the slave latch. Another observation can be made regarding relative sizing of stages in the multi-stage FD from Fig. 4.1. It may be possible to find a method for optimal relative sizing of the FD stages in order to achieve minimum jitter of the entire FD. This method would be similar to the logical effort method used for delay minimization in digital logic [Suth91]. In case of jitter minimization, two opposing parameters would be the size of a CML FD stage (capacitive load which increases jitter of the previous stage), and gain of the stage (decreasing the stage size decreases its gain). Deriving the optimization method is beyond the scope of this research, but it could become a part of future research.

Section 5:

The proposed analytical model for CML FD jitter

Having an analytical model for CML FD jitter is important for several reasons. First, once the jitter model is known, it will be possible to predict jitter performance before the circuit is fabricated. Therefore, whether the system meets the design specifications can be determined in the pre-silicon phase of the design process. Beside that, the model will establish relationships between circuit parameters and jitter. Knowing this dependence, it will be possible to find which circuit parameters are the most important contributors to the FD jitter, and this will help finding a design strategy for jitter reduction: the ultimate goal is to develop a very-low jitter frequency divider.

5.1. FD jitter analysis: state-of-the-art

As mentioned in the introductory section, there is not much work published in the area of FD jitter and phase noise analysis. Some efforts to characterize FD jitter and phase noise are presented in [Egan90, Egan91, Dris90, Dris92, Krou01]. [Egan90, Egan91 and Krou01] use jitter and phase noise measurements of a series of frequency dividers available at the time, and attempt to formulize a FD phase noise model by extrapolating the data. [Dris90 and Dris92] show only phase noise measurements of two types of analog frequency dividers. None of these papers shows a relationship between jitter or phase noise performance and circuit parameters, and hence, cannot offer any guidelines on how to design a low-jitter FD.

5.2. CML FD implementation

Since jitter generation is closely related to the actual realization of the CML FD circuit (jitter is caused by device noise), first we need to study the FD circuit implementation. Block diagram of a CML frequency divider by two is shown in Fig. 5.1. This block diagram is similar to the one given in Fig. 4.3, but is more closely related to the CML implementation. As shown in Fig. 5.1, master-slave latch and the level-shifter are biased with a DC voltage V_{BIAS} and inversion in the feedback path is realized by cross-connecting differential inputs and outputs of the master-slave latch. Also, it can be seen that signals contain both DC and AC components (e.g. $v_{CLK}=V_{CLK}+v_{clk}$) and that differential signals have the AC components in the counter-phase.

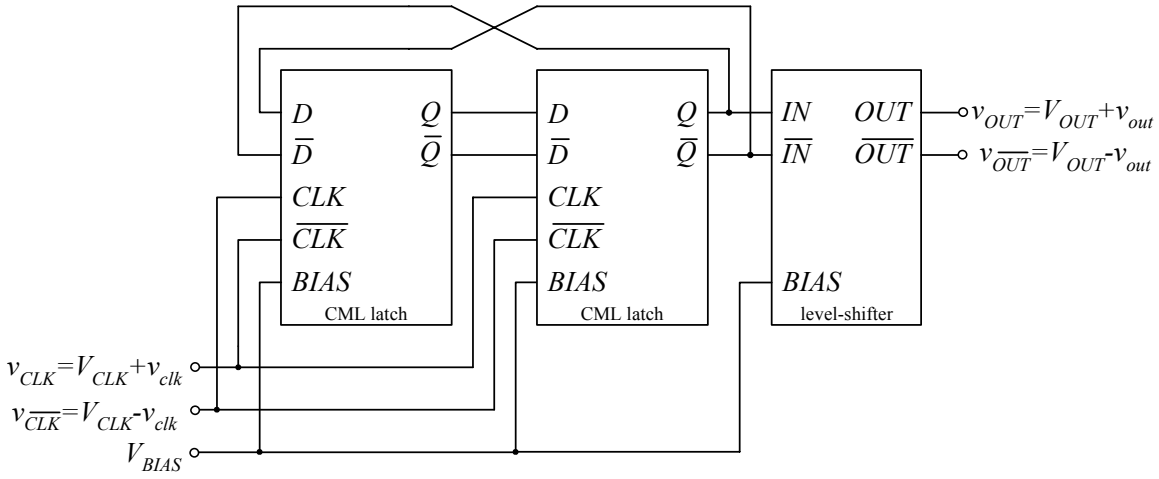


Fig. 5.1. Detailed block diagram of a CML frequency divider by two

Each CML latch from Fig. 5.1 is implemented as a circuit shown in Fig. 5.2. M_0 generates a constant current I_{BIAS} which is split between clock transistors M_1 and M_2 (M_1 and M_2 are identical). Since the current gain of the M_1-M_2 pair is high, when signals *CLK* and $\overline{CLK}$ are stable, only one of the transistors in the pair is active (in saturation). When *CLK* is 'high', another transistor pair, M_3-M_4, will stir the current I_{BIAS} coming through

M_1, and set the outputs of the latch depending on the input signals D and $\overline{D}$. This value will be kept by the cross-coupled transistors M_5 and M_6, while *CLK* is 'low'. Transistors M_3, M_4, M_5 and M_6 are all identical.

It should be noted that resistors R_Q and $R_{\overline{Q}}$ are usually implemented using PMOS devices in the linear region, rather than poly or silicide resistors, due to the large tolerance of the on-chip resistors (up to 30%) in some processes.

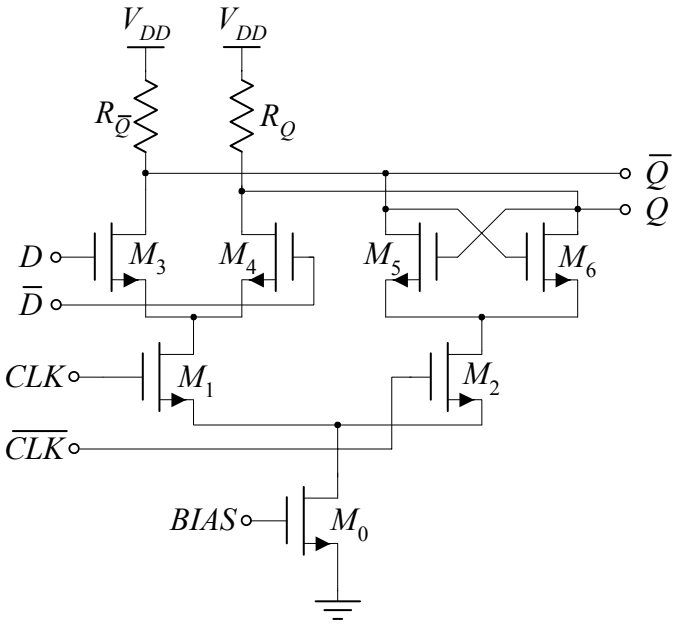


Fig. 5.2. Schematic of the CML latch

Schematic of the level-shifter is given in Fig. 5.3. The function of the level-shifter is to adjust the FD output level to the FD input level (i.e. V_{CLK}=V_{OUT} in Fig. 5.1), so that another FD stage can be driven. Level-shifter consists of two current sources, M_0 and M_2, and two source-followers, M_1 and M_3. Implementation of level-shifters may vary from the one in Fig. 5.3: for instance, a differential amplifier can be placed in front of the level-shifter, to provide additional signal gain (source-followers have voltage gain less than one).

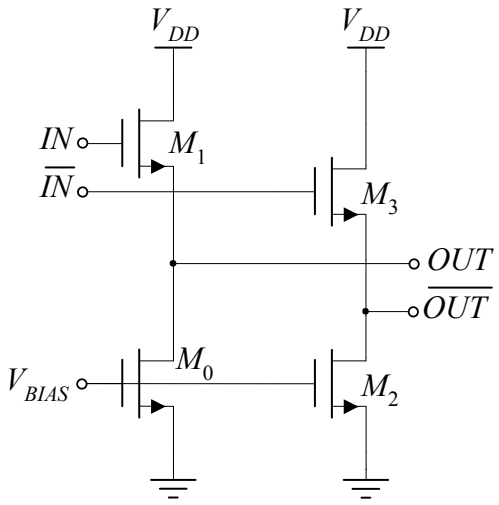


Fig. 5.3. Schematic of the level-shifter

In order to compare analytical results with simulations, one-stage CML frequency divider was designed using Fujitsu 0.11μm process with V_{DD}=1.2V. Simulated waveforms of this circuit are presented in Fig. 5.4, which shows input signals v_{CLK} and $v_{\overline{CLK}}$, and output signals of the master-slave latch, v_Q and $v_{\overline{Q}}$, before lowering the DC levels in the level-shifter.

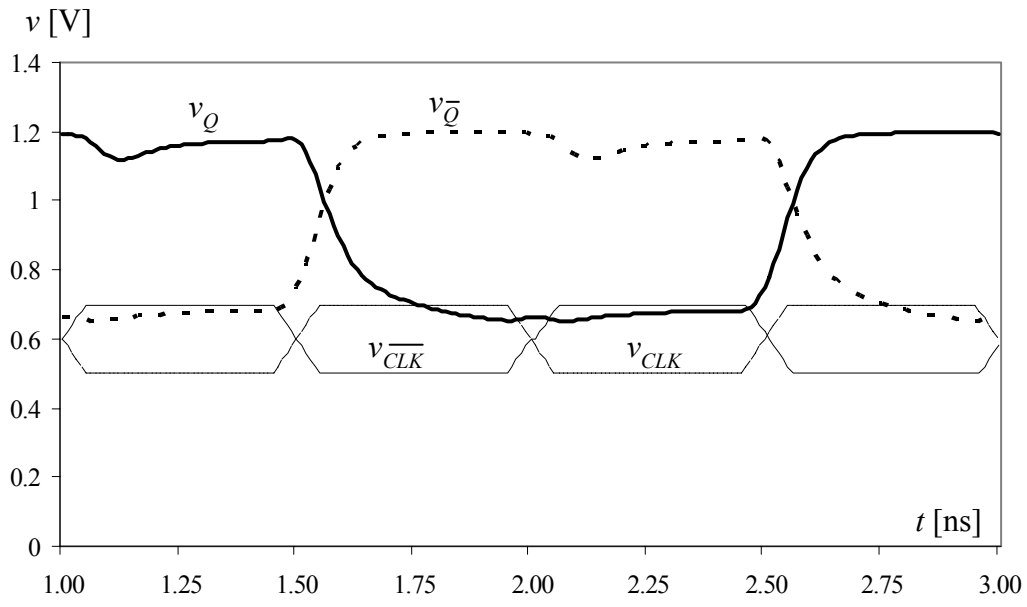


Fig. 5.4. Waveforms of the simulated CML FD without level-shifter

The FD takes the 1GHz input signal and outputs a signal whose frequency is 500MHz. DC level of the input signal is V_{CLK}=0.6V, and master-slave latch output DC level is V_Q=1V. Therefore, level-shifter is needed to lower the FD output DC level from 1V to 0.6V.

Some important design parameters of the CML latch, that are going to be used for comparison of the analytical model with simulations, are summarized in Table 5.1:

Table 5.1. CML latch circuit parameters

Design parameter	Symbol	Value
DC biasing current (drain current of M_0)	I_0	200μA
Output capacitance	$C_Q \equiv C_{\overline{Q}}$	22fF
Output resistance	$R_Q \equiv R_{\overline{Q}}$	2.45kΩ

5.3. Linear time-variant nature of jitter generation

The analytical jitter model proposed here is based on the linear time-variant (LTV) jitter and phase noise models for electric oscillators, which were first derived in the 1960s [Kuro68]. The main idea behind the LTV approach is that noise-to-jitter transfer function is time-dependent. More precisely, jitter generation is closely related to the oscillator output waveform. The approach was revived in the 1990s [Okum90, Okum93, Okum97]. In [Okum90], a simple SPICE-based simulator that performs a periodic small-signal analysis was implemented: the tool performs frequency (AC) analysis at each value of the periodically-varying operating point. Recently, the same feature was embedded in a Cadence simulator, Spectre [SpecRF]. However, LTV approach received more attention only after publishing of [Haji98]. While previous works focused on methods for numerical analysis of oscillator phase noise that is suitable for computer-aided design,

this work attempted to develop a general theory of oscillator phase noise. Supposedly, this theory should be valid for any kind of electric oscillators (LC, ring oscillators, etc), and it should give design guidelines for lowering phase noise. This work also received a lot of critiques because, in some parts, random nature of noise was neglected [Demi00].

Another important property of the LTV phase noise models is the cyclostationary nature of noise sources: not only the noise-to-jitter transfer function is time-variant, but also are the noise sources. Since the operating point varies periodically, statistical properties of noise also vary periodically.

The FD jitter model proposed here was inspired by the oscillator jitter and phase noise analyses presented in [McNe97] and [Haji98]. Improvements of the proposed model over these analyses will be discussed at the end of this section, after the model is presented.

5.4 The proposed CML FD jitter model

The FD jitter model presented here is still in its developing stage. It is just a simplified version of the future FD jitter model.

5.4.1. Assumptions and approximations

In order to simplify the FD jitter model, some assumptions and approximations need to be established. In future research, some of these approximations can be eliminated.

I. In these preliminary analyses, we will assume that only stationary, white noise is present in the FD circuit. This means that samples of each noise source, at different time instants, are not correlated. Furthermore, we will assume that different noise sources in the circuit are not correlated. In all realistic circuits, especially those

implemented in CMOS technology, flicker (1/*f*) noise is present, but effects of this type of noise can be accounted for later in the research. When flicker noise is present, assumption that samples of a noise source are uncorrelated does not hold anymore.

II. The second assumption is that, in a multi-stage frequency divider, each stage contributes to the total output jitter with the same amount of RMS jitter. Then, total output jitter power can be found using equation (4.2). With this assumption, jitter generation of only one FD stage needs to be analyzed in the following discussion.

III. In order to simplify the analysis even further, as we saw in Section 4, we can study effects of the master-slave latch noise and level-shifter noise separately. Furthermore, only jitter caused by noise sources in the slave latch should be accounted for in the master-slave latch jitter calculations, as shown in the same section. Total jitter of the FD stage can then be found using (4.4) from that section.

IV. It will be assumed that outputs of the master-slave latch, Q and $\overline{Q}$, start switching immediately after the arrival of the rising *CLK* edge. Clock signals, *CLK* and $\overline{CLK}$ will be approximated by perfect pulses with very sharp slopes and a relative phase shift of 180°. Outputs of the master-slave latch switch with the maximum slew-rate of the CML latch, which depends on the DC biasing current and output capacitance.

5.4.2. Master-slave latch jitter generation

To analyze jitter generated by the master-slave latch, we will study effects of a current source $i_n(t)$, connected to the Q output of the slave latch, as shown in Fig. 5.5, on variations of the crossing time of the slave latch outputs, $v_Q(t)$ and $v_{\overline{Q}}(t)$. Source $i_n(t)$

models the equivalent output-referred noise from devices in the slave latch, summed at node Q. As concluded in Section 4 and according to assumption III, there is no need to analyze effects of the master latch noise. Once we know how noise at node Q affects output jitter, we can use symmetry of the latch circuit to find effects of the equivalent noise source acting at node $\overline{Q}$.

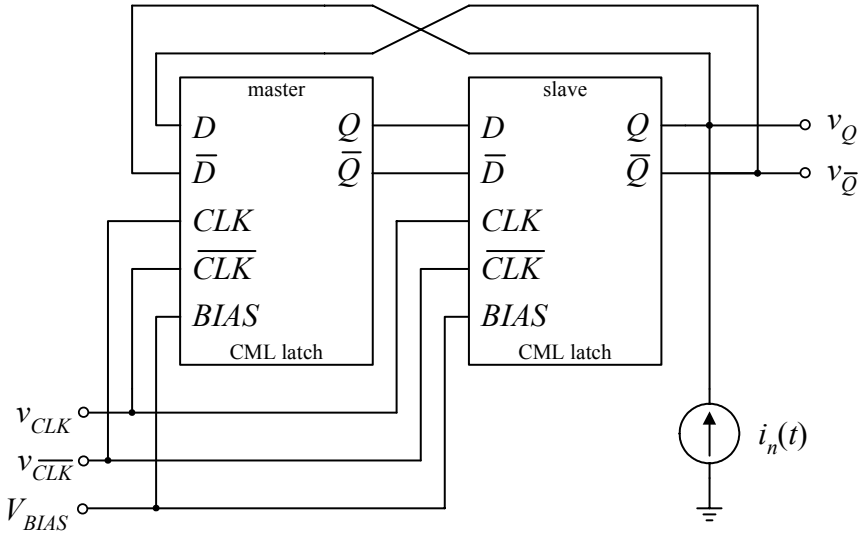


Fig. 5.5. Circuit used to study effects of the slave latch noise on output jitter

As mentioned earlier, noise-jitter transfer function is closely related to the output waveform. Fig. 5.4 shows waveforms of the simulated FD stage, without a level-shifter at the output. To simplify the analysis, we can approximate the FD output waveforms using assumption IV. Then, the idealized waveforms look like in Fig. 5.6.

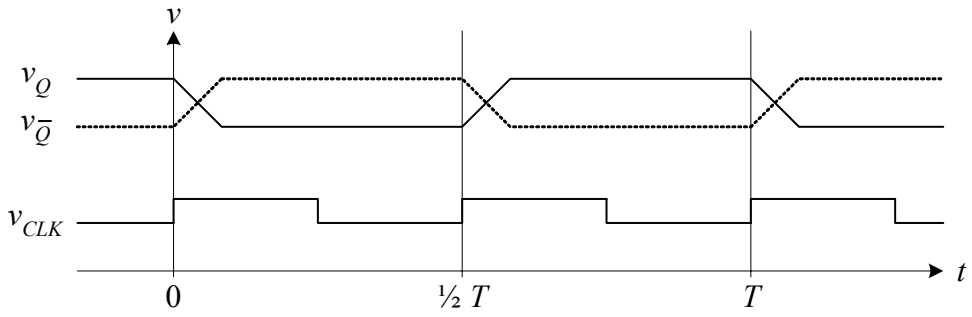


Fig. 5.6. Simplified waveforms from Fig. 5.5, using approximation IV

To see how noise transforms into jitter, let us observe output waveforms from Fig. 5.6, zoomed-in around t=0 (Fig. 5.7). When noise is not present, $v_Q(t)$ and $v_{\overline{Q}}(t)$ from Fig. 5.7 can be described by the following equations, for $t \in [0, 2t_d]$:

$$\begin{aligned} v_Q(t) &= V^+ - \frac{I_0}{C_Q} t \\ v_{\overline{Q}}(t) &= V^- + \frac{I_0}{C_{\overline{Q}}} t \end{aligned} \tag{5.1}$$

For $t < 0$, $v_Q(t) = V^+$ and $v_{\overline{Q}}(t) = V^-$. In (5.1), V^+ and V^- are the maximum and minimum master-slave output voltage levels, I_0 is the DC biasing current of the CML latch (drain current of M_0 from Fig. 5.2), and C_Q and $C_{\overline{Q}}$ are the total output capacitances at nodes Q and $\overline{Q}$ (due to circuit symmetry, $C_Q = C_{\overline{Q}}$). Using (5.1), nominal time when $v_Q(t)$ and $v_{\overline{Q}}(t)$ intersect, t_d, can be found as:

$$t_d = \frac{C_Q V_{SW}}{2I_0} = \frac{R_Q C_Q}{2}. \tag{5.2}$$

In (5.2), V_{SW} is the maximum voltage swing of the differential output ($V_{SW} = V^+ - V^-$) and R_Q is the slave latch output resistance at node Q, $V_{SW} = I_0 R_Q$ (see Fig. 5.2).

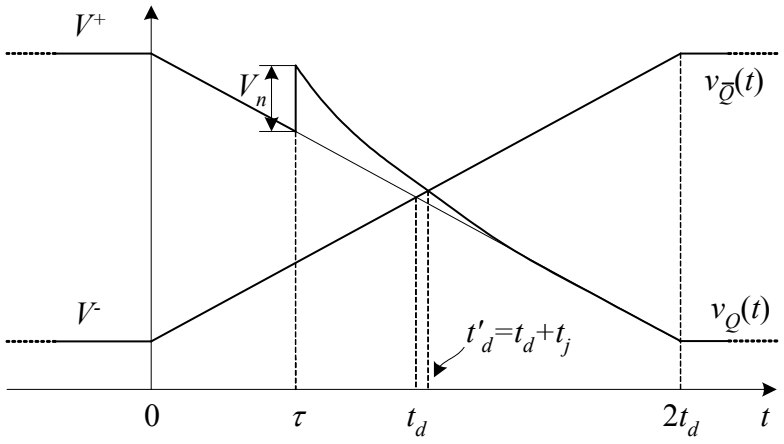


Fig. 5.7. Zoomed-in FD output waveforms

Let us now assume that noise source $i_n(t)$ is a current impulse, which occurs at time $t=\tau$. This current impulse causes injection of charge q_n at node Q, at time $t=\tau$. The injected charge will cause output voltage $v_Q(t)$ to abruptly increase by a value V_n, where $V_n=q_n/C_Q$ (Fig. 5.7). Effects of charge injection will start vanishing, following the exponential function, and $v_Q(t)$ for $t\in[\tau, 2t_d]$ can now be written as follows:

$$v_Q(t) = V^+ - \frac{I_0}{C_Q}t + V_n e^{-\frac{t-\tau}{R_Q C_Q}}. \tag{5.3}$$

Due to charge injection, zero-crossing time of the differential output voltage is changed and is now $t_d^{'}$. $t_d^{'}$ can be found by equating $v_Q(t)$ from (5.3) and $v_{\overline{Q}}(t)$ from (5.1). To simplify the calculations, we can approximate the exponential function with the first two terms of its Taylor series. The derivation of $t_d^{'}$ goes as follows:

$$v_Q(t_d^{'}) - v_{\overline{Q}}(t_d^{'}) = 0$$

$$V^+ - \frac{I_0}{C_Q}t_d^{'} + V_n e^{-\frac{t_d^{'}-\tau}{R_Q C_Q}} - V^- - \frac{I_0}{C_Q}t_d^{'} = 0$$

$$V_{SW} - \frac{2I_0}{C_Q}t_d^{'} + V_n - \frac{V_n}{R_Q C_Q}t_d^{'} + \frac{V_n}{R_Q C_Q}\tau = 0$$

$$t_d^{'} = \left(V_{SW} + V_n + \frac{V_n}{R_Q C_Q}\tau\right)\frac{1}{\frac{2I_0}{C_Q} + \frac{V_n}{R_Q C_Q}}$$

In the denominator of the term behind the parentheses, we can assume that

$$\frac{V_n}{R_Q C_Q} << \frac{2I_0}{C_Q}$$

which is a reasonable assumption since the voltage increase caused by noise V_n is expected to be much less than double the maximum voltage swing of the output:

$$\frac{V_n}{R_Q} << 2I_0$$

$$V_n << 2V_{SW}$$

Using this assumption, we can find $t_d^{'}$, the new crossing time of $v_Q(t)$ and $v_{\overline{Q}}(t)$:

$$t_d^{'} = \frac{C_Q}{2I_0}\left(V_{SW} + V_n + \frac{V_n}{R_Q C_Q}\tau\right). \tag{5.4}$$

Crossing time variation of the master-slave output, t_j from Fig. 5.7, can now be found by combining (5.4) and (5.2):

$$t_j = t_d^{'} - t_d = \frac{C_Q}{2I_0}\left(V_{SW} + V_n + \frac{V_n}{R_Q C_Q}\tau\right) - \frac{C_Q V_{SW}}{2I_0}$$

and finally

$$t_j = \frac{V_n C_Q}{2I_0}\left(1 + \frac{\tau}{R_Q C_Q}\right). \tag{5.5}$$

As expression (5.5) shows, zero-crossing time variation is proportional to τ, which is the moment when charge injection occurs. The closer the occurrence of charge injection to the nominal crossing time t_d, the more effects it has to the crossing time variation t_j. If the charge injection occurs after the crossing of the differential output, naturally, it will not affect the crossing time. Therefore, the upper limit for τ is $\tau_{max}=t_d$. The lower limit for τ is the value for which t_j reaches zero: $\tau_{min}=-R_Q C_Q=-2t_d$ (note that all the derivations above hold for $\tau < 0$). Therefore, range of interest is $\tau \in [-2t_d, t_d]$.

Let us now try to derive a noise-to-jitter transfer function. To do that, we need to describe effects expressed by (5.5) in a suitable mathematical form, i.e. we need to find a formal time-domain impulse response function of the "noise-to-jitter conversion system", and

then find the Laplace transform of that impulse response. First, we can use the relationship between V_n and the injected charge q_n, $V_n=q_n/C_Q$, and write t_j from (5.5) as:

$$t_j = \frac{q_n}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right). \tag{5.6}$$

Expression (5.6) shows response of the "noise-to-jitter conversion system" to the impulse excitation $q_n\delta(t-\tau)$: injection of q_n coulombs of charge at time $t=\tau$ will cause a crossing time variation of t_j seconds. To find the impulse response function, we need to describe the crossing time variation from (5.6) by some time-domain function. We can assume that, as a response to the current impulse, jitter occurs right after the arrival of the impulse, at $t=\tau$, and persists until the end of the current cycle, $t=T$. Assumption that impulse response ends at $t=T$ reflects the fact that, after the arrival of the new rising edge of v_{CLK}, retiming of the output signal occurs, and jitter generated around the previous rising edge of v_{CLK} (around $t=0$) does not propagate after $t=T$. Therefore, we can formally describe the impulse response as:

$$h_j(t,\tau) = h_j(t-\tau) = \frac{q_n}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\left[u(t-\tau)-u(t-T)\right],\ \tau\in[-2t_d,t_d] \tag{5.7}$$

Graphic representation of the impulse response function is shown in Fig. 5.8.

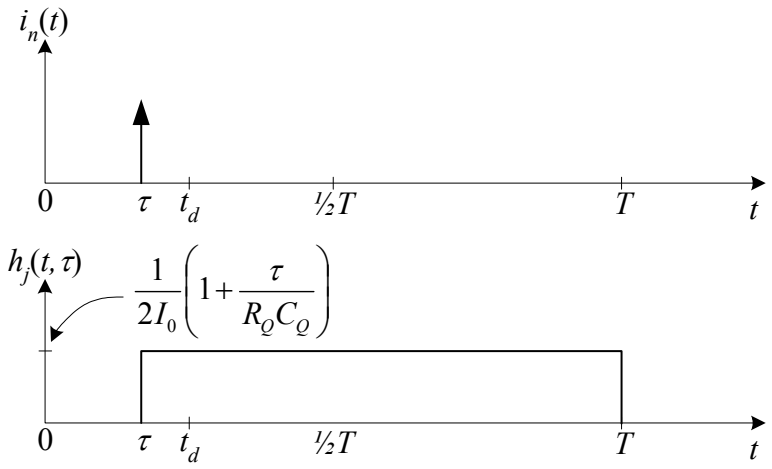


Fig. 5.8. Excitation $i_n(t)$ and impulse response function $h_j(t,\tau)$

We can now find a time-variant noise-jitter transfer function $H_j(s,\tau)$, as a Laplace transform of the impulse response $h_j(t,\tau)$:

$$\mathcal{L}\{h_j(t-\tau)\} = \mathcal{L}\left\{\frac{1}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\left[u(t-\tau)-u(t-T)\right]\right\}$$

$$H_j(s,\tau)e^{-s\tau} = \frac{1}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\frac{1}{s}\left[e^{-s\tau}-e^{-sT}\right]$$

$$= \frac{1}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\frac{1}{s}e^{-s\tau}\left[1-e^{-s(T-\tau)}\right].$$

Therefore,

$$H_j(s,\tau) = \frac{1}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\frac{1}{s}\left[1-e^{-s(T-\tau)}\right].$$

Substituting $s=j2\pi f$, we get $H_j(jf,\tau)$:

$$H_j(jf,\tau) = \frac{1}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\frac{1}{j2\pi f}e^{-j\pi f(T-\tau)}\left[e^{j\pi f(T-\tau)}-e^{-j\pi f(T-\tau)}\right].$$

$$= \frac{1}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\frac{1}{j2\pi f}e^{-j\pi f(T-\tau)}2j\frac{\left[e^{j\pi f(T-\tau)}-e^{-j\pi f(T-\tau)}\right]}{2j}$$

$$= \frac{1}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\frac{1}{\pi f}\sin\left(\pi f(T-\tau)\right)e^{-j\pi f(T-\tau)}$$

$$= \frac{1}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)(T-\tau)\frac{\sin\left(\pi f(T-\tau)\right)}{\pi f(T-\tau)}e^{-j\pi f(T-\tau)}$$

This can now be simplified using an assumption $T>>\tau$ for $\tau\in[-2t_d,\ t_d]$ (i.e. $T>>t_d$), yielding the final expression for the noise-jitter transfer function:

$$H_j(jf,\tau) = \frac{T}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\frac{\sin\left(\pi f T\right)}{\pi f T}e^{-j\pi f T},\ \tau\in[-2t_d,\ t_d]. \qquad (5.8)$$

Magnitude of the noise-jitter transfer function (5.8) is shown in Fig. 5.9. From the magnitude plot, it can be seen that the "noise-to-jitter conversion system" suppresses the noise components around frequencies that are integer multiples of the fundamental frequency, k/T.

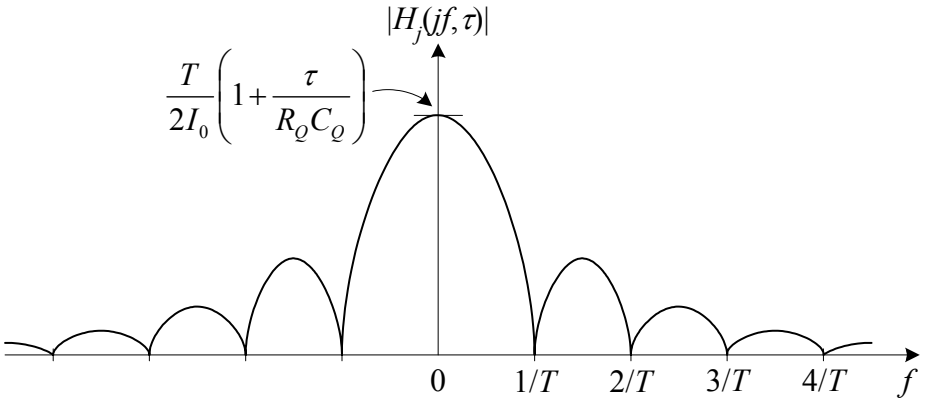


Fig. 5.9. Magnitude of the noise-jitter transfer function, $|H_j(jf,\tau)|$

Once we know the noise-jitter transfer function, we need to know the power spectral density (PSD) of the noise source $i_n(t)$ at time $t=\tau$, $S_n(f,\tau)$, in order to find power spectral density of the output jitter, $S_j(f,\tau)$:

$$S_j(f,\tau) = \left|H_j(jf,\tau)\right|^2 S_n(f,\tau) \tag{5.9}$$

Note that, in general, PSD of noise, S_n, depends on the impulse arrival time, τ.

Integrating (5.9) over all frequencies, we can obtain the expected instantaneous power of the output jitter, caused by the master-slave latch output-referred equivalent noise source at node Q, acting τ seconds from the time when slave latch output starts switching:

$$\overline{\sigma_{jQ}^2(\tau)} = \int_{-\infty}^{+\infty} \left|H_j(jf,\tau)\right|^2 S_n(f,\tau)df \quad , \ \tau\in[-2t_d,\, t_d] \tag{5.10}$$

In equation (5.10), it was assumed that power spectral densities are double-sided, hence integration is performed over the frequency range $(-\infty, +\infty)$.

In order to find average power of the jitter generated by noise during the entire period of the master-slave output signal, T, (5.10) needs to be integrated and averaged over the interval of τ, $\tau\in[-\frac{1}{2}T, \frac{1}{2}T]$. Note that $|H_j(jf,\tau)|$ is non-zero only in the interval $\tau\in[-2t_d, t_d]$.

$$\sigma_{jQ}^2 = \frac{1}{T}\int_{-T/2}^{T/2} \overline{\sigma_{jQ}^2(\tau)}d\tau = \frac{1}{T}\int_{-2t_d}^{t_d} \overline{\sigma_{jQ}^2(\tau)}d\tau$$

$$= \frac{1}{T}\int_{-2t_d}^{t_d} \left\{ \int_{-\infty}^{+\infty} \left|H_j(jf,\tau)\right|^2 S_n(f,\tau)df \right\} d\tau \tag{5.11}$$

Expression (5.11) gives total average jitter power generated by the equivalent current noise source on Q output (as in Fig. 5.5). Due to symmetry of the latch circuit, we can assume that jitter power caused by the equivalent noise source on $\overline{Q}$ output generates the same amount of jitter expressed in (5.11). Also, we can assume that noise sources on Q and $\overline{Q}$ are not correlated. Therefore, total jitter power caused by device noise in the master-slave latch during one cycle of the output signal is:

$$\sigma_j^2 = 2\sigma_{jQ}^2 = \frac{2}{T}\int_{-2t_d}^{t_d}\left\{\int_{-\infty}^{+\infty}\left|H_j(jf,\tau)\right|^2 S_n(f,\tau)df\right\}d\tau \tag{5.12}$$

Taking the square root of the total jitter power from (5.12) gives the RMS value of jitter generated during one cycle of the master-slave output signal i.e. cycle RMS jitter σ_j.

In the analysis above, we only investigated jitter generated around time t=0 or, according to the waveforms in Fig. 5.6 and Fig. 5.7, around the falling edge of $v_Q(t)$. In the same cycle, jitter is also generated during the rising transition of $v_Q(t)$, for $t\in[½T-2t_d, ½T+t_d]$. Due to symmetry, it can be assumed that the same amount of jitter is generated during both transitions of $v_Q(t)$ and therefore, one might expect that $2\sigma_j^2$ is the total average jitter power. However, we are only interested in the amount of jitter generated around one edge of $v_Q(t)$ because only one signal edge triggers the next FD stage and propagates through the following FD stages. Therefore, expression (5.12) yields the desired RMS cycle jitter of the master-slave latch.

Strictly speaking, impulse response function defined by (5.7) is periodic, with a period T, i.e. $h_j(t,\tau)=h_j(t+kT,\tau+kT)$, where k is an integer. The "noise-to-jitter conversion system" is then a linear periodically time-varying (LPTV) system and noise-jitter transfer function is actually represented by the Fourier series of $h_j(t,\tau)$. Since statistics of the noise sources acting in the FD circuit is cyclostationary, the autocorrelation function is also periodic and power spectral density is represented by its Fourier series. Phase noise analysis of LPTV systems with cyclostationary noise sources uses Floquet theory [Gard86]. In the analysis presented here, we are only interested in the RMS jitter generated during one cycle of the FD output signal i.e. cycle jitter, according to the definitions in Section 2. Hence, only one period of $h_j(t,\tau)$ is observed.

5.4.3. Level-shifter jitter generation

Level-shifter generates noise in exactly the same manner as the master-slave latch. When no device noise is present in the level-shifter circuit, a set of equations describing the output signals, similar to (5.1), can be found. Effects of noise on one of the outputs can also be analyzed by finding a time-dependent noise-jitter transfer function, which is going to have the same form as master-slave noise-jitter transfer function (5.8), but with level-shifter circuit parameters (DC biasing current, output capacitance and output resistance). Noise power spectral densities are also time-dependent, and expected instantaneous jitter power can be found by an equation similar to (5.10). Finally, average jitter power originating from equivalent noise sources on both output nodes can be found by an expression similar to (5.12). If this jitter power value is σ_{jLS}^2 and master-slave jitter power is σ_{jMS}^2, total average power of the entire FD stage, during one cycle of the FD output is

$$\sigma_{jFD}^2 = \sigma_{jMS}^2 + \sigma_{jLS}^2 \tag{5.13}$$

and the RMS value of jitter is σ_{jFD}.

5.4.4. Finding noise power spectral density

In calculations for jitter power, (5.8) through (5.12), time-varying power spectral density of noise $S_n(f, \tau)$ was assumed to be known. Methods for finding $S_n(f, \tau)$ will be studied in the future research, but now we should outline what $S_n(f, \tau)$ is and how to obtain it.

First, noise power spectral density $S_n(f, \tau)$ is a characteristic of the circuit output noise process τ seconds after the FD input signal arrival (more precisely, after the outputs start

switching). Statistics of that process can be obtained by measuring output noise at time τ, for a large number of measurements. Autocorrelation function of the samples from different measurements can be found, and Laplace transform of the autocorrelation will yield the power spectral density. It is expected that noise samples from different measurements are not going to be correlated and power spectral density should be constant. However, this needs to be proven in the future research.

To find $S_n(f,\tau)$ analytically, we need to find effects of the noise originating from devices in the circuit (resistors and transistors), summed at the output of the circuit. Some of the noise sources will contribute to the output noise with an amount that depends on the time τ, since the operating point is time-varying. For instance, current noise source of the resistor R_Q will have an effective value [Gray01]

$$i_{nR_Q} = \sqrt{\frac{4kT\Delta f}{R_Q}}$$

and this current source will appear at the Q output of the circuit. Its effective value does not depend on the operating point or τ. However, current noise source due to shot noise of M_4, for instance, (see Fig. 5.2) will have an effective value

$$i_{nM_4} = \sqrt{2qI_4\Delta f}$$

where I_4 is the drain current of M_4 which varies with τ. Therefore, powers of output-referred current noise sources from all devices have to be found at time τ, and then summed to form power of $i_n(\tau)$ from Fig. 5.5.

Finally, power spectral density $S_n(f,\tau)$ can be found through simulation. For instance, HSPICE can be used to find $S_n(f,\tau)$ by using .NOISE statement and performing .AC

analysis with DC voltages fixed to be identical to those of the switching latch circuit at time τ.

5.5. Comparison of the proposed model with HSPICE simulations

In the simulations, a one-stage CML FD without level-shifter, described at the beginning of this section was used.

5.5.1. Jitter generation as a function of FD load capacitance

As discussed in Section 4, RMS jitter generated by the FD increases with load capacitance at the FD output, C_Q. Some simulation results that confirm this were presented in that section (see Fig. 4.10). It should be noted here that, in the simulation, applied signals were not random; therefore results from Fig. 4.10 should be observed only qualitatively, rather than quantitatively.

Let us now use the expressions for jitter derived in this section, and study dependence of jitter on output capacitance. If we substitute $H_j(jf,\tau)$ from (5.8) into (5.12), we can obtain jitter power:

$$\sigma_j^2 = \frac{2}{T}\int_{-2t_d}^{t_d}\left\{\int_{-\infty}^{+\infty}\left|H_j(jf,\tau)\right|^2 S_n(f,\tau)df\right\}d\tau$$

$$= \frac{2}{T}\int_{-2t_d}^{t_d}\left\{\int_{-\infty}^{+\infty}\left|\frac{T}{2I_0}\left(1+\frac{\tau}{R_Q C_Q}\right)\frac{\sin(\pi fT)}{\pi fT}\right|^2 S_n(f,\tau)df\right\}d\tau$$

$$= \frac{2}{T}S_{n0}\left(\frac{T}{2I_0}\right)^2\int_{-2t_d}^{t_d}\left(1+\frac{\tau}{R_Q C_Q}\right)^2 d\tau\int_{-f_{FD}}^{f_{FD}}\left|\frac{\sin(\pi fT)}{\pi fT}\right|^2 df$$

$$= \frac{2}{T}S_{n0}\left(\frac{T}{2I_0}\right)^2\left(3t_d-\frac{3t_d^2}{R_Q C_Q}+\frac{3t_d^3}{(R_Q C_Q)^2}\right)\frac{K}{\pi T}$$

$$= \frac{2}{\pi T^2}S_{n0}K\left(\frac{T}{2I_0}\right)^2\left(3t_d-\frac{3t_d}{2}+\frac{3t_d}{4}\right)$$

$$= \frac{2}{\pi}S_{n0}K\left(\frac{1}{2I_0}\right)^2\frac{9}{4}t_d$$

$$= \frac{9}{8}\frac{S_{n0}K}{I_0}t_d$$

$$= \frac{9}{8}\frac{S_{n0}K}{I_0}t_d$$

In the calculations above, it was assumed that the noise PSD $S_n(f, \tau)$ was constant over the range of frequencies $[-f_{FD}, f_{FD}]$, with a value of S_{n0}, as well as that it was constant in time (not dependent on τ), according to assumption I. K is a unitless constant:

$$K = \int_{-\pi If_{FD}}^{\pi If_{FD}}\left|\frac{\sin x}{x}\right|^2 dx \Rightarrow \frac{K}{\pi T} = \int_{-f_{FD}}^{f_{FD}}\left|\frac{\sin \pi fT}{\pi fT}\right|^2 df$$

and, in the first approximation, we can assume that it does not depend on output capacitance, i.e. f_{FD} is not a function of C_Q. Substituting the value for t_d from (5.2), we obtain:

$$\sigma_j^2 = \frac{9}{16}\frac{S_{n0}K}{I_0}R_Q C_Q$$

Derivations above show that jitter increases with transition time (or delay), t_d, of the output signal, which is proportional to the output capacitance C_Q.

5.5.2. Simulation of zero-crossing time variation

The next experiment shows dependence of the output crossing time variation on noise current impulse arrival, τ. The test setup was the same as in Fig. 5.5, with $i_n(t)$ being a very short current pulse which injects about $q_n=2\times10^{-16}$C of charge. Fig. 5.10 presents simulation results – the measured crossing time variation per unit charge, $t'_j = t_j/q_n$, which is represented by the bold line in Fig. 5.10. Nominal output waveforms (when noise is not present) are also shown in Fig. 5.10. Time τ=0 is the arrival time of the rising *CLK* edge. The simulation results are compared to the value of t'_j predicted by the model, in (5.6), with the circuit parameters listed in Table 5.1.

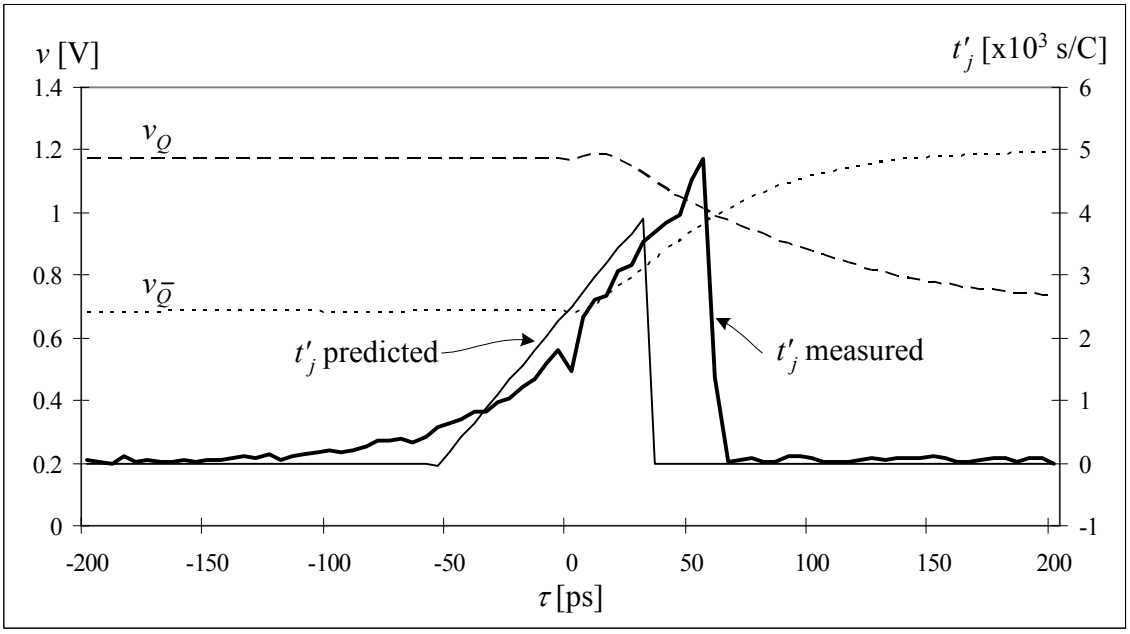


Fig. 5.10. Simulated and predicted crossing time variation per unit charge, t'_j

It can be seen from Fig. 5.10 that there exists matching between the model and the results obtained by simulation. The main mismatch is due to difference of the predicted nominal crossing time (delay time), t_d, which was about 30ps, and the measured t_d, which was 60ps. Therefore, curve for predicted t'_j ends early. This could be improved by using a

more accurate expression for delay time: $t_d = R_Q C_Q \ln 2$ which would, in this case, yield the value of about 40ps.

The results shown in Fig. 5.10 are encouraging because they confirm validity of (5.6). However, future research has to prove that the impulse response of the "noise-to-jitter conversion" system defined in (5.7) successfully approximates amount of jitter generated by the CML FD.

5.6. Novel approaches in the proposed model

Comparing to the previously published work on FD jitter and phase noise analysis, which mainly consists of reporting experimental data, the model proposed here gives a close insight into jitter generation mechanisms in FD, allowing jitter prediction. As mentioned before, the model was mainly inspired by oscillator jitter and phase noise analyses presented in [McNe97] and [Haji98]. Improvements and differences between the proposed model and these analyses will be discussed now.

First, [McNe97] and [Haji98] deal with electric oscillators, which are autonomous systems, unlike frequency dividers. Therefore, jitter generation mechanisms are different in these two types of circuits. In frequency dividers, jitter generated in one signal cycle is caused only by noise sources that are active in that cycle, in contrast to oscillators, where jitter generation mechanism has memory.

Ring-oscillator jitter model presented in [McNe97] does not account for time-variance of the noise-to-jitter conversion. It only evaluates jitter that is produced by noise sources at the time when oscillator output signals intersect. Therefore, FD jitter model proposed here would reduce to an analogous oscillator jitter model from [McNe97], if the above

analysis was performed only at $\tau=t_d$. Introducing time-variance significantly complicates the analysis, but is expected to yield more accurate estimate of jitter.

[Haji98] presents a time-variant model for oscillator phase noise. However, it treats device noise as a deterministic signal and sums effects of noise on phase shifts at different time instances τ using effective values rather than variances. In the FD jitter model proposed here, noise analysis of a linear (time-variant) system was performed, respecting the random nature of noise. Also, in [Haji98] phase noise is not related to circuit parameters and hence this model cannot give guidelines for reducing phase noise on the circuit-level. Impulse sensitivity function (ISF), which is the equivalent of the noise-jitter impulse response $h_j(t,\tau)$ presented here, is usually obtained through simulation, rather than circuit analysis, which was the case here.

Section 6:

Proposed future research and contributions

6.1. Proposed future research

In the future, analytical model for current-mode logic frequency divider (CML FD) jitter, proposed here, needs to be modified in order to develop a model that even more closely describes the phenomenon of jitter generation. For instance, improvements of the proposed model would be to find more accurate expressions for output voltages of the master-slave latch than those in (5.1), in order to get equations that more closely describe the actual waveforms from Fig. 5.4. This way, a more accurate estimate of the nominal crossing time t_d will be obtained, since it was shown that computed t_d was the main source of mismatch between the predicted and measured crossing time variation in Fig. 5.10. Also, more than first two terms of the Taylor series of the exponential function in (5.3) could be used, in order to find a more accurate expression for the crossing time variation t_j. The new time-varying impulse response of the "noise-to-jitter conversion system", $h_j(t,\tau)$, will depend on more circuit parameters than in the current model, which will give more insight into ways to reduce jitter by appropriate design. Also, effects of the level-shifter noise on FD jitter should be included and a method for finding the time-varying noise power spectral density $S_n(f,\tau)$ should be formulated, to complete the model. During the process of developing the model, computer simulations will be involved in order to validate the model. HSPICE or some other CAD tool can be used to compare noise-jitter transfer functions and noise power spectral densities obtained analytically and

through simulations. The simulations should also show whether the definition (5.7) of the "noise-to-jitter conversion system" impulse response function $h_j(t,\tau)$ is valid.

Once the analytical model for CML FD jitter is established, it should be used to predict jitter generated by a multi-stage FD (e.g. FD by 64). The FD will be implemented using the 0.11μm process by Fujitsu. The device will be fabricated and jitter performance will be measured. The experimental results will be compared to the analytical results and conclusions about the validity of the model will be made.

Using the analytical model, a set of design guidelines on how to minimize jitter in CML FD will be assembled. These guidelines will be used to design and fabricate a very low jitter FD for RF applications. Jitter performance of this FD will be measured and compared to the performance of other published FD designs.

Plan for the proposed future research, with a tentative schedule, is summarized in Table 6.1.

Table 6.1. Proposed future research tentative schedule

Develop analytical model: establish $h_j(t,\tau)$, $S_n(f,\tau)$	Spring 04 – Fall 05
Prepare test chip and test setup	Winter 05 – Spring 05
Measure FD jitter, compare with analytical model and analyze results	Summer 05
Give design guidelines for low-jitter FD and design a low-jitter FD	Fall 05 – Spring 06
Measure performance of low-jitter FD	Summer 06

6.2. Contributions

Jitter and phase noise can significantly impair performance of high-speed communication systems. Therefore, jitter specifications for phase-locked loops (PLL) that are used to generate clock and carrier signals in these systems are very strict. Even though they are a

part of every high-performance PLL, jitter or phase noise analysis of frequency dividers (FD) has not received much attention in the literature. Some papers report FD jitter or phase noise measurements, or at most, attempt to model FD phase noise by extrapolating the experimental data, but are all based on post-fabrication analysis. As shown in this proposal, FD jitter can considerably contribute to the total PLL output jitter since phase noise amplification is achieved through the PLL, especially when the division ratio is high. This analysis demonstrates the importance of modeling FD jitter and knowing the FD jitter performance before fabrication.

One important outcome of this research, once it is completed, will be the analytical model of CML FD jitter, which will show how device noise transforms into jitter and allow estimation of jitter generated by the FD in the pre-silicon stage of the design process. Current version of this model is presented in this proposal.

Another important outcome of the research will be a set of design guidelines that will be assembled using the model: dependence of jitter on circuit parameters, expressed in the model, will be used to derive methods for jitter minimization. These guidelines will be used to design a very low-jitter FD for RF applications.

Hopefully, this research will help designing even better high-performance, low-jitter clock and carrier signals generators, which will make possible achieving even higher signaling rates in communication systems.

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