EEC 212
Problem Set 6

Professor Hurst

Read: Chapter on Switched-Capacitor Circuits

1

A first-order switched capacitor high-pass filter is shown in Figure 1.

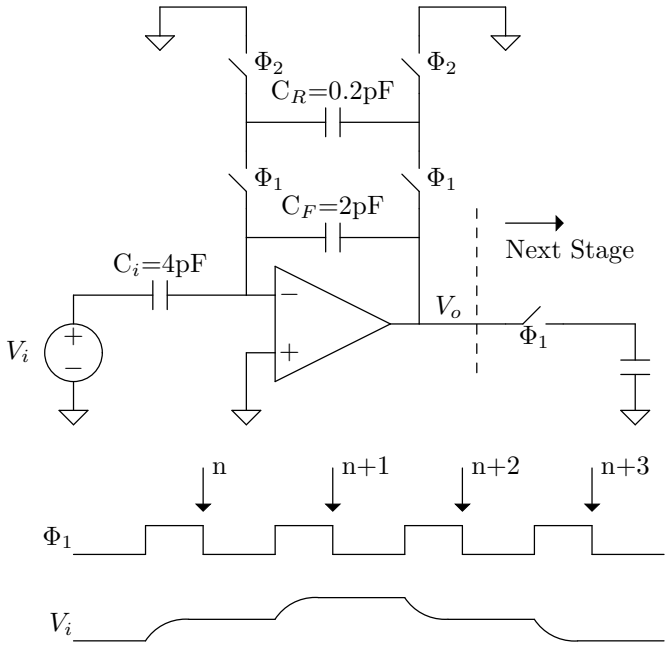

Figure 1: High-pass filter for Problem 1

(a) Find $H(z) = \frac{V_o}{V_i}(z)$. Assume an ideal op-amp and V_o is to be sampled on Φ_1.

(b) What is the new pole location if the op-amp has a finite open-loop voltage gain of 200?

2

An R-C filter shown in Figure 2 is to be transformed into the S-C filter shown in Figure 3. Assume an ideal op-amp is used (e.g., a $\rightarrow \infty$).
(a) If f_S = 200kHz, compute values for C_i and C_R using the approximation $R_{eqx} \approx 1/(f_S C_X)$.

(b) Find $H(z) = \frac{V_o}{V_i}(z)$. What is the dc gain? What is the minimum gain? At what frequency is the minimum gain?

(c) Verify the design using SWITCAP. Look at $H(z)$ using the command

SAMPLE OUTPUT IMPULSE ....

in SWITCAP. (See page 27 of the SWITCAP manual.)

(d) Plot $|\hat{H}\left(z = e^{j\omega T_S}\right)|$ for Figure 3 and $|H\left(s = j\omega\right)|$ for Figure 2 on the same graph for $f = 0$ to $f = f_S$. Over what frequency range do the two plots differ by less than 20%?

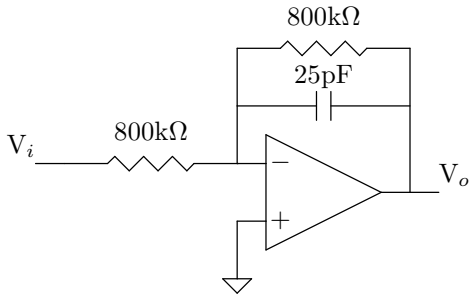

Figure 2: R-C Filter for Problem 2

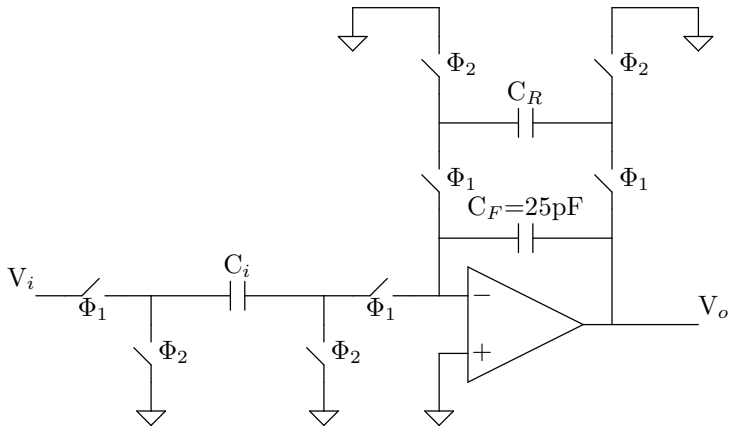

Figure 3: Transformed S-C Filter for Problem 2

3

Return ratio can be simulated using SPICE by breaking the loop at an arbitrary point and calculating 2 terms, RR'_V and RR'_I, which can be combined to find RR. (See attached, first 3 pages of a paper).

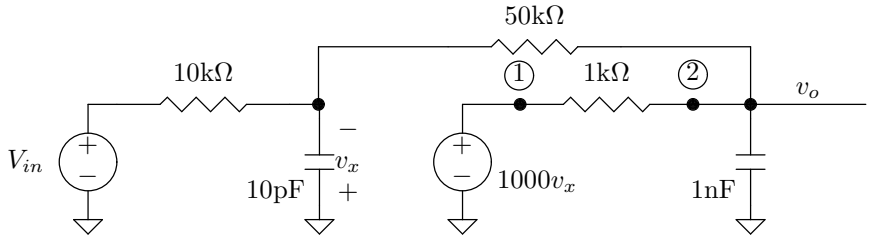

Figure 4: Circuit for Problem 3

(a) For the circuit in Figure 4, use SPICE to find the RR directly by breaking the loop at node 1. Print or plot the magnitude and phase of RR. Is this feedback circuits stable? What is the phase margin?

(b) Find the RR indirectly by breaking the loop at node 2 and finding $RR'_V = -v_r/v_d$ in Figure 4a of the attached paper and $RR'_I = -i_r/i_d$ in Figure 4b of the attached paper (use SPICE). Then RR can be found using Equation 3 in the paper. (Note: The return ratios are complex numbers.) Compare this answer with the answer you got in 3a. They should agree. [The return ratio can be found indirectly from SPICE simulations and some post processing. Potentially useful information on running simulations to find return ratio of a single-ended feedback circuit is on the 212 web page. It uses HSPICE and Linux post-processing scripts (that once worked but may not work now due to changes to HSPICE).]

There are three Appendices below:
Appendix A - Running SWITCAP
Appendix B - Sample SWITCAP input file
Appendix C - First 3 pages of this paper (the complete paper is available from the course web page):

P.J. Hurst and S.H. Lewis, **Determination of stability using return ratios in balanced fully differential feedback circuits.** *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 805-817, Dec. 1995.

Appendix A: Running SWITCAP at UCD

Note: SWITCAP is not the most user-friendly program. Its error messages can be confusing, and sometimes a major error in the input file will produce no output. However, SWITCAP is simple, easy to learn and effective. So we'll use it.

To run SWITCAP: see "How to run SWITCAP1 on a Linux computer" on the ECE 212 web page. The SWITCAP manual can be accessed from the ECE 212 web page (see "SWITCAP Manual").

Appendix B: Sample SWITCAP Circuit

The sample SWITCAP circuit is shown on Figure 5 and the corresponding netlist, which is the SWITCAP input file, is below. Note that #CLK means 'non-overlapping complement of CLK'.

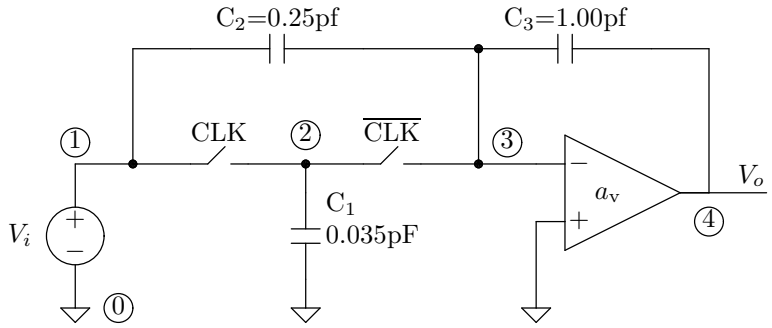

Figure 5: Sample SWITCAP problem ($a_v = 5500$)

Input netlist

```
TITLE: Sample SWITCAP Circuit;

TIMING;
PERIOD 8E-6;
CLOCK clk 1 (0 3/8);
END;

CIRCUIT;
S1 (1 2) clk;
S2 (2 3) #clk;
C1 (2 0) 0.035;
C2 (1 3) 0.250;
C3 (3 4) 1.000;
E1 (4 0 0 3) 5500;
V1 (1 0);
END;

ANALYZE SSS;
INFREQ 0.01 100000 LOG 15;
SET V1 AC 1.0 0.0;
PRINT VR(4) VI(4);
PLOT VDB(4) VP(4);
END;

END;
```