EEC 212
Problem Set 5

Professor Hurst

1

For the sample-and-hold circuit in Figure 1 estimate the $\frac{W}{L}$ value needed to give $R_{ON} \cdot C_H \leq 0.5$ μsec for $V_{CK} = 5$V and $V_{in} \leq 3$V. Assume k' = $60\frac{\mu A}{V^2}$ and $V_{T(MAX)}$=0.7V (including body effect).

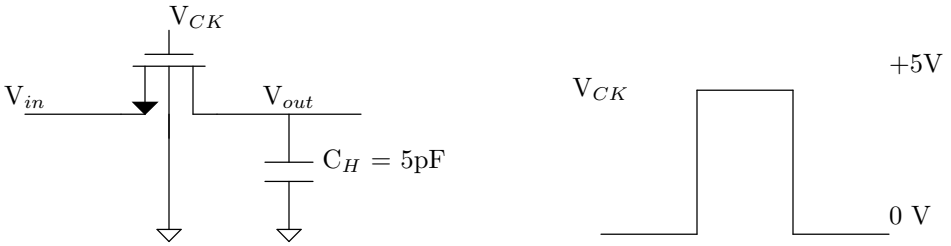

Figure 1: Sample-and-Hold Circuit for Problem 1

2

A fully differential op-amp with CMFB is show in Figure 2. All bodies of PMOS transistors are connected to V_{DD}, and all bodies of NMOS transistors are connected to V_{SS}. Let X_d=0, and use the transistor sizes listed on table below as well as the transistor data in the SPICE models (see next page).

Transistor	W (μm)	L (μm)
M_{1-2}, M_{1C-2C}	64	0.8
M_{3-4}, M_{26-27}, M_{11}	96	1.4
M_{21-24}	6	0.8
M_{14}, M_{25}, M_{52}	16	0.8
M_{13}	1.4	0.8

(a) Choose W values for M_{12} and M_{51} so that $|I_{D13}| = 20\mu$A. Use L=0.8μm for M_{51} and L=1.4μm for M_{12}.

(b) Use SPICE to find the low-frequency op-amp gain v_{od}/v_{id}, v_{oc}/v_{ic}, v_{od}/v_{ic}, and v_{oc}/v_{id} with the CMFB active. **NOTE:** To get HSPICE to compute the differential output voltage correctly using 'v(out1,out2)', you must include '.options acout=0' in your HSPICE input file. For the op-amp inputs, use $V_{IN(CM)} = -0.65$V.

(c) Calculate the output slew rate dV_{od}/dt if a 4 pF capacitor is connected from each op-amp output to ground.

(d) What is the differential output voltage swing of this op-amp? Assume that $V_{IN(CM)} = -0.65$V. (Ignore the body effect.)

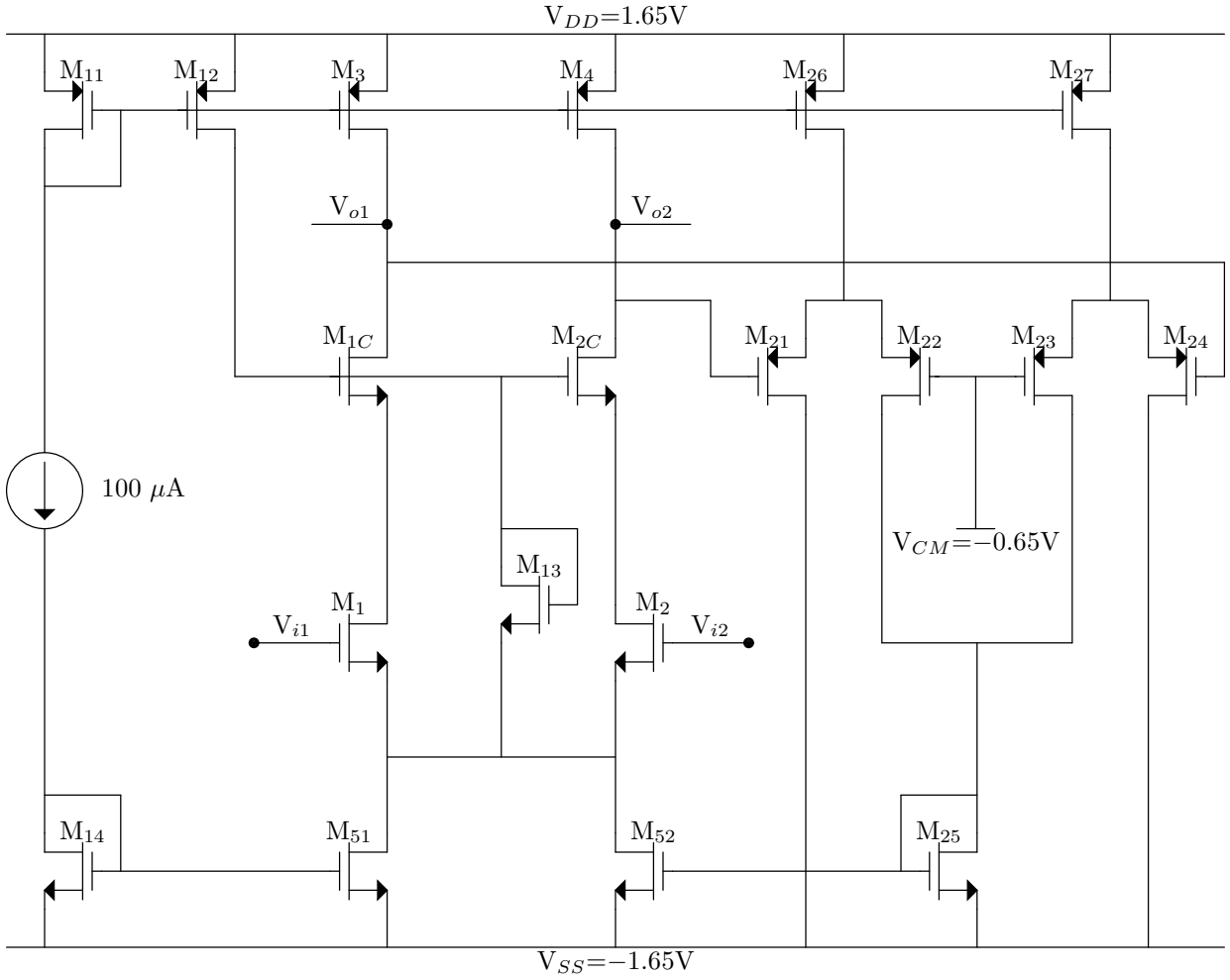

Figure 2: Op-amp for Problem 2

(e)** Repeat (b) when the input transistors are mismatched with $W_1 = 63\mu$m and $W_2 = 65\mu$m.

(f)** Repeat (b) when the load transistors are mismatched with $W_3 = 95\mu$m and $W_4 = 97\mu$m.

******Note: $V_{OS} \neq 0$ with mismatched transistors.

(g) It is possible to bias the op-amp without M_{51}. What change in device W/L should be made to M_{52} to keep the op-amp unchanged when M_{51} is deleted?

(h) Can you see any advantage to making the change described in (g)?

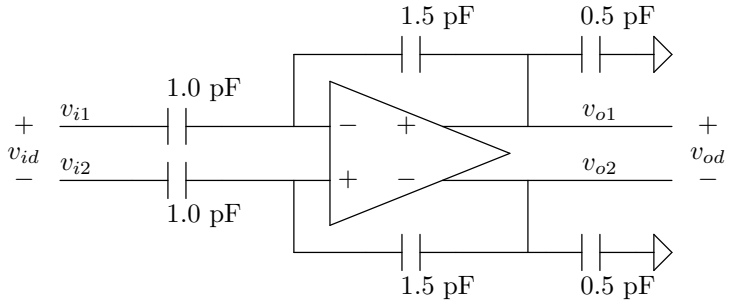

Figure 3: Circuit for Problem 3

3

During one clock phase in a SC filter, the op-amp in problem 2 is in the configuration shown in Figure 3.

(a) Apply a 1-V step as a differential input, using SPICE. What is the slew plus settle time to within 0.5% of the final value?

(b) What is the slew rate? How does this compare with the calculation of $\frac{\pm I_{BIAS}}{C_L'}$?

Note: You'll have to add DC feedback to this circuit; this feedback should not affect the circuit above about 10kHz. One way to do this is to put a very large resistor across each 1.5 pF cap: [e.g., rfb x y 1.0t].

SPICE MODELS: 0.4 μm CMOS

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.MODEL CMOSN NMOS LEVEL=3
+ TOX=0.8000E-08 XJ=0.150000U TPG=1 PHI=0.600000 DELTA=2.1370E-01
+ LD=9.0003E-08 VTO=0.60 GAMMA=0.5947 UO=450 THETA=1.9240E-01
+ RSH=1.7260E+01 KP=1.96E-04 NSUB=1.2706E+17 NFS=6.0410E+11
+ VMAX=1.8610E+05 ETA=2.1370E-02 KAPPA=8.4220E-02 CGDO=3.5E-10
+ CGSO=3.5E-10 CGBO=3.0251E-10 CJ=5.2E-04 MJ=0.59 CJSW=1.2E-10
+ MJSW=0.31 PB=0.98 ACM=3 HDIF=0.4u

.MODEL CMOSP PMOS LEVEL=3
+ TOX=0.8000E-08 XJ=0.150000U TPG=-1 PHI=0.600000 DELTA=2.0729E-01
+ LD=9.0000E-08 VTO=-0.80 GAMMA=0.5200 UO=137.3 THETA=1.6710E-01
+ RSH=3.6310E+00 KP=6.6E-05 NSUB=9.7132E+16 NFS=5.9890E+11
+ VMAX=3.0560E+05 ETA=1.8760E-02 KAPPA=5.9230E+00 CGDO=3.5E-10
+ CGSO=3.5E-10 CGBO=3.1661E-10 CJ=9.1191E-04 MJ=0.49 CJSW=1.2E-10
+ MJSW=0.201 PB=0.96 ACM=3 HDIF=0.4u
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You can copy the SPICE MODELS file from: ***/home/hurst/212/MOS_models_0.4um***