EEC 212
Problem Set 2

Professor Hurst

1

(a) Compute the error in the ratio of C_2/C_1 for the two layouts below in Figures 1 & 2 when there is a 1 μm overetch on each edge of all top plates. The overetch causes C_1 to be 8 μm×8 μm. The desired C_2/C_1 ratio is 11.

(i)

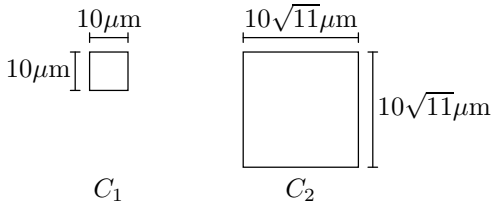

Figure 1: Layout 1 for Problem 1a.

(ii)

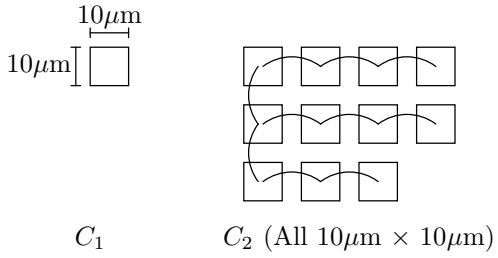

Figure 2: Layout 2 for Problem 1a.

(b) Repeat (a) for the capacitors Figures 3 & 4: The desired C_2/C_1 ratio is 11.5.

(i)

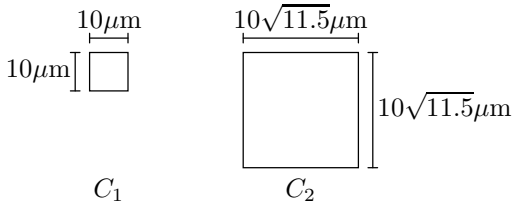

Figure 3: Layout 1 for Problem 1b.

(ii)

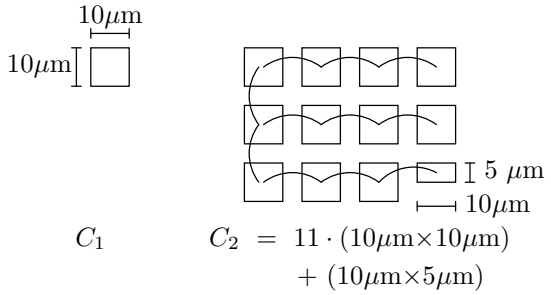

Figure 4: Layout 2 for Problem 1b.

2

Read the Capacitor Matching material in Section 2.4 in the text.

3

Using the results on page 110, find the W and L for C_X in Figure 5 to give a ratio $C_2/C_1 = 11.8$, independent of overetch:

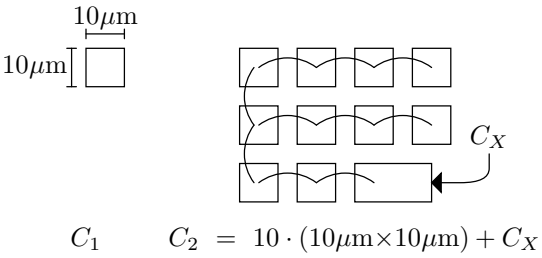

Figure 5: Layout for Problem 3.

4

If R can vary by ±30% and C can vary by ±10%, what are the maximum and minimum values of f_{-3dB} for the one-pole filter in Figure 6?

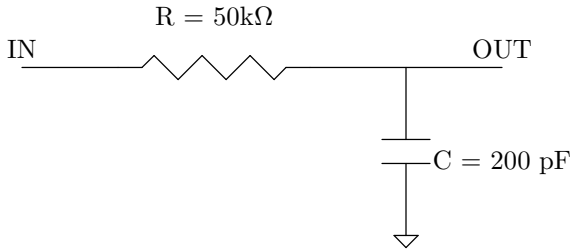

Figure 6: Low pass filter for Problem 4

5

What is the small-signal voltage gain for the circuit in Figure 7? Assume all transistors are saturated with $I_D = 100\mu$A, $\lambda_N = 0.05\text{V}^{-1}$, $|\lambda_P| = 0.01\text{V}^{-1}$. Take any other data needed from the first table in problem

set 1. Assume $\gamma_n = 0$ V$^{\frac{1}{2}}$, and ignore impact ionization (See attached).

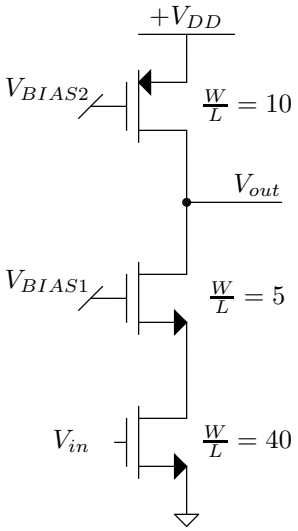

Figure 7: Amplifier for Problem 5

6

Read the material in the text on resistors and capacitors (see table of contents). (Ignore "switched-cap resistors" for now.)

Substrate Current Flow in MOS Transistors

Avalanche breakdown affects current flow in bipolar transistors. As the reverse-bias voltages on the device are increased, carriers traversing the depletion regions gain sufficient energy to create new electron-hole pairs in lattice collisions by a process known as *impact ionization*. Eventually, at high-enough bias voltages, the process results in large avalanche currents. For collector-base bias voltages well below the breakdown value, a small enhanced current flow may occur across the collector-base junction due to this process with little apparent effect on the device characteristics.

Impact ionization also occurs in MOSFETs but has a significantly different effect on the device characteristics. This difference is because the channel electrons (for the NMOS case) create electron-hole pairs in lattice collisions in the drain depletion region, and some of the resulting holes then flow to the substrate, creating a substrate current. (The electrons created in the process flow out the drain terminal.) The carriers created by impact ionization are therefore not confined within the device as in a bipolar transistor. The effect of this phenomenon can be modeled by inclusion of a controlled current generator I_{DB} from drain to substrate, as shown in Fig. 8 for an NMOS device. The magnitude of this substrate current depends on the voltage across the drain depletion region (which determines the energy of the ionizing channel electrons), and also on the drain current (which is the rate at which the channel electrons enter the depletion region). Empirical investigation has shown that the current I_{DB} can be expressed as

$$I_{DB} = K_1 \left(V_{DS} - V_{DSsat}\right) I_D e^{-[K_2/(V_{DS}-V_{DSsat})]} \tag{1}$$

where K_1 and K_2 are process-dependent parameters and $V_{DS(act)}$ is the minimum value of V_{DS} for which the transistor operates in the saturation region. Typical values for NMOS devices are $K_1 = 5\ \mathrm{V}^{-1}$ and $K_2 = 30$ V. The effect is generally much less significant in PMOS devices because the holes carrying the charge in the channel are much less efficient in creating electron-hole pairs than energetic electrons.

The major impact of this phenomenon on circuit performance is that it creates a parasitic resistance from drain to substrate. Because the common substrate terminal must always be connected to the most negative supply voltage in the circuit, the substrate of an NMOS device in a p-substrate process is an ac ground. Therefore, the parasitic resistance shunts the drain to ac ground and can be a limiting factor in many circuit designs. Differentiating (1), we find for the drain-substrate small-signal conductance

$$\begin{aligned} g_{db} &= \frac{\partial I_{DB}}{\partial V_D} \\ &= K_2 \frac{I_{DB}}{(V_{DS}-V_{DSsat})^2} \end{aligned} \tag{2}$$

where the gate and source are assumed to be held at fixed potentials.

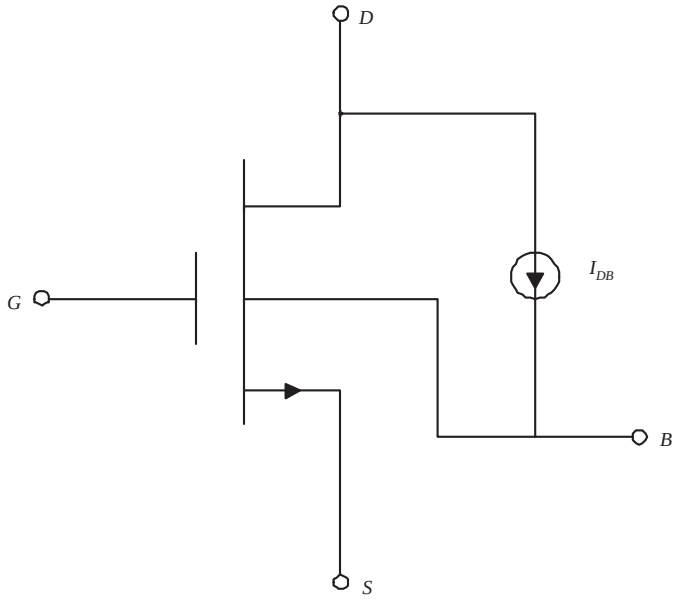

Figure 8: Representation of impact ionization in a MOSFET by a drain-substrate current generator