EEC 212
Problem Set 1

Professor Hurst

Read: Chapter 1 and 2

1

Calculate λ using the attached table 2.1 for: (use $L = L_{drawn} - 2L_d$)

(a) NMOS transistor with $W = 20$ μm and $L_{drawn} = 3$ μm.

(b) NMOS transistor with $W = 20$ μm and $L_{drawn} = 10$ μm.

- Operating Point: $I_D = 100$ μA, $V_{DS} = 5$V, $V_{SB} = 0$V.
- For N_A in the equation for λ, use $N_A(Surface) \approx \underbrace{N_A + N_{Si}}_{values\ in\ Table\ 2.1}$.
- For the built-in potential, use $\phi = 0.7$V.

2

Calculate the small-signal model parameters of the NMOS device shown in Figure 1, including g_m, g_{mb}, r_o, C_{gs}, C_{gd}, C_{sb}, and C_{db}. Assume the transistor is biased at a drain-source voltage of 2 Volts and a drain current of 20μA. Use the process parameters that are specified in Table 2.4. Assume $V_{SB} = 1$V. For the built-in potential in the formulas for λ and X_d, use $\phi = 0.7$V.

3

Plot the total on-resistance (R_{ON}) vs. V_{IN} for $-5\text{V} \leq V_{IN} \leq +5\text{V}$ for the MOS switch shown in Figure 2 for the following three cases. Use the device data on the next page with $(\frac{W}{L})_N = 10$, and $(\frac{W}{L})_P = 20$. Use $\gamma_P = \gamma_N = 0$. (Use Table 2.1)

(a) $V_{GN} = V_{GP} = 5$V.

(b) $V_{GN} = V_{GP} = -5$V.

(a) $V_{GN} = 5$V and $V_{GP} = -5$V.

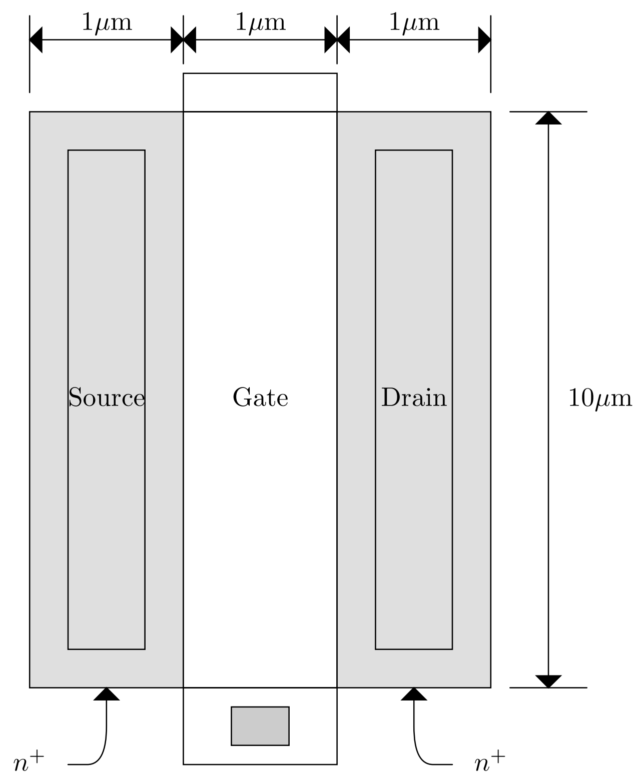

Figure 1: Transistor for Problem 2.

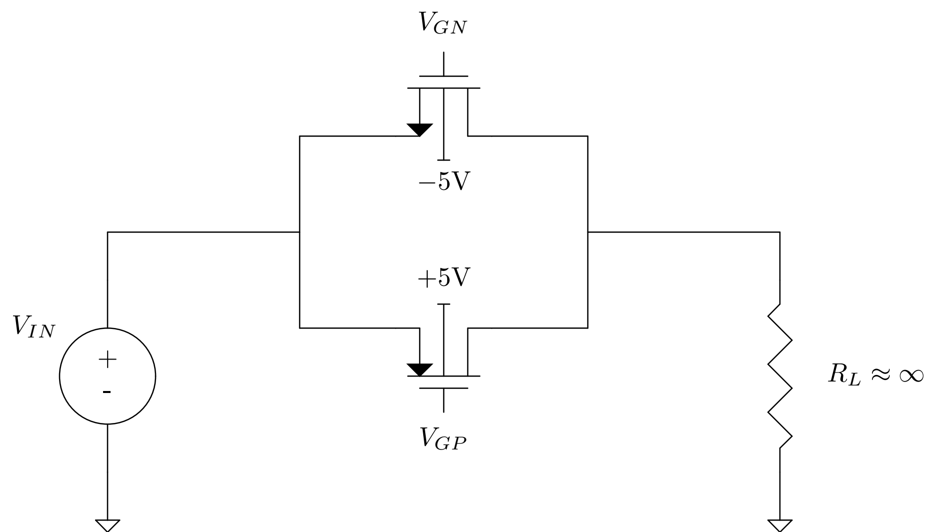

Figure 2: CMOS Switch for Problem 3.

TABLE 2.1 Summary of Process Parameters for a Typical Silicon-Gate n-Well CMOS Process with 3 μm Minimum Allowed Gate Length (Table taken from Gray, Hurst, Lewis and Meyer text book)

Parameter	Symbol	Value n-Channel Transistor	p-Channel Transistor	Units
Substrate doping = N_{SUB}	N_A, N_D	1×10^{15}	1×10^{16}	Atoms/cm^3
Gate oxide thickness	t_{ox}	400	400	Angstroms
Metal-silicon work function	ϕ_{ms}	− 0.6	− 0.1	V
Channel mobility	μ_n, μ_p	700	350	cm^2/V-sec
Minimum drawn channel length	L_{drwn}	3	3	μm
Source, drain junction depth	X_j	0.6	0.6	μm
Source, drain side diffusion	L_d	0.3	0.3	μm
Overlap capacitance per unit gate width	C_{ol}	0.35	0.35	fF/μm
Threshold adjust implant (box dist)				
impurity type		P	P	
effective depth	X_i	0.3	0.3	μm
effective surface concentration	N_{si}	2×10^{16}	0.9×10^{16}	Atoms/cm^3
Nominal threshold voltage	V_{t0}	0.7	− 0.7	V
Polysilicon gate doping concentration	N_{dpoly}	10^{20}	10^{20}	Atoms/cm^3
Poly gate sheet resistance	R_s	20	20	$\Omega/Square$
Source, drain-bulk junction capacitances (zero bias)	C_{j0}	0.08	0.20	fF/μm^2
Source, drain-bulk junction capacitance grading coefficient	n	0.5	0.5	
Source, drain periphery capacitance (zero bias)	C_{jsw0}	0.5	1.5	fF/μm
Source, drain periphery capacitance grading coefficient	n	0.5	0.5	
Source, drain junction built-in potential	ψ_0	0.65	0.65	V
Surface-state density	$\frac{Q_{SS}}{q}$	10^{11}	10^{11}	Atoms/cm^2

Also use:

$$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm \quad (1)$$

$$\epsilon_{si} = 1.04 \times 10^{-12}\ F/cm \quad (2)$$

$$\phi_{SB} = \phi_{DB} = 0.65\ V \quad (3)$$

TABLE 2.4 Summary of Process Parameters for a Typical Silicon-Gate n-Well CMOS Process with 0.4 μm Minimum Allowed Gate Length (Table taken from Gray, Hurst, Lewis and Meyer text book)

Parameter	Symbol	Value n-Channel Transistor	Value p-Channel Transistor	Units
Substrate doping	N_A, N_D	5×10^{15}	4×10^{16}	Atoms/cm^3
Gate oxide thickness	t_{ox}	80	80	Angstroms
Metal-silicon work function	ϕ_{ms}	− 0.6	− 0.1	V
Channel mobility	μ_n, μ_p	450	150	cm^2/V-sec
Minimum drawn channel length	L_{drwn}	0.4	0.4	μm
Source, drain junction depth	X_j	0.15	0.18	μm
Source, drain side diffusion	L_d	0.09	0.09	μm
Overlap capacitance per unit gate width	C_{ol}	0.35	0.35	fF/μm
Threshold adjust implant (box dist)				
impurity type		P	P	
effective depth	X_i	0.16	0.16	μm
effective surface concentration	N_{si}	4×10^{16}	3×10^{16}	Atoms/cm^3
Nominal threshold voltage	V_{t0}	0.6	− 0.8	V
Polysilicon gate doping concentration	N_{dpoly}	10^{20}	10^{20}	Atoms/cm^3
Poly gate sheet resistance	R_s	5	5	$\Omega/Square$
Source, drain-bulk junction capacitances (zero bias)	C_{j0}	0.2	0.4	fF/μm^2
Source, drain-bulk junction capacitance grading coefficient	n	0.5	0.4	
Source, drain periphery capacitance (zero bias)	C_{jsw0}	1.2	2.4	fF/μm
Source, drain periphery capacitance grading coefficient	n	0.4	0.3	
Source, drain junction built-in potential	ψ_0	0.7	0.7	V
Surface-state density	$\frac{Q_{SS}}{q}$	10^{11}	10^{11}	Atoms/cm^2