1. The circuit below is a differential Sample-and-Hold circuit. Each NMOS transistor acts as a switch, controlled by the clock PHI.

![Differential Sample-and-Hold Circuit Diagram]

a) Assume that PHI is high (V_{PHI} = 5V) and each NMOS transistor is in the triode region, with V_{DS} = 0V. Find W/L to give an on-resistance R_{ON} of 40 k\Omega for each transistor. Assume the two inputs are both 0 V for this calculation.

W / L =

\[
R_{on} = \frac{1}{k_n \frac{W}{L} (V_{GS} - V_T)}
\]

\[
= \frac{1}{180 \mu A V_2 (\frac{W}{L}) (5V - 1V)} = 40k\Omega
\]

\Rightarrow \frac{W}{L} = 0.035
b) It is important that the capacitors and transistors are closely matched. You are allowed 200 (\mu m)^2 of total area for the top plates of the two capacitors. Sketch the layout of the top plates for the two capacitors. Give the dimensions of the capacitors on your drawing. (For this part, the most important thing is capacitor matching. Don't worry about the -3 dB frequency of the filter or the capacitor values.)

Use max area, close together,

(should include common centroid)
A two-stage op amp is shown below. It was designed to have a bias current \( IB = 20 \, \mu A \). However, due to a layout error, the op amp is operating with a bias current \( IB = 10 \, \mu A \), which is half of the design value. For each parameter below, relate the value of the parameter when \( IB = 10 \, \mu A \) to the value of the parameter when \( IB = 20 \, \mu A \). (That is, find the scale factor that relates the two values.)

Assume DC biasing places all the transistors in the saturation region for both values of \( IB \), and further assume that all capacitances do not change when the bias current changes.

\[ a_v = \frac{v_{out}}{v_{id}} \]

a) How does the low-frequency voltage gain, \( a_v = \frac{v_{out}}{v_{id}} \), change?

\[ a_v(IB = 10 \, \mu A) = \frac{v_{out}}{v_{id}} = \frac{1}{2} \cdot a_v(IB = 20 \, \mu A) \]

\[ a_v = \frac{g_m \cdot R_2}{g_m \cdot R_2} \cdot \frac{1}{\sqrt{I_B} \cdot \sqrt{I_B}} \cdot \frac{1}{I_B} = \frac{1}{I_B} \]
b) slew rate\( (IB = 10 \, \mu A) = \frac{1}{2} \cdot \text{slew rate}\ (IB = 20 \, \mu A) \)

c) The output resistance of the op amp is \( R_{out} \).

\[ R_{out} = R_{e} \parallel R_{o} \alpha \frac{1}{I_{B}} \]

\[ \alpha \leq \frac{1}{I_{B}} \leq \frac{1}{I_{E}} \]

d) dominant pole: \( p_1(IB = 10 \, \mu A) = \frac{0.35}{11} \cdot p_1(IB = 20 \, \mu A) \)

\[ p_1 = -\frac{1}{g_m R_0 R_1 C_c} \]

\[ \alpha = \frac{-1}{\sqrt{5} \frac{1}{I_g} \frac{1}{I_g}} = -I_{E}^{\frac{3}{2}} \]
e) The non-dominant pole is $p_2$:

$$p_2(\text{IB} = 10 \ \mu\text{A}) = 0.71 \cdot p_2(\text{IB} = 20 \ \mu\text{A})$$

$$p_2 \approx -\frac{g_m}{C_e} \cdot \alpha - \sqrt{I_B}$$

f) The upper limit of the op-amp output voltage swing is $V_{out}^+$:

Circle one:
- $V_{out}^+$ (IB = 10 \ \mu\text{A}) is LESS THAN, GREATER THAN, SAME AS $V_{out}^+$ (IB = 20 \ \mu\text{A})

$$V_{out}^+ = 5V - |V_{b3, SAT}(mX)|$$

$$= 5V - \sqrt{\frac{2I_D(mX)}{k_p(10)}}$$

$I_B \uparrow \Rightarrow V_{out}^+ \uparrow \Rightarrow V_{out}^+$
3. A fully differential op amp with common-mode feedback is shown. Assume all transistors are saturated, and assume M1 = M2 = M3 = M4 = M5. All transistors have W/L = 50. Ignore all capacitances except C_L.

\[ \text{V_B} \]

\[ \text{m3} \]

\[ \frac{C_L}{S_pF} \]

\[ \frac{C_L}{S_pF} \]

\[ \text{V_B} \]

\[ \text{m4} \]

\[ \text{m2} \]

\[ \text{m5} \]

\[ \text{in} \]

\[ \text{out} \]

\[ \text{5V} \]

\[ \text{3V} \]

\[ \text{100\mu A} \]

\[ \text{10\mu A} \]

\[ \text{10\mu A} \]

\[ \text{100\mu A} \]

\[ \text{100\mu A} \]

\[ -5V \]

\[ a) \text{ What is the DC drain current in M5? } I_D(M5) = \frac{120\mu A}{220\mu A} - 100\mu A \]
b) What is the differential-mode gain? \( \frac{v_{od}}{v_{id}} = \) 

\[ \frac{\pm \Delta v}{\Delta t} = \frac{N_{od}}{2} \frac{m_3}{m_1} \frac{N_{id}}{2} \]

\[ I_{b_1} = 110 \mu A \]
\[ I_{b_2} = 10 \mu A \]
\[ q_{m_1} = \sqrt{2(180 \mu A)(50)110 \mu A} = 1410 \mu A \]
\[ q_{m_3} = 4.25 \mu A \]

\[ \frac{N_{od}}{N_{id}} = q_{m_1} \left( \frac{1}{R_{o_3}} \cdot q_{m_3} \cdot R_{o_1} \right) = \]

\[ = (1410 \mu A) \cdot \left( \frac{1}{0.02 \cdot 10 \mu A} \right) \cdot (425 \mu A) \cdot \left( \frac{1}{0.02 \cdot 110 \mu A} \right) = 1.36 \Omega \]

c) What is the slew rate? \( \frac{d v_{od}}{dt} = \frac{44 V}{\mu s} = 44 \times 10^{-6} V \)

\[ \max I_{out} = 110 \mu A \]

flows thru two 5 pf caps

in series

\[ \Rightarrow \frac{d v_{od}}{dt} = \frac{I}{C} = \frac{110 \mu A}{2.5 pF} = 44 \frac{V}{\mu s} \]
A fully differential op amp with common-mode feedback is shown. Assume all transistors are saturated, and assume M1 = M2 = M3 = M4 = M5. All transistors have W/L = 50. Ignore all capacitances except C_L.

a) What is the DC drain current in M5? \( I_{D(M5)} = \frac{120}{\mu A} \)

\[ 220 \mu A - 100 \mu A \]
4. Use Blackman's impedance formula to compute the output resistance of the circuit below. Compute the return ratios with respect to the $g_m$ controlled source of $M_1$. Assume the transistor is saturated. Give the results in terms of $R_L$ and transistor parameters that could be computed, such as $g_m$, $r_o$, etc. Ignore all capacitances in this problem.

\[ V_{DD} \]
\[ V_{in} \]
\[ V_{out} \]
\[ R_L \]
\[ R_{out} \]

a) What is $R_{out}$ when $g_m(M_1) = 0$? $R_L \parallel r_o$

b) What is $RR(g_m(M_1)$ with output port open)? $g_m\left(\frac{r_o \parallel R_L}{r_o \parallel R_L}\right)$

\[ i_t(r_o \parallel R_L) = -N_X \]
\[ R_L \]
\[ r_o \]

\[ RR = -\frac{i_t}{i_t} = g_m\left(\frac{r_o \parallel R_L}{r_o \parallel R_L}\right) \]
c) What is \( \text{RR}(g_m(M1) \text{ with output port shorted})? \)

\[
\begin{align*}
\text{Short out} & \implies N_{out} = N_X = 0 \\
& \implies \text{no return current}
\end{align*}
\]

d) Now applying Blackman's formula, what is \( R_{out} \) of this feedback circuit?

\[
R_{out} = R_{01} || R_L \cdot \frac{1}{1 + g_m(R_{01} || R_L)}
\]

\[
\left( \approx \frac{1}{g_m} \quad \text{if} \quad g_m(R_{01} || R_L) \gg 1 \right)
\]