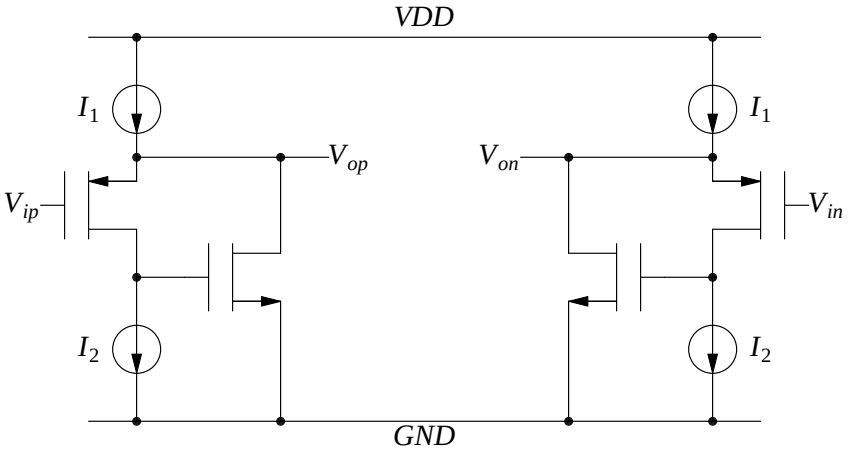
EEC 210 Project
Due: 5pm on Dec. 3, 2018.

REQUIREMENTS

The objective of this project is to design a differential output buffer with low power dissipation under the following conditions:

1. The differential buffer consists of two single-ended buffers, where one operates on the positive input and the other on negative input. Each single-ended buffer should use a "super source follower" configuration, which uses negative feedback to improve the buffer performance. (This circuit is covered in the text book.) The differential buffer schematic is shown below.



2. The circuit that operates on V_{ip} must be identical to the circuit that operates on V_{in}. (That is, the circuit should be symmetric or balanced.)
3. The only elements that you may use in your buffer are n- and p-channel MOS transistors.
4. I will post an HSPICE template file on the 210 web site. The template file specifies the names of the input nodes, output nodes, power-supply node, and bias-current input node of your buffer. The file also includes the inputs, output load, a power supply, a current source, and transistor models. The models represent the characteristics of transistors in a 0.4-µm, n-well, CMOS process. This means that p-channel transistors built in individual wells can be source-well connected to eliminate the body effect.
5. Your buffer should meet all specifications when driving a load of 15 kΩ in parallel with 8 pF between its output terminals (V_{op} to V_{on}).
6. The minimum drawn channel length is 0.5 µm.
7. For good matching, use unit elements. You may assume that there is no mismatch between identical devices.
8. Your buffer must meet all specifications with one power supply of value $V_{DD} = 4.5\ V$.
9. You may use the ideal 200 µA current source in the template file as the input to current mirror(s) that produce all the constant currents I_1 and I_2 required in your design.
10. Assume that the buffer must operate at room temperature only.
11. For each transistor in the buffer, you must specify not only the width (W) and length (L) of the gate, but also the area and perimeter of the source (AS and PS) and drain (AD and PD). Use the formulas and format given in the template file.

12. The key performance characteristics of the reference are its small-signal gain, output resistance, total harmonic distortion (THD), step response, and power dissipation.

    a. The small-signal gain, a_v, is defined here as $\frac{v_{op}}{v_{ip}} = \frac{v_{on}}{v_{in}}$, which is the gain of each half of the buffer by itself under small-signal conditions. Similarly, the output resistance, r_{out}, here is defined as the output resistance of each half of the buffer by itself. Both should be measured using the inputs and the .TF statement in the template file. The requirements are: $0.97 \le a_v \le 1.0$ and $r_{out} \le 10\ \Omega$.

    b. The THD should be measured on the differential output, $V_{od} = V_{op} - V_{on}$, with a .FOUR analysis. There isn't a specification for THD, but report the THD reported by HSPICE for a differential sinusoidal input of 4 V peak-to-peak at 1 MHz. This input is in the template file. Hopefully THD will be less than 0.5%, which is fairly low.

    c. The input for the step response test is given in the template file. The step response is characterized by two parameters: the final value and the overshoot. The final value, $V_{od\ fin}$, is defined as the final value of the differential output long after the step change. The overshoot, OS, is defined as: $\frac{V_{od\ \max}}{V_{od\ fin}}$, where $V_{od\ \max}$ is the maximum value of V_{od} during the step response. The requirements are: $1.94V \le V_{od\ fin} \le 2.0V$ for a 2-V differential input step (see the template file) and $0.95 \le OS \le 1.1$. The purpose of this test is to make sure that your buffer is stable.

13. To meet these requirements, you should consider the properties of the current mirrors presented in class to design current sources I_1 and I_2.

OPTIMIZATION

The goal of this project is to meet all requirements with a small power dissipation. The power dissipation, P_D, is defined here as the product of 4.5 V and the total current drawn from the 4.5-V supply with zero differential input.

REPORT (Please keep it short and turn in only these items.)

1. On the first page of your report, make a table that shows the values you obtained for a_v, r_{out}, THD, $V_{od\ fin}$, OS, and P_D.
2. Draw and label a circuit schematic and provide a copy of the corresponding SPICE input listing.
3. Address the following issues in a brief summary (no more than three one-sided pages):
    a. Describe your strategy to meet the specifications.
    b. Describe your strategy to minimize the P_D.
4. Attach only key SPICE outputs to your report.

GRADING (Your score will be determined by the following criteria)

Design Strategy	10%
Meeting Requirements	70%
Small P_D	10%
Report Organization and Completeness	10%