University of California, Davis
College of Engineering
Department of Electrical and Computer Engineering

EEC114 LABORATORY

I. OBJECTIVES AND GENERAL DIRECTIONS

The object of this laboratory is to reinforce the EEC114 lecture material, to teach the use of basic lab equipment, to teach laboratory skills, both general and troubleshooting, and to develop good experimental note-taking habits. You should purchase a bound lab notebook, preferably one with grid lines. All your pre-lab calculations, lab notes, data, and reports should be kept in the lab notebook. Lab reports need not repeat information that is published in this lab manual. However, your lab notebook and manual together should contain enough information to repeat the experiments. It will be graded at the end of each experiment.

To simplify the grading process, the lab manual includes a page to summarize the results from each experiment. These pages are included at the end of the lab manual. The appropriate summary page should be attached to the beginning of each lab report in your lab notebook. All requested information, both experimental results and calculated values, should be copied onto this page. Any items left blank on the summary page will receive no credit. All corresponding calculations, required graphs and measurements of the lab along with any notes on the various circuits should appear in the report following the results page. Items appearing on the summary page without supporting calculations in the body of the report will also receive no credit. Any questions in the lab instructions should be answered at the END of the report.

II. PREPARATION FOR LABS

Time spent in the lab is to be used building and testing circuits, NOT learning the lab material and calculating circuit values. Read the labs and do any required calculations before coming to the lab.

III. BASIC LAB GROUND RULES

The work area in the lab must be left in the following condition at the end of the lab period:

(1) All test equipment neatly placed on the bench.
(2) All components replaced in their proper boxes or drawers in the storage cabinet.
(3) Wires hung up neatly on the wall in their proper section.

IV. LAB BOOK WRITE UPS

Each student will turn in a separate lab report that was prepared *completely* by the student himself/herself. You will work in pairs in the laboratory to obtain your data and then individually to prepare your lab report.

V. GRADING

Grading will be based on:

(1) pre-lab calculations (where applicable)
(2) lab report
(3) student's lab skills
(4) lab demonstrations

VI. PROJECT

A design project will be assigned during the second half of the quarter.

Acknowledgment - The EEC114 laboratory experiments were written by P. Chan, P. Gray, P. Hurst, R. Levinson and J. Pierret .

CA3045, CA3046 Types

General-Purpose Transistor Arrays For Low-Power Applications at Frequencies from DC through the VHF Range

THREE ISOLATED TRANSISTORS AND ONE DIFFERENTIALLY-CONNECTED TRANSISTOR PAIR

The CA3045 and CA3046 each consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

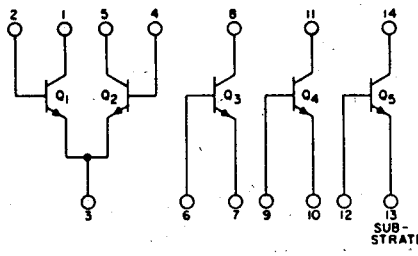


Fig. 1 - Schematic diagram. Note that the substrate (pin 13) must be connected to the lowest supply voltage.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

	CA3045		CA3045F, CA3046		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A up to 55°C	–	–	300	750	mW
T_A > 55°C	–	–	Derate at 6.67		mW/°C
T_A up to 75°C	300	750	–	–	mW
T_A > 75°C	Derate at 8		–	–	mW/°C
Collector-to-Emitter Voltage, V_{CEO}	15	–	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	5	–	V
Temperature Range:					
Operating	−55 to +125		−55 to +125		°C
Storage	−65 to +150		−65 to +150		°C
Lead Temperature (During Soldering): At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max:	+265		+265		°C

*The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	-	100	-	-
		V_{CE} = 3 V, I_C = 1 mA	40	100	-	-
		V_{CE} = 3 V, I_C = 10 μA	-	54	-	-
Input Offset Current for Matched Pair Q_1 and Q_2	$\lvert I_{IO_1} - I_{IO_2} \rvert$	V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA	-	0.715	-	V
		V_{CE} = 3 V, I_E = 10 mA	-	0.800	-	
Magnitude of Input Offset Voltage for Differential Pair	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors	$\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$	V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	−1.9	-	mV °C
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} 3 V, I_C 1 mA	-	1.1	-	μV°C

FEATURES

- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- 5 general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz
- Full military temperature range for CA3045
  -55 to +125°C
- The CA3045 is available in a sealed-junction Beam-Lead version (CA3045L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

APPLICATIONS

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

STATIC CHARACTERISTICS

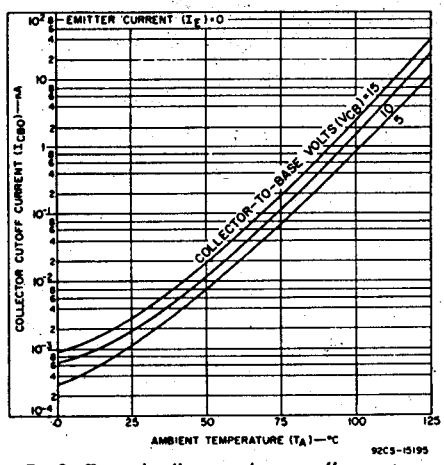


Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

CA3045, CA3046 Types

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS
DYNAMIC CHARACTERISTICS						
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF

STATIC CHARACTERISTICS

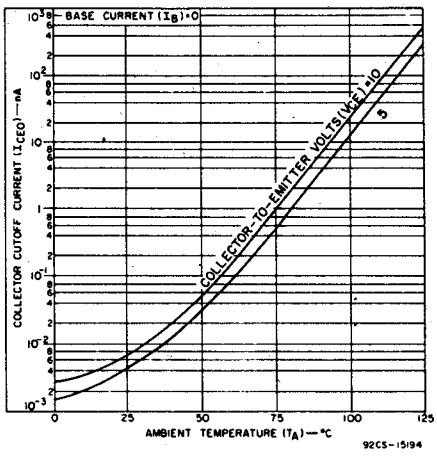


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

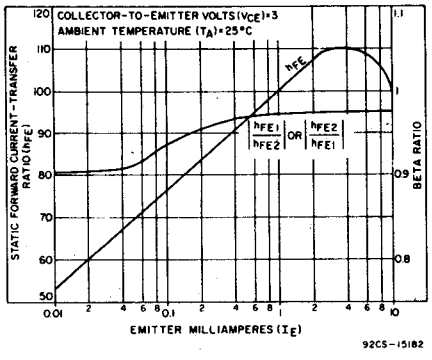


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

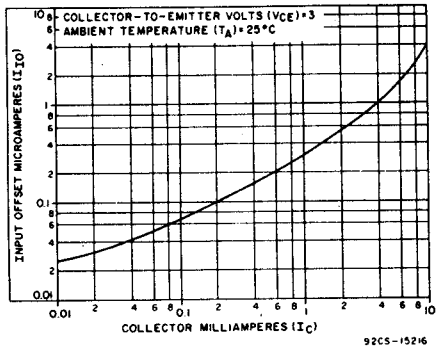


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

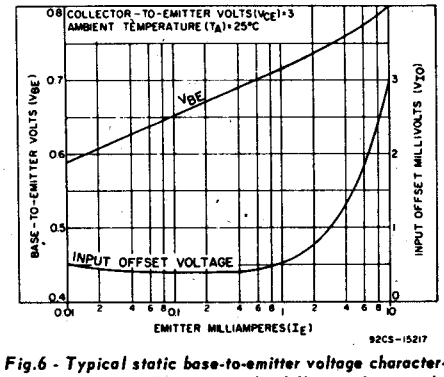


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

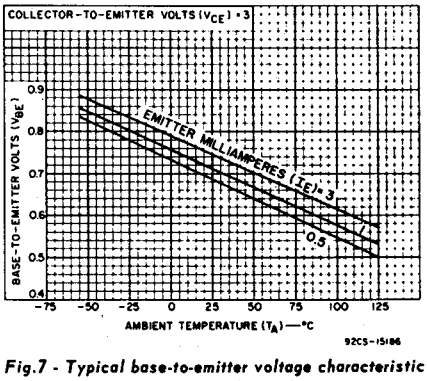


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

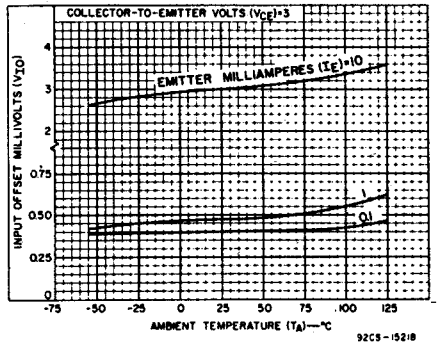


Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

CA3045, CA3046 Types

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

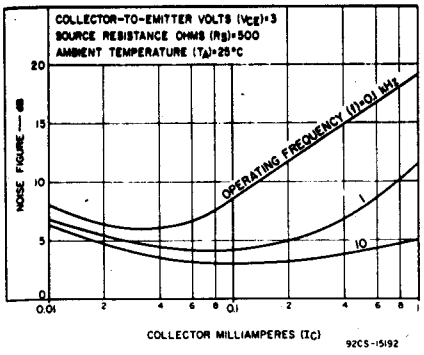


Fig.9(a) - Typical noise figure vs collector current.

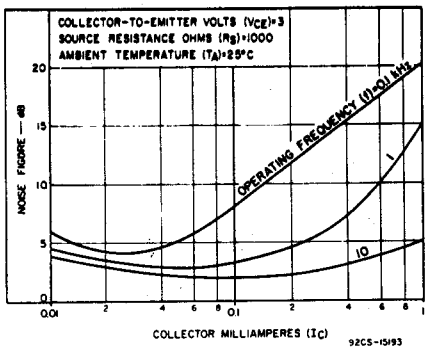


Fig.9(b) - Typical noise figure vs collector current.

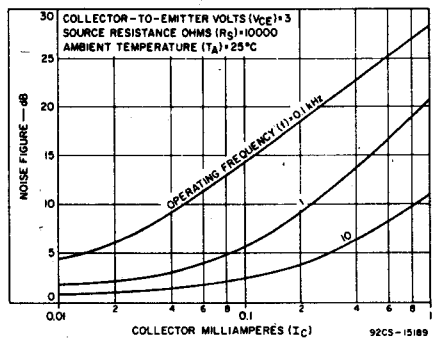


Fig.9(c) - Typical noise figure vs collector current.

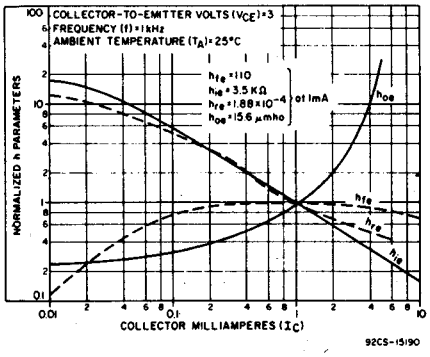


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

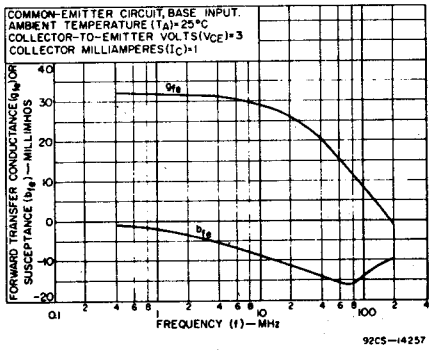


Fig.11 - Typical forward transfer admittance vs frequency.

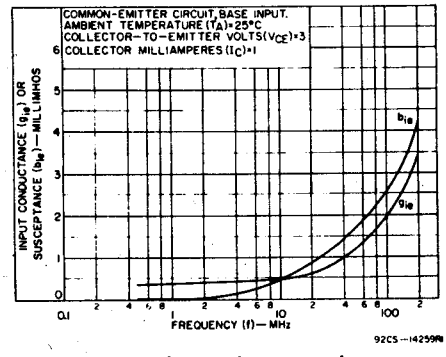


Fig.12 - Typical input admittance vs frequency.

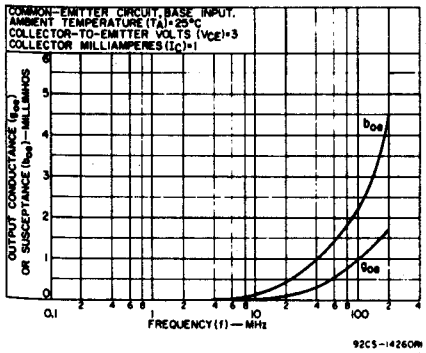


Fig.13 - Typical output admittance vs frequency.

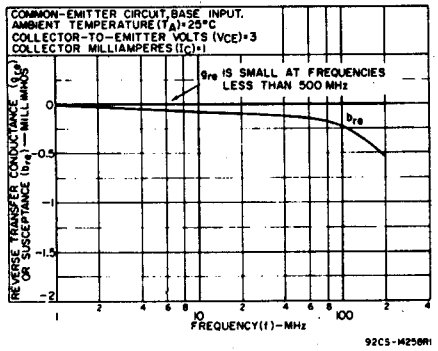


Fig.14 - Typical reverse transfer admittance vs frequency.

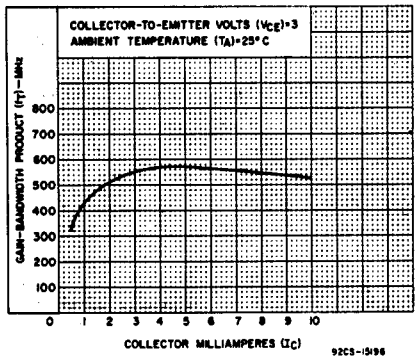


Fig.15 - Typical gain-bandwidth product vs collector current.

CA3086
General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially— Connected Transistor Pair

For Low—Power Applications from DC to 120MHz

RCA-CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

Applications

- General-purpose use in signal processing systems operating in the DC to 120-MHz range
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

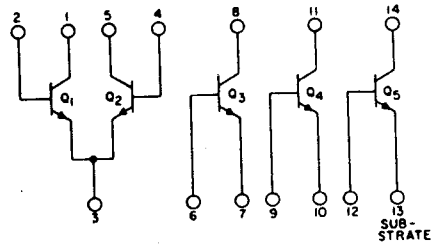


Fig. 1 - Schematic diagram. Note that the substrate (pin 13) must be connected to the lowest supply voltage.

MAXIMUM RATINGS, Absolute—Maximum Values at T_A = 25°C

DISSIPATION:		
Any one transistor	300	mW
Total package up to T_A = 55°C	750	mW
Above T_A = 55°C	derate linearly 6.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−55 to + 125	°C
Storage	−65 to + 150	°C
LEAD TEMPERATURE (During soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) From case for 10 seconds max.	+ 265	°C
The following ratings apply for each transistor in the device:		
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	20	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}*	20	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT, I_C	50	mA

* The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	Typ. Characteristic Curves Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	—	20	60	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	—	15	24	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	—	20	60	—	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	—	5	7	—	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	2	—	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	3	—	See Curve	5	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 1mA	4	40	100	—	

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

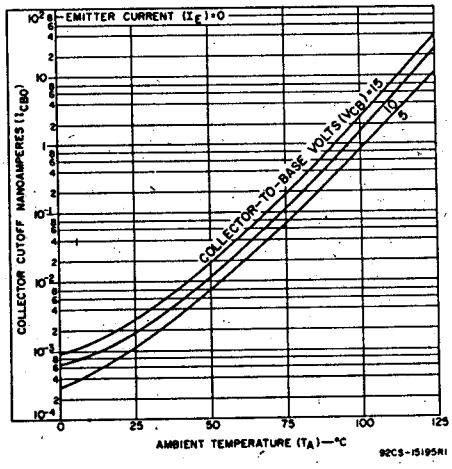


Fig.2– I_{CBO} vs T_A.

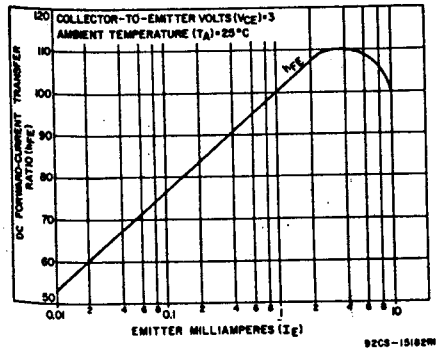


Fig.3– h_{FE} vs I_E.

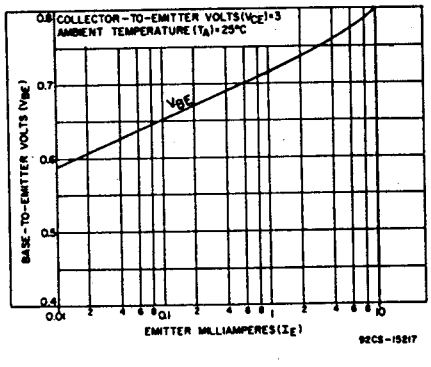


Fig.4 V_{BE} vs I_E.

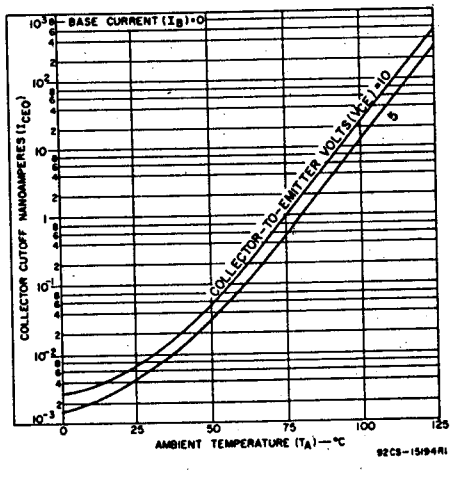


Fig.5– I_{CEO} vs T_A.

CA3086

ELECTRICAL CHARACTERISTICS at T_A = 25°C Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		–	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1k Ω		–	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	–
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8×10^{-4}	–
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 − j1.5	mmho
Input Admittance	Y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	Y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	Y_{re}			11	See Curve	–
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		–	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		–	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		—	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

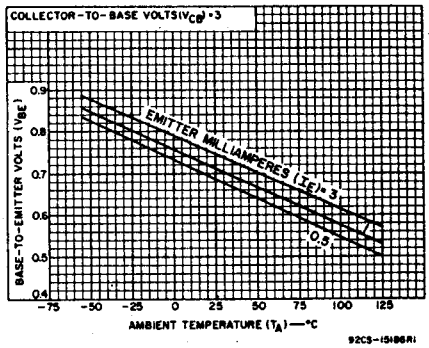


Fig.6 – V_{BE} vs T_A.

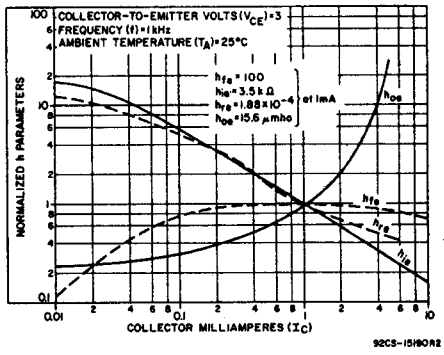


Fig.7 – Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

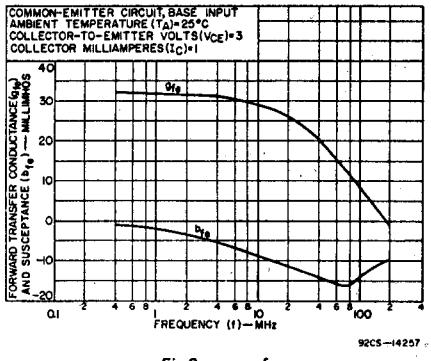


Fig.8 – y_{fe} vs f.

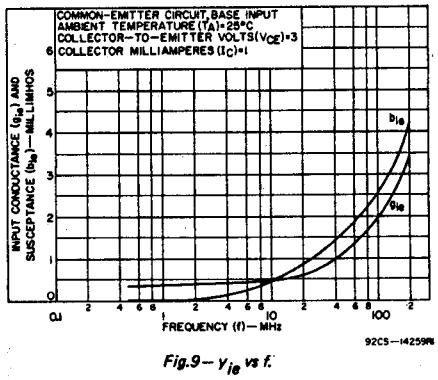


Fig.9 – y_{ie} vs f.

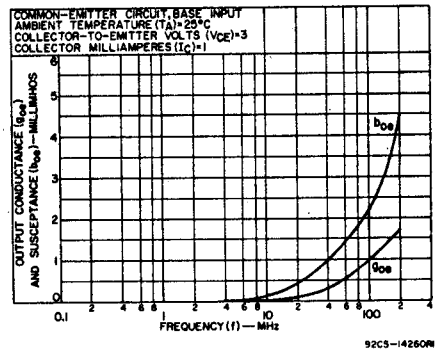


Fig.10 – y_{oe} vs f.

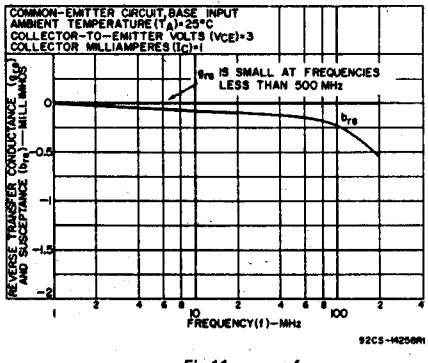


Fig.11 – y_{re} vs f.

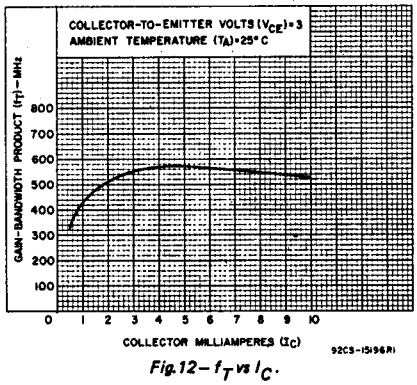


Fig.12 – f_T vs I_C.

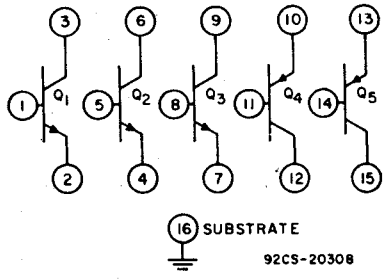
CA3096E, CA3096AE

N-P-N/P-N-P Transistor-Array IC

RCA-CA3096E and CA3096AE are general-purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096AE and CA3096E are identical, except that the CA3096AE specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and $V_{CE(SAT)}$ (see Table I).

CA3096E and CA3096AE are supplied in 16-lead dual-in-line plastic packages.



Schematic Diagram

TABLE I—CA3096AE AND CA3096E ESSENTIAL DIFFERENCES*

RCA TYPE	I_{CBO} (nA)		I_{CEO} (nA)		$V_{CE(SAT)}$ (V)		$\lvert V_{IO}\rvert$ (mV)		$\lvert I_{IO}\rvert$ (μA)	
	n-p-n	p-n-p	n-p-n	p-n-p	n-p-n	p-n-p	n-p-n	p-n-p	n-p-n	p-n-p
CA3096AE	40	−40	100	−100	0.7	0.4	5	5	0.6	0.25
CA3096E	100	−100	1000	−1000	1.0	0.7	–	–	–	–

* Maximum values.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (For Equipment Design)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	CA3096AE, CA3096E LIMITS			UNITS
			Min.	Typ.	Max.	
For Each n-p-n Transistor:						
Collector-Cutoff Current (CA3096AE)	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.0013	40	nA
Collector-Cutoff Current (CA3096AE)	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.0055	100	nA
Collector-Cutoff Current (CA3096E)	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.0013	100	nA
Collector-Cutoff Current (CA3096E)	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.0055	1	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	35	50	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	45	100	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10 μA, I_B = I_E = 0	45	100	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	6	8	–	V
Emitter-to-Base Zener Voltage	V_Z	I_Z = 10 μA	6	7.9	9.8	V
Collector-to-Emitter Saturation Voltage (CA3096AE)	$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA	–	0.24	0.5	V
Collector-to-Emitter Saturation Voltage (CA3096E)	$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA	–	0.24	0.7	V
Base-to-Emitter Voltage	V_{BE}	I_C = 1 mA, V_{CE} = 5 V	0.6	0.69	0.78	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = 1 mA, V_{CE} = 5 V	150	390	500	
Magnitude of Temperature Coefficient: V_{BE} (for each transistor)	$\lvert\Delta V_{BE}/\Delta T\rvert$	I_C = 1 mA, V_{CE} = 5 V	–	−1.9	–	mV/°C
For Each p-n-p Transistor:						
Collector-Cutoff Current (CA3096AE)	I_{CBO}	V_{CB} = −10 V, I_E = 0	–	−0.055	40	nA
Collector-Cutoff Current (CA3096AE)	I_{CEO}	V_{CE} = −10 V, I_B = 0	–	−0.12	100	nA
Collector-Cutoff-Current (CA3096E)	I_{CEO}	V_{CE} = −10 V, I_B = 0	–	−0.12	1	μA
Collector-Cutoff-Current (CA3096E)	I_{CBO}	V_{CB} = −10 V, I_E = 0	–	−0.055	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = −100 μA, I_B = 0	−40	−75	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = −10 μA, I_E = 0	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = −10 μA, I_C = 0	−40	−100	–	V
Emitter-to-Base Zener Voltage	V_Z	I_Z = 10 μA	10	16	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 10 μA, I_B = I_C = 0	40	100	–	V
Collector-to-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = −1 mA, I_B = −100 μA	–	−0.16	−0.4	V
Base-to-Emitter Voltage	V_{BE}	I_C = −100 μA, V_{CE} = −5 V	−0.5	−0.6	−0.7	V
DC Forward-Current Transfer Ratio	h_{FE}	I_C = −100 μA, V_{CE} = −5 V	40	85	200	
		I_C = −1 mA, V_{CE} = −5 V	20	47	150	
Magnitude of Temperature Coefficient: V_{BE} (for each transistor)	$\lvert\Delta V_{BE}/\Delta T\rvert$	I_C = −100 μA, V_{CE} = −5 V	–	−2.2	–	mV/°C
For Transistors Q1 and Q2 (As a Differential Amplifier): CA3096AE ONLY						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 5 V, I_C = 1 mA	–	0.3	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		–	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$		–	1.1		μV/°C
For Transistors Q4 and Q5 (As a Differential Amplifier): CA3096AE ONLY						
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = −5 V, I_C = −100 μA, R_S = 0	–	0.15	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		–	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$		–	0.54	–	μV/°C

Features:

- **Matched General-Purpose Transistors (CA3096AE Only)**
- **Input Offset Voltage ± 5 mV**
- **Input Offset Current:**
  - **p-n-p Pair ± 250 nA max. @ I_C = −100 μA**
  - **n-p-n Pair ± 0.6 μA max. @ I_C = 1 mA**
- **High h_{FE}**
  - **n-p-n transistor: 150 min. @ I_C = 1 mA**
  - **p-n-p transistor: 40 min. @ I_C = 100 μA**
- **High Breakdown Voltages:**
  - **n-p-n transistor: $V_{(BR)CEO}$ = 35 V min; $V_{(BR)CBO}$ = 45 V min.**
  - **p-n-p transistor: $V_{(BR)CEO}$ = 40 V min; $V_{(BR)CBO}$ = 40 V min.**
- **Separate Substrate Connection**
- **Low Noise Figure:**
  - **n-p-n transistor: 2.2 dB typ. at 1 kHz**
  - **p-n-p transistor: 3 dB typ. at 1 kHz**

Applications:

- **Differential Amplifiers**
- **DC Amplifiers**
- **Sense Amplifiers**
- **Level Shifters**
- **Timers**
- **Lamp and Relay Drivers**
- **Thyristor Firing Circuits**
- **Temperature-Compensated Amplifiers**
- **Operational Amplifiers**

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

		Each n-p-n Transistor	Each p-n-p Transistor	
Collector-to-Emitter Voltage	V_{CEO}	35	−40	V
Collector-to-Base Voltage	V_{CBO}	45	−40	V
Collector-to-Substrate Voltage	V_{CIO}	45	45	V
Emitter-to-Base Voltage	V_{EBO}	6	−40	V
Collector Current	I_C	50	−10	mA
Dissipation P_D:				
Up to T_A = 55 °C:				
Device (Total)		750		mW
Each Transistor		200		mW
Above T_A = 55 °C		Derate Linearly 6.67		mW/°C
Temperature Range:				
Operating		−55 to +125		°C
Storage		−65 to +150		°C
Lead Temperature (During Soldering) At distance 1/16 ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.		265		°C

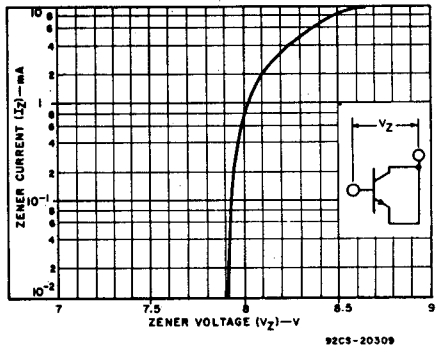


Fig.1—Base-to-emitter zener characteristic (n-p-n).

CA3096E, CA3096AE

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor				
Noise Figure (low frequency)	NF	f = 1 kHz, V_{CE} = 5 V, I_C = 1 mA, R_S = 1 kΩ	2.2	dB
Low-Frequency, Input Resistance	R_i	f = 1.0 kHz, V_{CE} = 5 V, I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance	R_o		80	kΩ
Admittance Characteristics:		f = 1 MHz, V_{CE} = 5 V, I_C = 1 mA		
Forward Transfer Admittance	$\frac{9fe}{Yfe\ bfe}$		7.5	mmho
			−j13	
Input Admittance	$\frac{9ie}{Yie\ bie}$		2.2	mmho
			j3.1	
Output Admittance	$\frac{9oe}{Yoe\ boe}$		0.76	mmho
			j2.4	
Gain-Bandwidth Product	f_T	V_{CE} = 5 V, I_C = 1.0 mA	280	MHz
		V_{CE} = 5 V, I_C = 5 mA	335	
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V	0.75	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V	0.46	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 3 V	3.2	pF
For Each p-n-p Transistor				
Noise Figure (low frequency)	NF	f = 1 kHz, I_C = 100 μA, R_S = 1 kΩ	3	dB
Low-Frequency Input Resistance	R_i	f = 1 kHz, V_{CE} = 5 V, I_C = 100 μA	27	kΩ
Low-Frequency Output Resistance	R_o		680	kΩ
Gain-Bandwidth Product	f_T	V_{CE} = 5 V, I_C = 100 μA	6.8	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = −3 V	0.85	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = −3 V	2.25	pF
Base-to-Substrate Capacitance	C_{BI}	V_{BI} = 3 V	3.05	pF

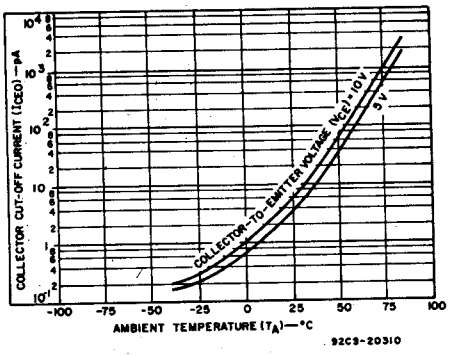


Fig.2—Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

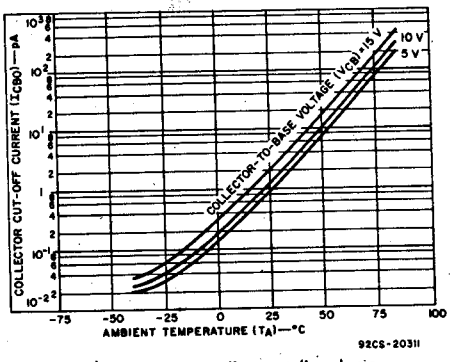


Fig.3—Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

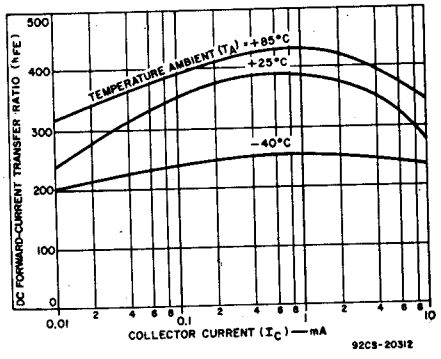


Fig.4—Transistor (n-p-n) h_{FE} as a function of collector current.

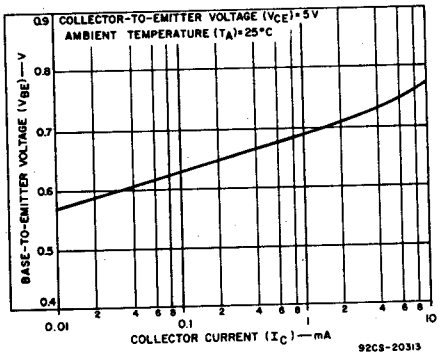


Fig.5—V_{BE} (n-p-n) as a function of collector current.

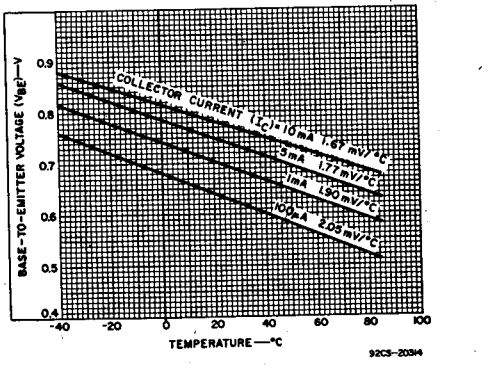


Fig.6—V_{BE} (n-p-n) as a function of temperature.

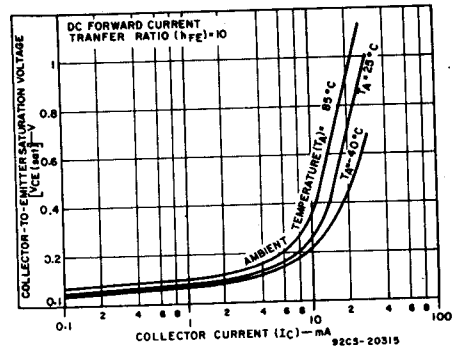


Fig.7—$V_{CE(SAT)}$ (n-p-n) as a function of collector current.

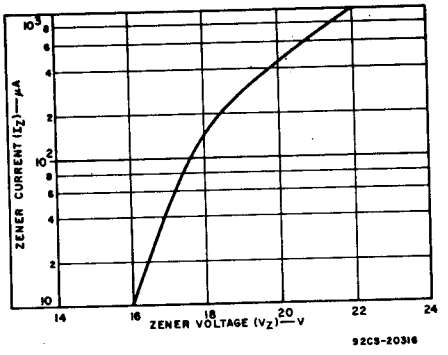


Fig.8—Base-to-emitter zener characteristic (p-n-p).

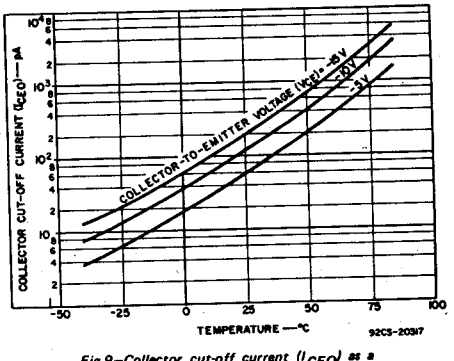


Fig.9—Collector cut-off current (I_{CEO}) as a function of temperature (p-n-p).

CA3096E, CA3096AE

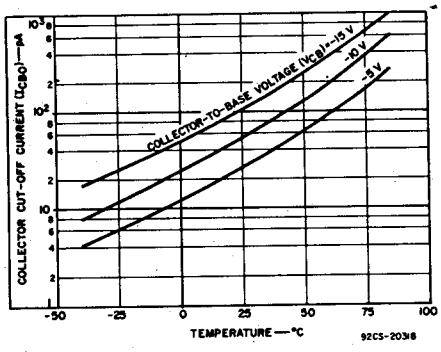


Fig.10—Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

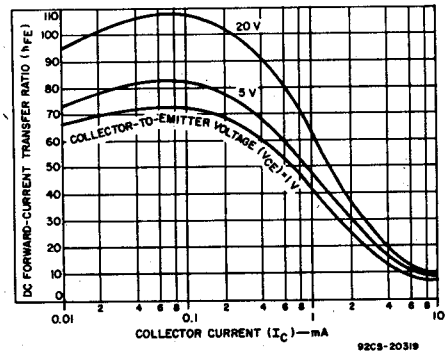


Fig.11—Transistor (p-n-p) h_{FE} as a function of collector current.

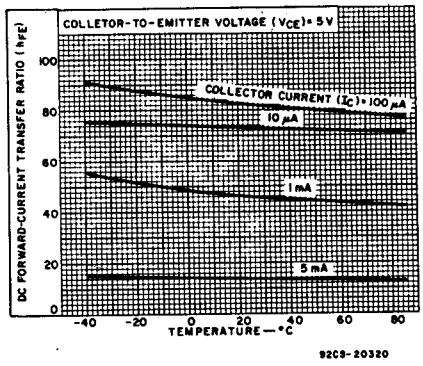


Fig.12—Transistor (p-n-p) h_{FE} as a function of temperature.

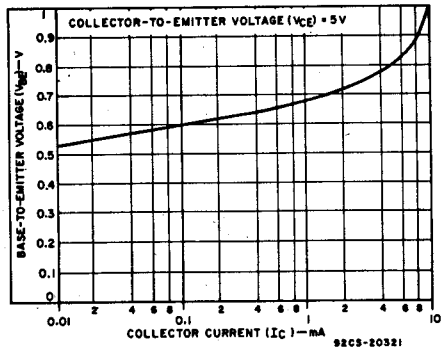


Fig.13—V_{BE} (p-n-p) as a function of collector current.

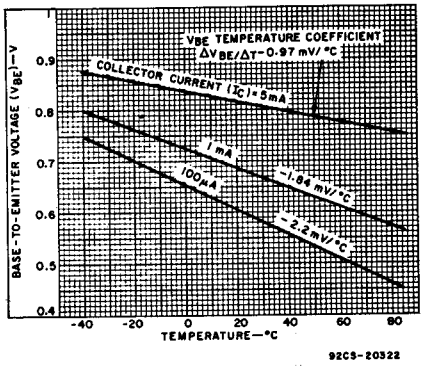


Fig.14—V_{BE} (p-n-p) as a function of temperature.

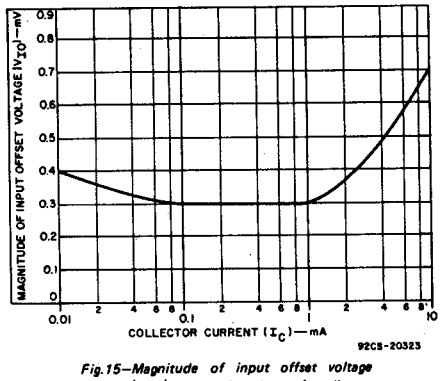


Fig.15—Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor Q_1–Q_2.

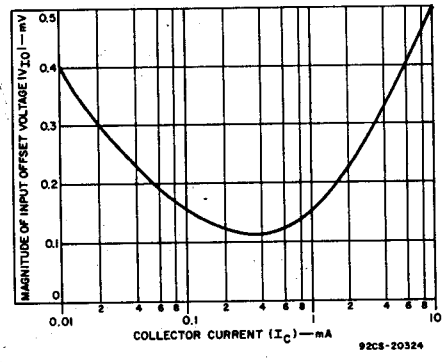


Fig.16—Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistors Q_4–Q_5.

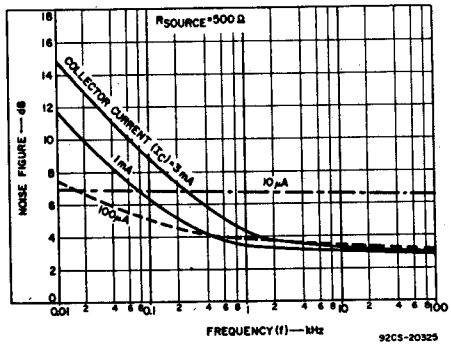


Fig.17—Noise figure as a function of frequency for n-p-n transistors.

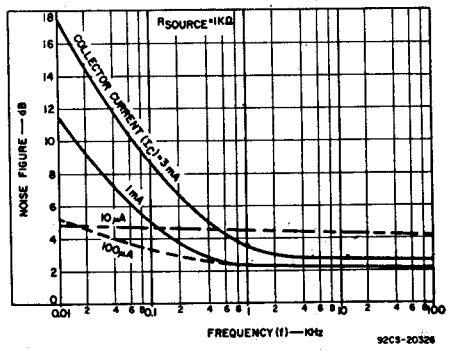


Fig.18—Noise figure as a function of frequency for n-p-n transistors.

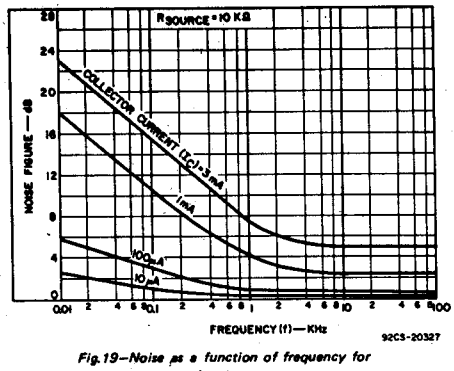


Fig.19—Noise as a function of frequency for n-p-n transistors.

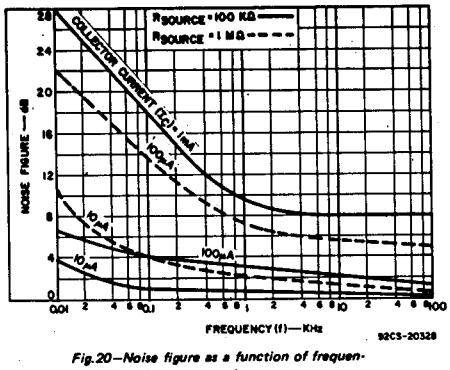


Fig.20—Noise figure as a function of frequency for n-p-n transistors.

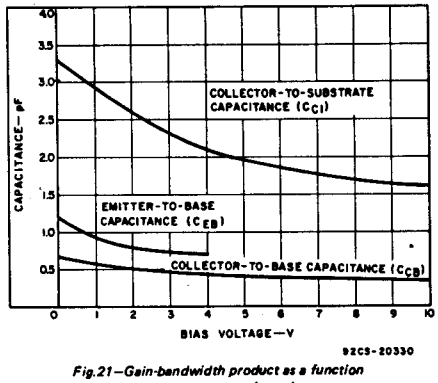


Fig.21—Gain-bandwidth product as a function of collector current (n-p-n).

CA3096E, CA3096AE

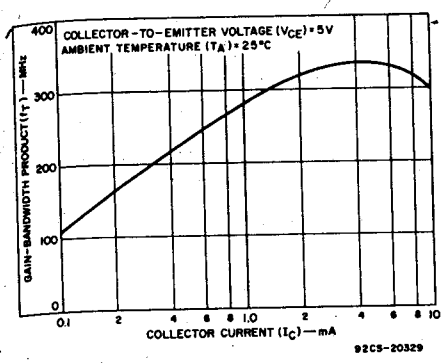


Fig.22—Capacitance as a function of bias voltage (n-p-n).

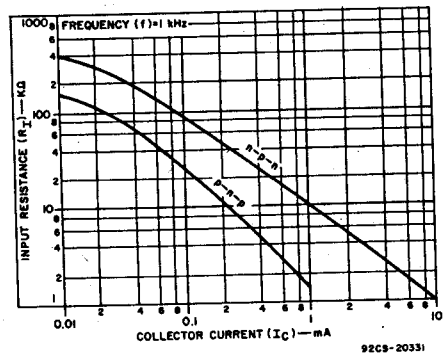


Fig.23—Input resistance as a function of collector current.

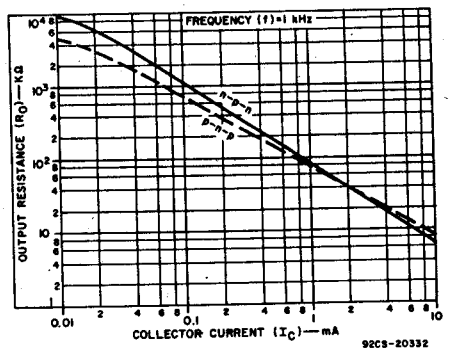


Fig.24—Output resistance as a function of collector current.

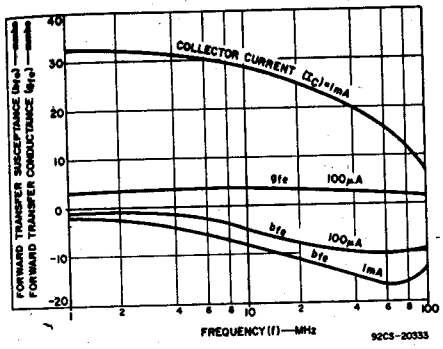


Fig.25—Forward transconductance as a function of frequency.

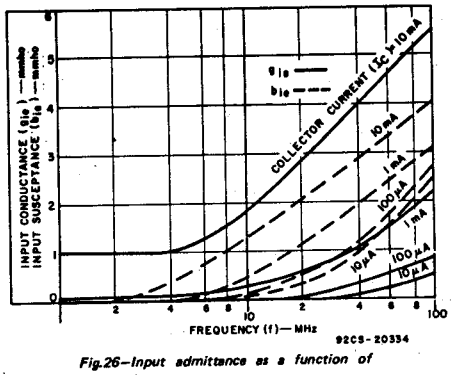
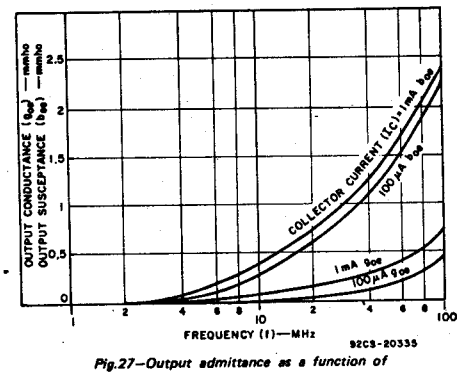


Fig.26—Input admittance as a function of frequency.



Pig.27—Output admittance as a function of frequency.

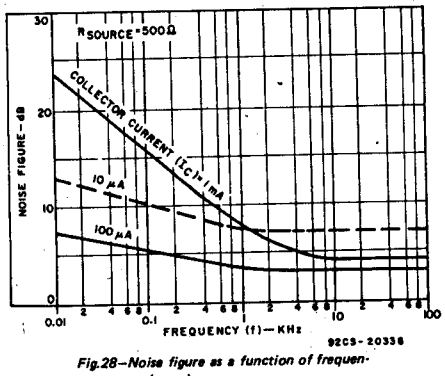


Fig.28—Noise figure as a function of frequency (p-n-p).

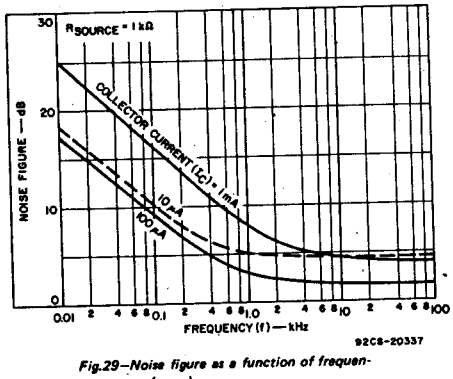


Fig.29—Noise figure as a function of frequency (p-n-p).

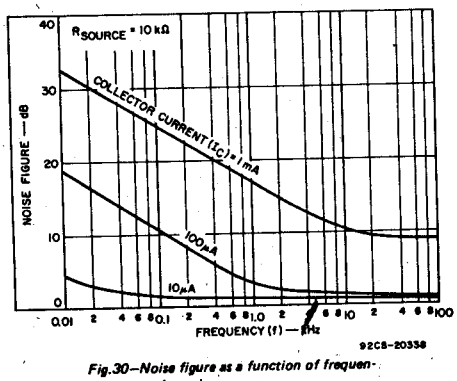


Fig.30—Noise figure as a function of frequency (p-n-p).

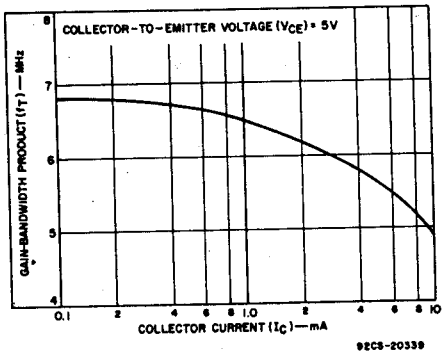


Fig.31—Gain-bandwidth product as a function of collector current (p-n-p).

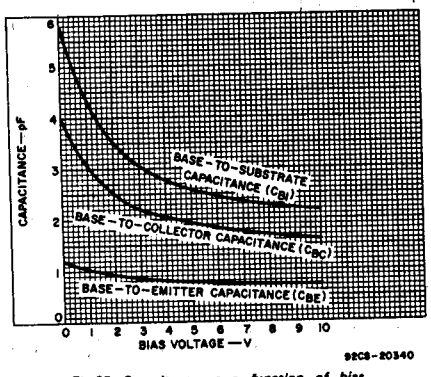


Fig.32—Capacitance as a function of bias voltage (p-n-p).

For application information, see Data Bulletin File No. 595.

CA741, CA747, CA748, CA1458, CA1558 Types

Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commercial Applications

"G" Suffix Types—Hermetic Gold-CHIP in Dual-In-Line Plastic Package
"E" Suffix Types—Standard Dual-In-Line Plastic Package
"T" and "S" Suffix Types—TO-5 Style Package

The RCA-CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 10); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747CG, CA747E, CA747G (See Fig. 9); and types CA1458, CA1558, CA747CT, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

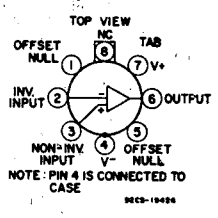
RCA's manufacturing process makes it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your RCA Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

Features:

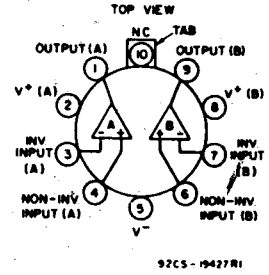
- Input bias current (all types): 500 nA max.
- Input offset current (all types): 200 nA max.

Applications:

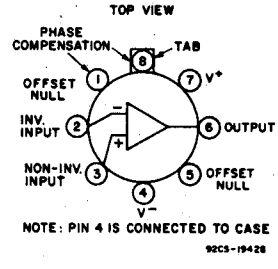
- Comparator
- DC amplifier
- Integrator or differentiator
- Multivibrator
- Narrow-band or band-pass filter
- Summing amplifier



1a.—CA741CS,CA741CT,CA741S, & CA741T with internal phase compensation.



1b.—CA747CT and CA747T with internal phase compensation.



1c.—CA748CS, CA748CT,CA748S, and CA748T with external phase compensation.

Fig. 1 — Functional diagrams.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C:*

DC Supply Voltage (between V^+ and V^- terminals):	
CA741C, CA747C▲, CA748C, CA1458▲	36 V
CA741, CA747▲, CA748, CA1558▲	44 V
Differential Input Voltage	±30 V
DC Input Voltage*	±15 V
Output Short-Circuit Duration	Indefinite
Device Dissipation:	
Up to 70°C (CA741C, CA748C)	500 mW
Up to 75°C (CA741, CA748)	500 mW
Up to 30°C (CA747)	800 mW
Up to 25°C (CA747C)	800 mW
Up to 30°C (CA1558)	680 mW
Up to 25°C (CA1458)	680 mW
For Temperatures Indicated Above	Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^- (CA741C, CA741, CA747CE, CA747CG)	±0.5 V
Ambient Temperature Range:	
Operating – CA741, CA747E, CA748, CA1558	−55 to +125 °C
CA741C, CA747C, CA748C, CA1458	0 to +70 °C†
Storage	−65 to +150 °C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265 °C

* If Supply Voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

▲ Voltage values apply for each of the dual operational amplifiers.

† All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)
CA1458	dual	int.	no	20k	6	0 to +70▲
CA1558	dual	int.	no	50k	5	−55 to +125
CA741C	single	int.	yes	20k	6	0 to +70▲
CA741	single	int.	yes	50k	5	−55 to +125
CA747C	dual	int.	yes*	20k	6	0 to +70▲
CA747	dual	int.	yes*	50k	5	−55 to +125
CA748C	single	ext.	yes	20k	6	0 to +70▲
CA748	single	ext.	yes	50k	5	−55 to +125

*In the 14-lead dual-in-line plastic package only.

▲All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

Type No.	PACKAGE TYPE AND SUFFIX LETTER										FIG. No.
	TO-5 STYLE			PLASTIC		Gold-CHIP PLASTIC		CHIP	Gold-CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L	8L	14L				
CA1458	T		S	E		G		H	GH		1d, 1h
CA1558	T		S	E		G					1d, 1h
CA741C	T		S	E		G		H	GH		1a, 1e
CA741	T		S	E		G				L	1a, 1e
CA747C		T			E		G	H	GH		1b, 1f
CA747		T			E		G				1b, 1f
CA748C	T		S	E		G		H	GH		1c, 1g
CA748	T		S	E		G					1c, 1g

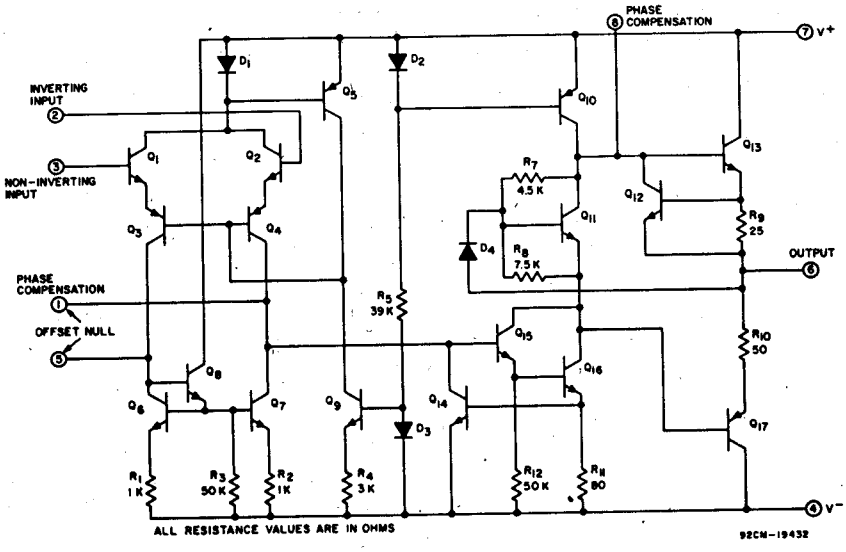
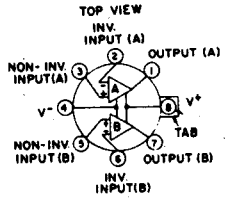
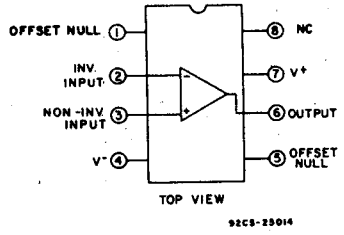


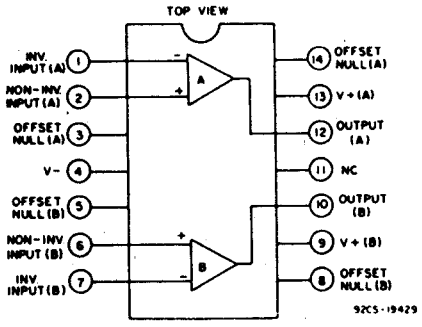
Fig. 2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.



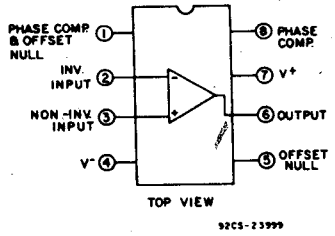
1d.—CA1458S,CA1458T,CA1558S, and CA1558T and internal phase compensation.



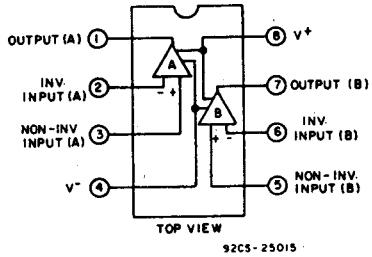
1e.—CA741CE,CA741CG,CA741E, and CA741G with internal phase compensation.



1f.—CA747CE,CA747CG,CA747E, and CA747G with internal phase compensation.



1g.—CA748CE,CA748CG,CA748E, and CA748G with external phase compensation.



1h.—CA1458E,CA1458G,CA1558E, and CA1558G with internal phase compensation.

Fig. 1 — Functional Diagrams (Cont'd)

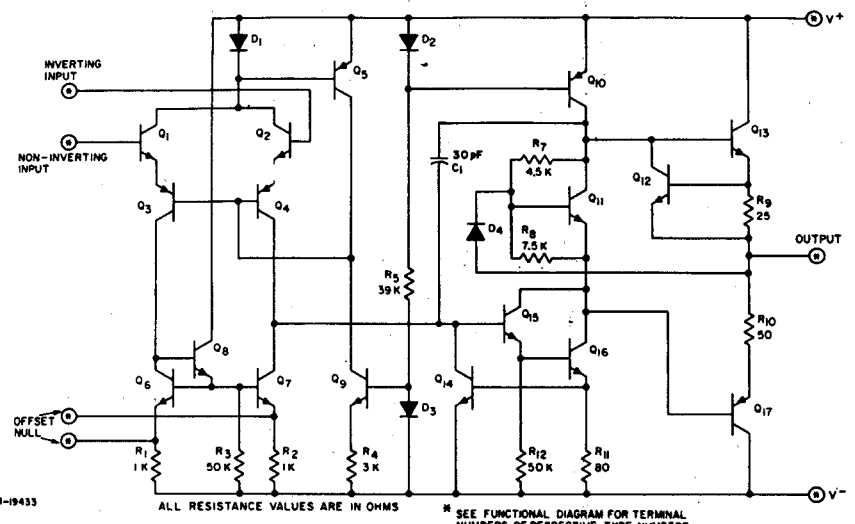


Fig.3—Schematic diagram of operational amplifiers with internal phase compensation for CA741C, CA741, and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

ELECTRICAL CHARACTERISTICS

For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V	Ambient Temperature, T_A	LIMITS CA741 CA747* CA748 CA1558*			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	$R_S = \leq 10\,k\Omega$	25 °C	–	1	5	mV
		−55 to +125 °C	–	1	6	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		−55 °C	–	85	500	
		+125 °C	–	7	200	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		−55 °C	–	300	1500	
		+125 °C	–	30	500	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$ $V_O = \pm 10$ V	25 °C	50,000	200,000	–	
		−55 to +125 °C	25,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		−55 to +125 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	70	90	–	dB
Supply Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	−55 to +125 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	−55 to +125 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
		−55 °C	–	2	3.3	
		+125 °C	–	1.5	2.5	
Device Dissipation, P_D		25 °C	–	50	85	mW
		−55 °C	–	60	100	
		+125 °C	–	45	75	

* Values apply for each section of the dual amplifiers.

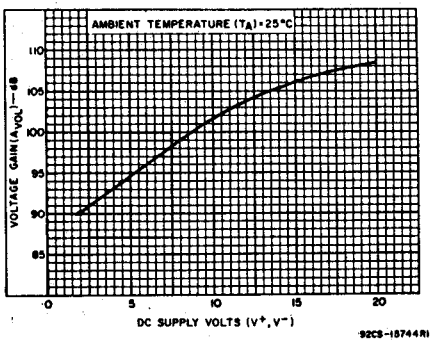


Fig.4—Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

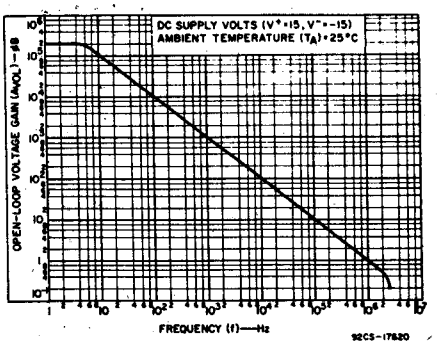


Fig.5—Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

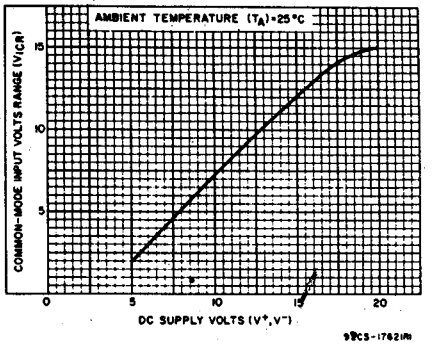


Fig.6—Common-mode input voltage range vs. supply voltage for all types.

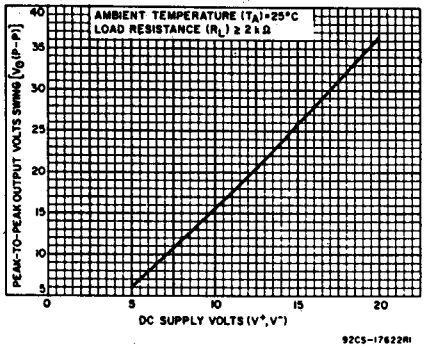


Fig.7—Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C.

CA741, CA747, CA748, CA1458, CA1558 Types

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V	Ambient Temperature, T_A	LIMITS CA741C CA747C* CA748C CA1458* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S = \leq 10\,k\Omega$	25 °C	–	2	6	mV
		0 to 70 °C	–	–	7.5	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		0 to 70 °C	–	–	300	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		0 to 70 °C	–	–	800	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$, $V_O = \pm 10$ V	25 °C	20,000	200,000	–	
		0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\,k\Omega$	25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	25 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	25 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	25 °C	±10	±13	–	
		0 to 70 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
Device Dissipation, P_D		25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS $V\pm = \pm 15$ V	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance, R_O		75	Ω
Output Short-Circuit Current		25	mA
Transient Response: Rise Time, t_r	Unity gain, $V_I = 20$ mV, $R_L = 2\,k\Omega$, $C_L \leq 100$ pF	0.3	μs
Transient Response: Overshoot		5	%
Slew Rate, SR: Closed-loop	$R_L \geq 2\,k\Omega$	0.5	V/μs
Slew Rate, SR: Open-loop▲		40	V/μs

▲ Open-loop slew rate applies only for types CA748C and CA748.

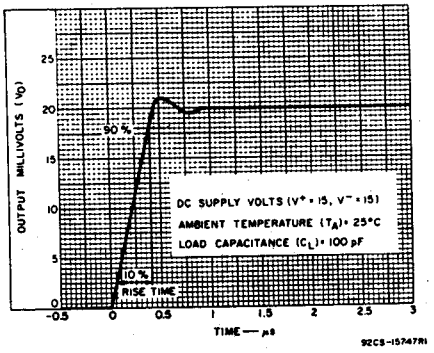


Fig.8—Output voltage vs. transient response time for CA741C and CA741.

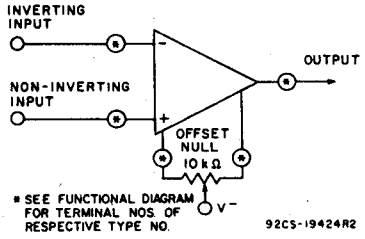


Fig.9—Voltage-offset null circuit for CA741C, CA741, CA747CE, CA747CG, CA747E, and CA747G.

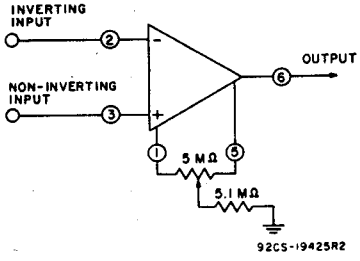


Fig.10—Voltage-offset null circuit for CA748C and CA748.

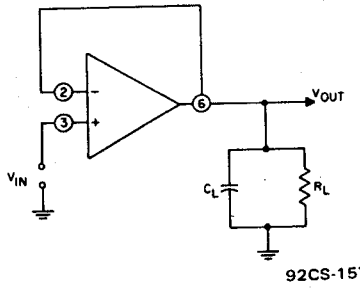


Fig.11—Transient response test circuit for all types.

TYPES 2N3905, 2N3906, A5T3905, A5T3906
P-N-P SILICON TRANSISTORS

BULLETIN NO. DL-S 7311577, NOVEMBER 1971—REVISED MARCH 1973

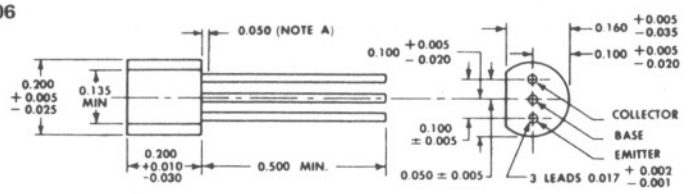
SILECT† TRANSISTORS‡
FOR GENERAL PURPOSE SATURATED-SWITCHING AND AMPLIFIER APPLICATIONS

- **For Complementary Use with N-P-N Types 2N3903, 2N3904, A5T3903, and A5T3904**
- **Rugged One-Piece Construction with In-Line Leads or Standard TO-18 100-mil Pin-Circle Configuration**

mechanical data

These transistors are encapsulated in a plastic compound specifically designed for this purpose, using a highly mechanized process developed by Texas Instruments. The case will withstand soldering temperatures without deformation. These devices exhibit stable characteristics under high-humidity conditions and are capable of meeting MIL-STD-202C, Method 106B. The transistors are insensitive to light.

2N3905, 2N3906

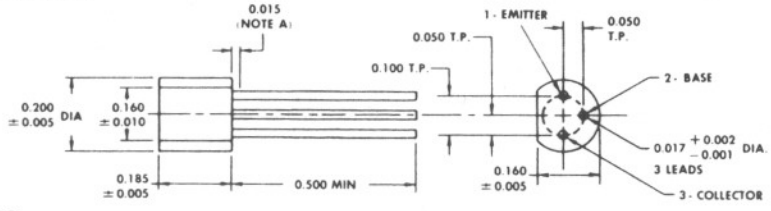


NOTES: A. Lead diameter is not controlled in this area.
B. All dimensions are in inches.

*ALL JEDEC TO-92 DIMENSIONS AND NOTES ARE APPLICABLE

EBC

A5T3905, A5T3906



NOTES:
A. Lead diameter is not controlled in this area.
B. Leads having maximum diameter (0.019) shall be within 0.007 of their true positions measured in the gaging plane 0.054 below the seating plane of the device relative to a maximum-diameter package.
C. All dimensions are in inches.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-Base Voltage	−40 V*
Collector-Emitter Voltage (See Note 1)	−40 V*
Emitter-Base Voltage	−5 V*
Continuous Collector Current	−200 mA*
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	625 mW§ 310 mW*
Storage Temperature Range	−65°C to 150°C§ −55°C to 135°C*
Lead Temperature 1/16 Inch from Case for 60 Seconds	260°C§ 230°C*

NOTES: 1. This value applies between 10 μA and 200 mA collector current when the base-emitter diode is open-circuited.
2. Derate the 625-mW rating linearly to 150°C free-air temperature at the rate of 5 mW/°C. Derate the 310-mW (JEDEC registered) rating linearly to 135°C free-air temperature at the rate of 2.81 mW/°C.

*The asterisk identifies JEDEC registered data for the 2N3905 and 2N3906 only. This data sheet contains all applicable registered data in effect at the time of publication.

†Trademark of Texas Instruments

‡U.S. Patent No. 3,439,238

§Texas Instruments guarantees these values in addition to the JEDEC registered values which are also shown.

USES CHIP P15

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*electrical characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		2N3905 A5T3905 MIN	2N3905 A5T3905 MAX	2N3906 A5T3906 MIN	2N3906 A5T3906 MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = -10\ \mu A$, $I_E = 0$		−40		−40		V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = -1$ mA, $I_B = 0$,	See Note 3	−40		−40		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = -10\ \mu A$, $I_C = 0$		−5		−5		V
I_{CEV}	Collector Cutoff Current	$V_{CE} = -30$ V, $V_{BE} = 3$ V			−50		−50	nA
I_{BEV}	Base Cutoff Current	$V_{CE} = -30$ V, $V_{BE} = 3$ V			50		50	nA
h_{FE}	Static Forward Current Transfer Ratio	$V_{CE} = -1$ V, $I_C = -100\ \mu A$		30		60		
		$V_{CE} = -1$ V, $I_C = -1$ mA		40		80		
		$V_{CE} = -1$ V, $I_C = -10$ mA		50	150	100	300	
		$V_{CE} = -1$ V, $I_C = -50$ mA	See Note 3	30		60		
		$V_{CE} = -1$ V, $I_C = -100$ mA		15		30		
V_{BE}	Base-Emitter Voltage	$I_B = -1$ mA, $I_C = -10$ mA	See Note 3	−0.65	−0.85	−0.65	−0.85	V
		$I_B = -5$ mA, $I_C = -50$ mA			−0.95		−0.95	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_B = -1$ mA, $I_C = -10$ mA	See Note 3		−0.25		−0.25	V
		$I_B = -5$ mA, $I_C = -50$ mA			−0.4		−0.4	
h_{ie}	Small-Signal Common-Emitter Input Impedance	$V_{CE} = -10$ V, $I_C = -1$ mA, f = 1 kHz		0.5	8	2	12	kΩ
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio			50	200	100	400	
h_{re}	Small-Signal Common-Emitter Reverse Voltage Transfer Ratio			0.1 X 10^{-4}	5 X 10^{-4}	0.1 X 10^{-4}	10 X 10^{-4}	
h_{oe}	Small-Signal Common-Emitter Output Admittance			1	40	3	60	μmho
$\|h_{fe}\|$	Small-Signal Common-Emitter Forward Current Transfer Ratio	$V_{CE} = -20$ V, $I_C = -10$ mA, f = 100 MHz		2		2.5		
f_T	Transition Frequency	$V_{CE} = -20$ V, $I_C = -10$ mA,	See Note 4	200		250		MHz
C_{obo}	Common-Base Open-Circuit Output Capacitance	$V_{CB} = -5$ V, $I_E = 0$, f = 100 kHz to 1 MHz			4.5		4.5	pF
C_{ibo}	Common-Base Open-Circuit Input Capacitance	$V_{EB} = -0.5$ V, $I_C = 0$, f = 100 kHz to 1 MHz			10		10	pF

NOTES: 3. These parameters must be measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle ≤ 2%.
4. To obtain f_T, the $|h_{fe}|$ response is extrapolated at the rate of −6 dB per octave from f = 100 MHz to the frequency at which $|h_{fe}| = 1$.

*operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	2N3905 A5T3905 MIN	2N3905 A5T3905 MAX	2N3906 A5T3906 MIN	2N3906 A5T3906 MAX	UNIT
$\overline{NF}$	Average Noise Figure	$V_{CE} = -5$ V, $I_C = -100\ \mu A$, $R_G = 1$ kΩ, Noise Bandwidth = 15.7 kHz, See Note 5		5		4	dB

NOTE 5: Average Noise Figure is measured in an amplifier with response down 3 dB at 10 Hz and 10 kHz and a high-frequency rolloff of 6 dB/octave.

*The asterisk identifies JEDEC registered data for the 2N3905 and 2N3906 only.

Standard Component Values

STANDARD 1/4 WATT RESISTANCE VALUES 5%

OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS	OHMS
2.2	9.1	→39	160	→680	3000	→12K	→51K	→220K	910K	→3.9M
2.4	→10	43	→180	750	→3300	13K	→56K	240K	→1.0M	4.3M
2.7	11	→47	→200	→820	3600	→15K	62K	→270K	1.1M	→4.7M
3.0	→12	51	→220	→910	→3900	16K	→68K	300K	→1.2M	5.1M
→3.3	→13	→56	240	→1000	4300	→18K	75K	→330K	1.3M	→5.6M
3.6	→15	→62	→270	→1100	→4700	→20K	→82K	360K	→1.5M	→6.2M
3.9	16	→68	→300	→1200	→5100	→22K	→91K	→390K	1.6M	6.8M
4.3	→18	75	→330	→1300	→5600	→24K	→100K	→430K	→1.8M	→7.5M
4.7	20	→82	360	→1500	6200	→27K	110K	→470K	→2.0M	→8.2M
5.1	→22	91	→390	1600	→6800	30K	→120K	510K	→2.2M	9.1M
→5.6	24	→100	430	→1800	7500	→33K	→130K	→560K	2.4M	→10M
6.2	27	110	→470	→2000	→8200	→36K	→150K	→620K	→2.7M	
6.8	30	→120	→510	→2200	9100	→39K	160K	→680K	3.0M	
7.5	→33	130	→560	2400	→10K	43K	→180K	→750K	→3.3M	
8.2	36	→150	620	→2700	11K	→47K	200K	→820K	3.6M	

Standard Capacitor Values

pF	pF	µF	µF	µF	µF	µF	µF
10	→100	→.001	→.01	→.10	→1	→10	→100
12	→120	.0012	.012	.12			
15	150	.0015	.015	.15	1.5	15	
18	180	.0018	.018	.18	→2.0		
20	→200	→.002	→.02	.2			
→22	→220	.0022	.022	→.22	2.2	→22	220
→25	→250	.0025	.025	.25			
27	→270	.0027	.027	→.27			
→33	→300	→.0033	→.030	→.33	→3.3	→33	
→39	→390	.0039	.039	.39			
→47	→470	→.0047	→.047	→.47	→4.7	→47	470
50	500	.005	→.05	.5			
56	560	.0056	.056	.56			
→68	680	→.0068	→.068	.68	6.8		
75	750	.0075	.075	.75			
→82	820	.0082	.082	.82			

1 % RESISTORS

→ points to parts in stock.

43.2 Ω	2.15 kΩ	232kΩ
69.8 Ω	26.7 kΩ	267kΩ
93.1 Ω	29.2 kΩ	332 kΩ
806 Ω	30.9 kΩ	340 kΩ