University of California, Davis
College of Engineering
Department of Electrical and Computer Engineering

Experiment No. 8
COMPENSATION IN FEEDBACK AMPLIFIERS

I.   OBJECTIVE

To demonstrate the conditions for oscillation in a feedback amplifier and the use of compensation to prevent oscillation for a given feedback configuration.

REQUIRED EQUIPMENT

One 3086 transistor array and three 2N2222 transistors
Oscilloscope, Sine wave generator
Assorted resistors and capacitors
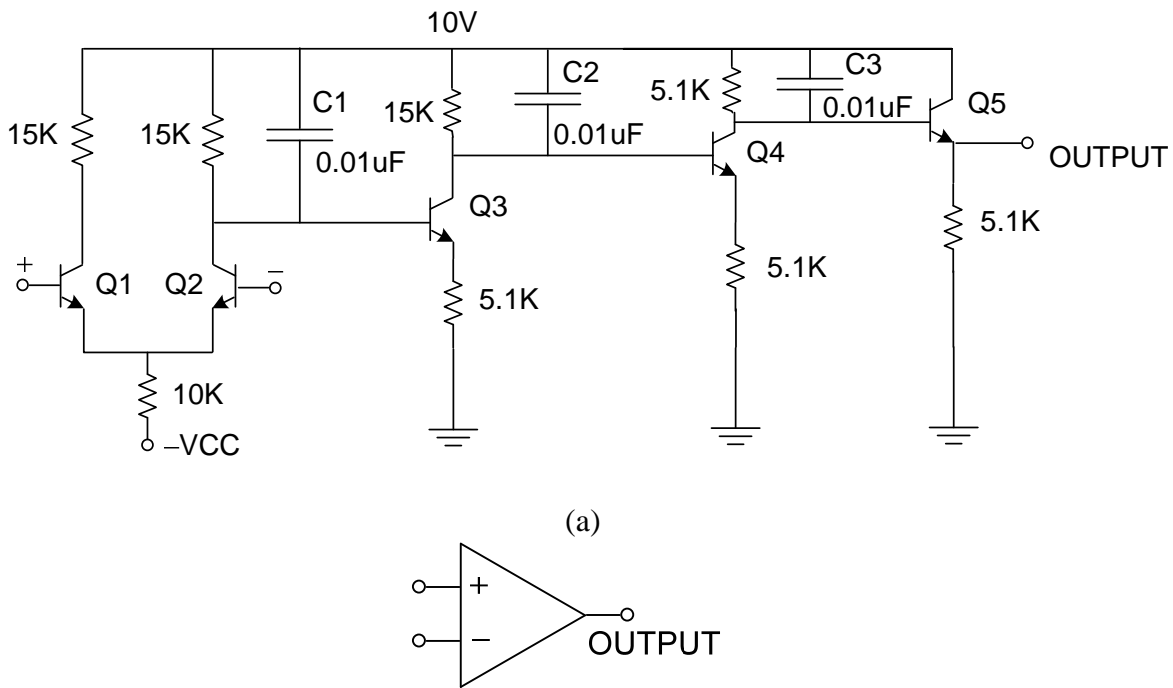

(a)

(b)

Figure 1. (a) Open-loop amplifier schematic. (b) Symbol for the circuit in (a).
For Q1-Q2, use a 3086 transistor array. For Q3-Q5, use 2N2222 transistors.

II. DISCUSSION/BACKGROUND

Three low frequency poles are intentionally designed into the circuit shown in Figure 1. The three poles, p1-p3, are associated with the three capacitors C1-C3. (For this experiment, the internal capacitances associated with the transistors can be ignored – i.e. they are open circuits – since they introduce additional high frequency poles that are at much higher frequencies than poles p1-p3.) As a result of the choice of p1-p3, the circuit, when connected in feedback, is not unity-gain stable. Therefore, it will oscillate if it is connected in a feedback configuration with too much feedback. Also, in order to make the open-loop gain characteristic easy to measure, the gain of the circuit is intentionally designed to be less than 1000. The circuit consists of four stages: a differential-pair input stage, two common-emitter-with-degeneration intermediate stages, and an emitter follower output stage. The input stage amplifies the differential input signal, provides most of the circuit's voltage gain, and produces one of the three low-frequency poles. The two intermediate gain stages provide very little gain; however, they each establish one of the three low-frequency poles. The output stage is a voltage buffer stage with a low output resistance.

III. PRELAB

Reading: Material on feedback and compensation in your text book (GHLM Chapters 8 and 9).

Prelab Calculations

(1) Assume the base of Q1 is connected to ground via a 1k Ohm resistor, and the base of Q2 is connected to ground via a 1k Ohm resistor. Assume that –VCC is adjusted so that the voltage at the collector of Q2 (VC2) is 2.6 Volts DC. Assume that $\beta \gg 1$ for all transistors. Calculate the DC voltage for all circuit nodes in Figure 1.

(2) Calculate the low-frequency voltage gain from the positive input to the output, when the negative input is grounded.

(3) Note that C1, C2, and C3 each produce a low frequency pole. Note also that these three poles are independent of each other. Estimate the values of the three low-frequency poles.

(4)   Calculate and plot magnitude of gain (in dB) vs. frequency from 50 Hz to 30 kHz on a log-log scale.

(5)   Calculate and plot phase of gain (in degrees) vs. frequency for the same frequencies on a linear-log scale (phase on a linear (y) scale, frequency on a log (x) scale).

(6)   From the plots of parts 4 and 5 above, determine the gain and phase margin if this amplifier is used in a feedback circuit with feedback factor of 1 (i.e., in a unity-gain feedback configuration: Rx = 0 in Fig. 2). Is the unity-gain feedback circuit stable? If the circuit is connected as shown in Figure 2, for what values of Rx will it oscillate and for what values of Rx will it be stable?

(7)   Calculate the value of C1 necessary to compensate the circuit in Fig. 2 so that it will have a phase margin of about 45° when the closed-loop gain is Vout/Vin = 10.
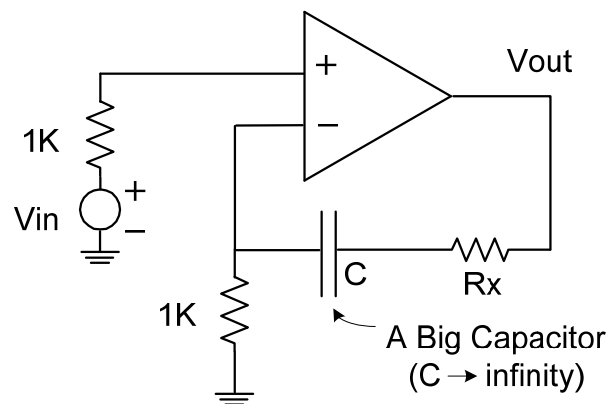

Figure 2. Transistor amplifier in feedback.

IV. PROCEDURE

(1)   Build the circuit in Figure 1 neatly (see NOTE below). Widely separate the first three gain stages to avoid interstage capacitive coupling, which could cause undesired feedback. Also connect a 1k Ohm resistor from the base of Q1 to ground and from the base of Q2 to ground. It is suggested that you build the circuit one stage at a time and verify the DC operating point as you go. Adjust –VCC so that VC2 is approximately 2.6 Volts DC. (Then –VCC will be approximately –10 volts.)

NOTE: The 3086 IC has a substrate pin (pin 13) that is shared with one of the transistors on the array. IT IS IMPORTANT THAT PIN 13 BE CONNECTED TO

THE MOST NEGATIVE SUPPLY (–VCC) to assure proper operation of the transistors. Make this connection, which is not shown in Figure 1, and do not use the transistor that has its emitter connected to pin 13.

(2) Measure the DC operating voltage of all nodes in the circuit. All the transistors should be in the forward active region of operation - check this.

(3) Connect the circuit as shown in Figure 3. At 50 Hz, set the magnitude of the output of the sine wave generator so that the amplifier output is not distorted. Use the oscilloscope to measure the magnitude of the open loop gain vs. frequency from 50 Hz to 10 kHz. Also, use the oscilloscope to measure the phase of the gain vs. frequency from 50 Hz to 10 kHz. The phase can be measured by displaying the input and output signals on the oscilloscope and measuring the time delay τ from the input peak to the output peak, and then converting that information to a phase shift θ using the formula: $\theta = -360^o(\tau \cdot f_{in})$. Tabulate the data. From the data, determine the gain and phase margins if this amplifier is used in a feedback circuit with feedback factor of 1. (When making these measurements, it may be helpful to increase the amplitude of the input as frequency increases.)
NOTES: a) A bigger capacitor (> 15µF) can be used if desired. b) A non-polarized capacitor can be built by connecting two polarized capacitors in series with the negative terminals connected together. c) It may be necessary to put a resistor (say 20k Ohms) in series with the signal generator, to produce a sufficiently small signal at the + input of the amplifier to avoid output clipping.
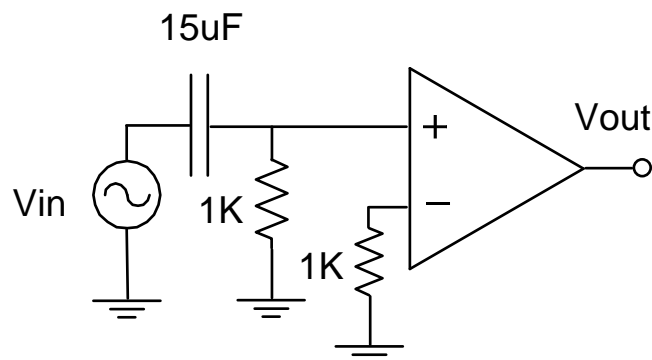

Figure 3.

(4) Plot the data from the last step on the same graphs that you made in the prelab.

(5)   Connect the circuit as shown in Figure 4. Use a 100k Ohm variable resistance box for Rx. What values of Rx cause oscillation, and what are the corresponding closed-loop gains? (Assume Vin would be connected as shown in Fig. 3.)   What is the frequency of oscillation? Relate this data to the measured and calculated open-loop gain and phase characteristics.
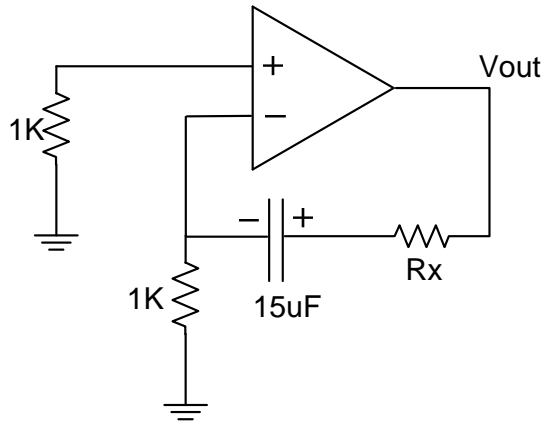

Figure 4.

(6)   Compensate the circuit for a closed-loop gain of 10 by replacing C1 with a capacitor whose capacitance is greater than or equal to the value that you calculated in the last part of the prelab calculations. Use this value for C1 in Steps 7 - 9.

(7)   Again, use a variable resistance box for Rx. For what values of Rx and what closed-loop gains is the circuit now stable?

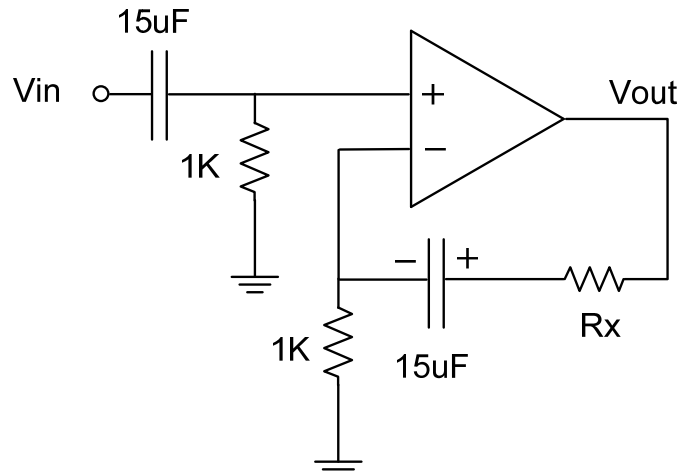Figure 5.

(8)   Connect the circuit as shown in Figure 5. Measure the magnitude of the open-loop gain vs. frequency as in Step 3 with Rx an open circuit. With Rx open, there is no

feedback. Plot this open-loop gain data. Now, set Rx for a closed-loop gain of 10 and measure the closed-loop gain vs. frequency. Sketch this closed-loop gain on the same plot as the open-loop gain data just taken.

(9) Try changing Rx, and measure the frequency response near the frequency at which the gain falls by 3 dB from its mid-band value. (Look at four values, two values of Rx larger than the value of Rx in (8), and two values smaller.). Note that decreasing Rx increases the feedback which in turn increases the bandwidth and decreases the gain. Also note that for values of Rx producing a low phase margin, peaking in the closed loop gain characteristic occurs near the 3 dB bandwidth. For Rx sufficiently small, oscillation may occur.
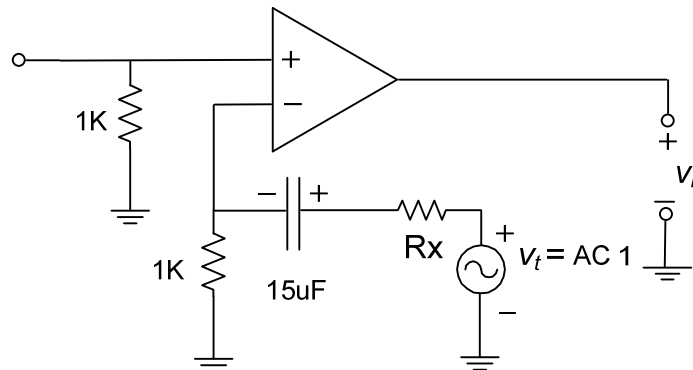

Figure 6.

(10) Use SPICE to simulate the phase margin of the feedback amplifier. One way to do this is to set all independent sources to zero, break the feedback at a point where loading can be ignored, inject a unit-amplitude AC test signal into the loop and measure the return signal. This is illustrated in Figure 6, where the break point is at the output of the emitter follower. This is a good break point because the output impedance of the emitter follower is low.[1] Such a simulation directly measures loop transmission T as $T = -v_r / v_t$.

Simulate the AC loop gain and phase vs. frequency for Fig. 1 (uncompensated: $C_1 = 0.01$ μF) for the value of Rx that initiated oscillation in Step 5. Compare SPICE and measured results. Report the phase margin, both simulated and measured.

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[1] Also, this is a good break point because no DC current flows through this break point. In general, DC sources must be added on both sides of the break to maintain the closed-loop DC operating point for the small-signal simulation.

For SPICE, use the models posted on the class web page.

(11) Simulate the loop gain magnitude and phase vs. frequency for Fig. 1 (compensated) using the value of Rx that sets the closed-loop gain to 10 (see Step 8). Compare SPICE and measured results. Report the simulated phase margin.

For this same value of Rx, use SPICE to find the midband output resistance with feedback. Also, calculate by hand the open-loop and closed-loop mid-band output resistance for the circuit that you simulated in Step 11. Compare your hand calculations using formulas from the text book with the SPICE simulation results.

2N2222 PIN DIAGRAM
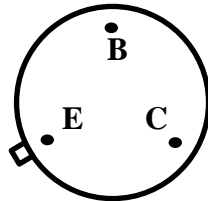
2N2222 transistor pin diagram (bottom view)

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LAB CHECKLIST

LAB. #8

ITEM	TA REMARKS
Part 3	
Part 5	

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