A Power Delivery Network and Cell Placement Aware IR-drop Mitigation Technique: Harvesting Unused Timing Slacks to Schedule Useful Skews

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Abstract— **This paper, presents a novel technique for reducing the intensity of IR hot-spots by leveraging the unused timing slacks to schedule useful skews. The peak current minimization problem is reformulated into a collection of smaller problems of reducing the peak current of each via-stack in the on-chip Power Delivery Network (PDN). In addition to timing information, it considers the PDN and cell placement information while scheduling the clock arrival times. Hence, while reducing the peak current, it effectively reduces the intensity the IR hot-spots. Application of the proposed solution to a selected number of IWLS benchmarks reduces the peak IR-drop by ~35%, and peak current by ~37%.**

Keywords-IR drop, peak current minimization, Power Delivery Network, signal and power integrity.

I. INTRODUCTION

A synchronous pipelined circuit relies on the distribution of the clock for timing management. At each triggering edge of the clock, each register captures the incoming signal, and propagates it to the next stage of combinational logic. Each triggering edge of the clock gives rise to a surge of switching activity, however the switching activity is quickly suppressed as the signals propagate down the timing paths [1]. Therefore, the peak current demand lines up with the triggering edge of the clock. The situation is further aggravated when synchronous circuits are optimized for zero clock skew [2] as all registers would switch at the same time, aggregating the extent of on-die IR drop.

IR drop has a resistive and an inductive element. The resistive element of IR drop denoted by IR could be reduced by lowering the resistance of Power Delivery Network (PDN) or reducing the current demand. The inductive form of IR drop, denoted by *Ldi/dt* could be reduced by reducing the inductance of board and package, or by reducing the rate of change in the demanded current. Following these guidelines, several techniques for reducing the peak current demand have been proposed. Work in [3] reduces the current demand for clock distribution network by operating half of the clock buffers in each of the rising and falling edge of the clock. The work in [4] reduces the peak current by either state replication or state re-encoding to minimize the peak switching value of the FSM. Work in [1] [2] [5] [6] [7] widens the distribution of the Clock Arrival Time (CAT) to reduce the simultaneous switching of cells and peak current. These methods, reduce the overall peak current, however they have limited ability to address the formation of local IR hot-spots. This is because the formation of regions with high IR-drop is due to the simultaneous switching of small collection of cells that are spatially placed close to one another and share the most resistive parts of the PDN, such as M1 rails and lower metal layer vias. Therefore, although previous peak current reduction techniques widen the distribution of CATs, for being ignorant to cell placement with respect to the PDN, they cannot prevent a concentrated cluster of registers to have similar CATs, and therefore have limited preventive power against the formation of IR-hot spots.

Our proposed technique reformulates the peak current reduction into many smaller problems of reducing the peak current of each via-stack that is connected to Metal-1 rails in IR hot spots. This reformulation allows the optimization of the peak current by considering both temporal and spatial arrival time of the clocks, and proves to be very effective in removing IR hot-spots. During the physical design, this technique is applicable at any stage after the Clock Tree Synthesis (CTS). The rest of this paper is organized as follows: Section II, builds the necessary background, Section III explains the proposed methodology, section IV provides the experimental and simulation results, and section V concludes the paper.

II. BACKGROUD

To safely signoff a chip for fabrication and to avoid timing failures in the fabricated chip, different sources of on chip variability should be carefully modeled and margined. One of the sources of on-chip variability is dynamic IR drop and its implied cycle to cycle voltage variation. The excessive IR drop or large cycle to cycle voltage variation could cause various forms of timing failure. Considering that timing failure of a single timing path is enough to make a chip non-functional, the margins for IR drop and voltage noise, are calculated based on the worst-case scenarios. The impact of IR drop and voltage variation worsens at scaled voltages. With 5% voltage noise in a design that is operated at Super Threshold Voltage (STV), 10-20% performance variation is observed [8]. However, the situation becomes far worse when the circuit is operated at Near Threshold Voltage (NTV), where 5% of voltage noise causes more than ~200% performance variation [8]. To prevent such delay variation from causing timing failures, during physical design, appropriately large design margins for IR-drop and endpoint uncertainty (to account for jitter in the result of voltage variation) are adopted. However, the price will be paid in terms of Power, Performance and Area (PPA) penalties, which increase super-linearly at the scaled voltages to a point that for designs operating at NTV, margin requirements for IR-drop and voltage noise could even eliminate the feasibility of such solutions.

A. Improving PPA & peak current by building clock skews

In a pipelined design, the longest stage of the pipelined circuit dictates the overall clock period. Hence the conventional CTS flows that build a clock tree with minimized or zero clock skew will result in little or no timing slack in longer pipeline stages, while building larger unused

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slacks in shorter stages of the pipeline. A novel idea, to mitigate this problem and to improve the PPA was the introduction of time borrowing technique. In this technique, which is widely adopted by commercial EDAs [10] [11], the unused slack in a shorter pipeline stage is borrowed and is pushed to the subsequent or preceding longer pipeline stage by building useful skews [9]. The source and destination registers, for the transfer of timing slack, do not need to be successive stages; the timing slacks could be moved across multiple stages until delivered to the destination stage.

In addition to timing closure, the useful skew is also leveraged for reduction of peak current. Each triggering edge of clock initiates a surge of toggle activities on die. However, as signals propagate forward in the combinatorial logic, their toggle activity is quickly suppressed, and thus, their current demand is quickly reduced. Therefore, widening the distribution of CAT, as claimed in [1] [2] [7] [6], reduces the simultaneous switching activities, resulting in reduction in the peak current. Although these techniques reduce the overall peak current, they cannot effectively address the occurrence of IR hot-spots. This is because by widening the distribution of clock's arrival time, there is no guaranty that a subset of registers, that simultaneously switch, are not placed near one another.

B. *Background on Power Delivary Network*

Construction of a typical PDN in advanced geometry nodes where 9 or more metal layers exist, as illustrated in Fig. 1, starts with building Metal 1 (M1) rails to which the power and ground pins of standard cells are connected. M1 rails are altered between Power (P) and Ground (G), and are usually implemented by placing filler cells in the design, followed by pre-routing the PG pins and subsequent removal of the filler cells. This leaves the M1 rails which are separated by the height of standard cells behind. Considering the increase in the current and power density in the scaled geometries, the M1 rail alone may not be strong enough to meet IR drop and Electromigration (EM) requirements. Therefore, M2 rail could be optionally routed in parallel to M1 rails. A batch of higher-level metal straps (usually M7) wich are routed orthogonal to M1 rails is then drawn to distribute the current more evenly. These straps are connected to M1 rails at each of their cross-layer intersections by using a via-stack. Choosing the size of via-stack is a physical design tradeoff; larger via-stacks reduce the resistive IR drop, however consume more routing resource.

Upper PDN metal layers (M8 & M9) are progressively made wider and will be connected to lower level PDN to evenly distribute the current across the chip. PDN is then extended to the Re-Distribution Layer (RDL) to further distribute the current and to connect the PDN to bumps that interface the on chip and the package PDN. Package also plays a big role in dictating the IR drop as it is highly inductive. The power and ground routes in the package should be alternated to reduce inductive coupling and inductive (*Ldi/dt)* IR drop.

Considering the structure of a typical PDN, the simultaneous switching of cells, may lead to formation of local IR-hot spots when placement of the cells ties their power and ground pins to the most resistive section of PDN. In this case the demanded current for simultaneous cell switching integrates over the M1 rail and lower level via stacks. M1 rail and lower level via stacks are highly resistive, which lead to large instantaneous IR drop. In this work, to mitigate the intensity of IR hot-spots we consider the relative placement of cells and their connectivity to the PDN while scheduling the clock arrival times to address the peak current reduction and IR hot-spot mitigation at the same time.

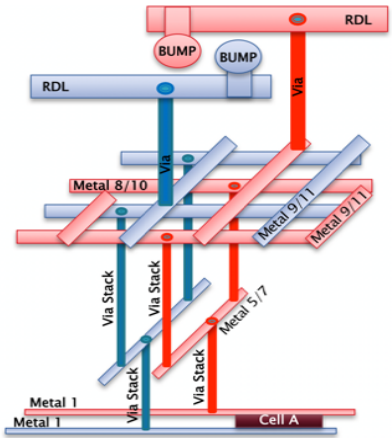

Figure 1. PDN Construction

C. *Impact of IR drop on Timing*

Delay of a cell depends on the voltage waveform or more specifically the differential voltage $V_{DD}(t) - V_{SS}(t)$ that is supplied to its power and ground pin while it is propagating a signal. This duration of time is formally defined as a cell's Timing Window (TW). In Static Timing Analysis (STA) a fixed voltage is applied to all cells. However in reality, each cell sees a unique voltage waveform; this voltage waveform is a function of the neighboring cell's switching activity and the PDN resistive, inductive (in package and board) and capacitive response to the demanded current. The correlation between the experienced voltages of two cells reduces, as cells are further placed apart, sharing a smaller portion of the PDN.

The structure of a timing path, as illustrated in Fig. 2, could be broken into Common, Launch, Capture, and Data path. It is possible to have most of the launch paths in an IR hot-spot where as the capture path lies mostly in a lower IR drop region, and vice versa. Therefore, it is possible that a substantial voltage difference between the cells in launch and capture sub-paths is developed.

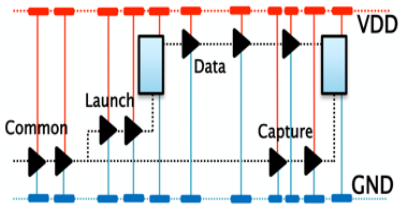

Figure 2. Structure of a timing path.

STA variables used to margin the impact of IR drop are the **operating voltage** and the endpoint's **uncertainty**: For a safe timing closure (1) the highest IR drop defines the voltage

supplied in the STA. Therefore, many cells that see smaller IR drop are penalized. (2) the largest cycle to cycle or launch to capture voltage variation defines the CTS jitter, therefore many timing paths experiencing less launch to capture voltage variation are penalized. Applying a lower operating voltage to the STA is not sufficient to model the impact of IR hot-spots, as the overall lower or higher voltage could be only seen at the launch or capture portion of the timing path. Therefore, it should be also margined as endpoint uncertainty to account for such operating condition jitter.

III. Proposed Methodology

To simultaneously reduce the peak current and the intensity of IR hot-spots, as illustrated in Fig. 3, we break the problem of overall peak current reduction into many smaller problems of via stack peak current minimization; The most resistive section of the PDN is the M1-rail and the via stack that connects the M1 to the wider upper layer (M7) metal straps. Considering that the M1-rails and lower level via-stacks are highly resistive, they are the most contributing elements to the formation of high-IR regions. Therefore, if the integral of the current, which is demanded through each lower level via stack could be lowered, the intensity of IR hot-spots could be greatly mitigated.

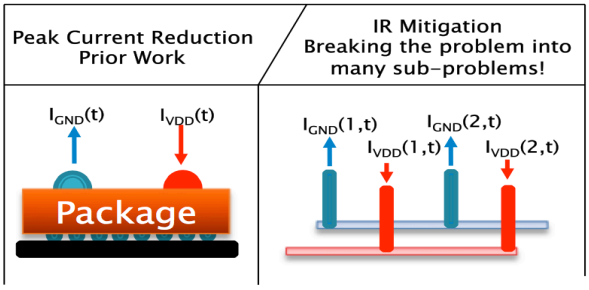

Figure 3. Breaking the overall peak current reduction problem into many smaller via-peak-current minimization problems.

Let us define the Minimum Resistance Path (MRP) as the least resistive path in the PDN from a cell to a bump or a pad. A PDN, which is constructed as explained in section II.B, has a regular mesh structure. Therefore, for a given standard cell, the via stacks closest to the power and ground pins of that cell are parts of its (Ground and Power) MRP. Most of the current delivered or returned to/from a cell, runs through its MRP. Table I. defines a few other terms that are used in our formulation.

Table *1*. Abbreviations and Definitions

Term	Definition
D	Distance between neighboring via stacks
H	Height of standard cells
V[i]	i-th via-stack in MRP region
MRR(via[i])	The region bounded by equations (1) and (2). The min resistive path for all cells in this region goes through via[i]
X(FF[i]), X(V[i])	Cartesian X location of FF[i] or V[i]
Y(FF[i]), Y(V[i])	Cartesian Y location of FF[i] or V[i]

Problem formulation: For each via V[i], and all flip-flops FF[j] that satisfy the two conditions below, schedule the clock arrival time such that the peak current demand through V[i] is minimized.

$$X[V[i]] - \frac{D}{2} < X[FF[j]] < X[V[i]] + \frac{D}{2} \quad (1)$$

$$Y[V[i]] - H < Y[FF[j]] < Y[V[i]] + H \quad (2)$$

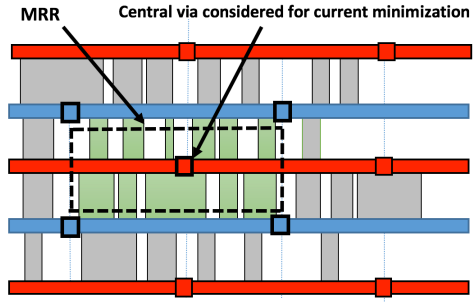

Figure 4. Minimum Resistive Region (MRR) of the central via

In other words, considering each via stack as a source or sink for the current, we are aiming to schedule the arrival time of the triggering edge of the clock to the clock pin of each FF in MRR such that the expected simultaneous switching of FFs and the expected current demand through via is minimized. Note that satisfying conditions (1) and (2), as illustrated in the example given in Fig. 4 ensures that FFs are in the MRR of the via-stack considered for peak current reduction.

The simultaneous switching of FFs in the same MRR has an additive effect on the demanded current and injected charge in the shared MRP. In addition, FFs have different strength and various output loads. Therefore, when scheduling the arrival time of FFs, their size and output load should be considered. To account for cell strength and output load variation, we built a simple yet effective model: The current that each FF draws during the switching will be will be directly proportional to its output load $\boldsymbol{C_L}$, and inversely proportional to its propagation delay $\boldsymbol{T_p}$. Let's define Expected Current Demand (ECD) of a FF as:

$$ECD = C_L/T_p \quad (3)$$

The capacitive load of the FF ($\boldsymbol{C_L}$) is obtained by adding FF's internal capacitance, output wire capacitance and fan-out gate capacitances, and the propagation delay through the FF ($\boldsymbol{T_p}$) is obtained from graph based timing analysis.

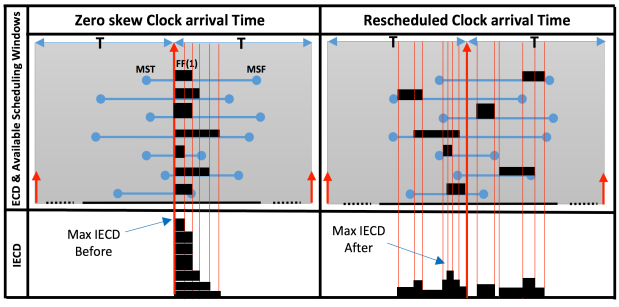

Figure 5. Deriving the IECD from ECD of all FFs in MRR.

To schedule the clock arrival times, first, the ECD of each FF in the MRR of interest is computed. This is illustrated in

Fig. 5 (left). Each black rectangle represents a FF. The height of the rectangle is the ECD of that FF, and the width of the rectangle is the propagation delay of that FF. The blue line, associated with each FF, shows the range in which that FF could be scheduled. This range is defined as the scheduling window of each register. Scheduling windows are computed by analyzing the available slack "**to**" and "**from**" each FF. Fig. 6. Illustrates an example on how the scheduling window of register FF is obtained. In this example, the minimum available timing slack from start-points S1, S2 and S3 to flip-flop FF is that of S2→FF with 1.0ns of slack. The smallest slack from FF, as a start point, is that of FF→ E1 with 0.5ns. Therefore, without causing timing violation, the arrival time of the clock to the clock pin of FF could be skewed within this scheduling window, spanning a scheduling window of width 1.5ns. Note that scheduling window could be easily extended by considering multiple pipeline stages. For example, if there exists available slack for all timing paths starting from E1, the arrival time of clock to E1 could be skewed and pushed out by 0.5ns, making it possible for FF to be skewed late by 1ns, instead of 0.5ns.

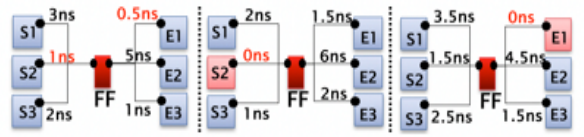

Figure 6. Timing slack transfer using CAT scheduling

To roughly obtain the demanded current signature over time, the ECDs of all FFs are integrated over two consecutive clock cycles. The Integrated ECD (IECD) curve is divided into many ECD-Slices (ECDS). The boundary of each slice is defined by the start and end-point of the timing windows of individual FFs. As illustrated in Fig. 5. (left), the maximum IECD, for a zero-skewed clock tree, happens in the first ECDS slice. Our proposed IR-mitigation technique skews the clock arrival time of FFs in a MRR region, within their available scheduling window, to minimize or considerably reduce the peak value of IECD in any ECDS slice.

Explanation of the Algorithm:

The pseudocode in Fig. 7 provides a detail description of the algorithm used to implement the proposed solution. The flow consists of 3 steps: (1) performing IR analysis, (2) identifying IR-hot spots, and preparing a clock skew plan, (3) implementing the clock skew by running incremental CTS. The second step is the heart of our work. In this step, we first find the available scheduling window of each FF in the MRR using the function **Collect_Timing_Information**. Then the arrival time of each FF is scheduled to have the maximum time difference with the arrival time of zero-skewed clock by pushing it as early or as late as possible. This step alone, reduced both peak current, and IR-hot spot intensity, but doesn't eliminate the chances of FF simultaneous switching. In order to further reduce the intensity of IR-hot spots, multiple rounds of analysis and optimization is applied. In each round, the IECD of the newly scheduled clock distribution is computed, and the ECDS slices with maximum/largest expected demand current (due to simultaneous switching) are identified. The maximum expected current value of all ECDS slices in an IECD curve is computed using **max_IECD** function. The FFs contributing to the max_IECD, which are a small subset of the original FFs, are flagged. Then the arrival time of each flagged FF is swept, using small timing steps. At each step a new IECD (IECD_temp) is computed. If the IECD_temp has a lower max_IECD value, the new arrival time of the clock for that FF is recorded, and the IECD_temp replaces the existing IECD. When all FFs contributing to the maximum current ECDS slice are re-scheduled, one optimization round is concluded. **NoR,** in this pseudocode, is the number of times that the above Peak ECDS current reduction flow would run. NoR should be experimentally obtained. Setting up the NoR to a small number, may lead to existence of some simultaneous switching in spatially close registers, when the situation could have been fully avoided. Setting the NoR to a very large number and resolving all or most timing-window overlaps, may lead to scheduling the clock arrival times closer and closer to the zero skew clock. This reduces the local resistive IR drop, however may increase the overall peak current, contributing to larger inductive IR drop.

```
Mitigate_IR_and_Peak_Current () {
| Run IR drop analysis
| If high intensity IR regions exist
| | Set tslice = small time slice (e.g. 5ps)
| | Set NoR = 5; // Number of optimization Rounds
| | For each IR-hot spot {
| | | For each via(i) {
| | | | Schedule_FFS (NoR, tslice, Via[i])
| | | }
| | }
| Run CTS to implement the scheduled clock arrival times
}

Schedule_FFS (int NoR, int tslice, struct via) {
| Collect_Timing_information(MRR[via[i])
| Schedule the arrival time of all FFs to be at
|       max distance from early edge of the arriving clock
|       by pushing them as early or as late as possible.
| Compute the IECD
| For (i=1; i<NoR; i++) { // rounds of optimization
| | For each FF[i] contributing to max ECDS,
| |              in the descending order of ECD per FF {
| | | For tt = tmst[i]; tt<tmsf[i]; tt+=tslice {
| | | | Set arrival time of FF[i] to be tt.
| | | | Compute the new IECD → IECD_temp
| | | | if max_IECD (IECD_temp) > max_IECD(IECD) {
| | | | | set new_SAT = tt;
| | | | | set IECD = IECD_temp;
| | | | }
| | | }
| | | if new_SAT != current arrival time {
| | | | Schedule the clock arrival time of FF[i] to be "new_SAT"
| | | | Annotate the FF with required book keeping information.
| | | }
| | }
| }
}

Collect_Timing_Information (MRR) {
| For each FF[i] in the MRR[via[i]] {
| | Set tmst[i] = The min slack for all paths ending at FF[i]
| | Set tmsf[i] = The min slack in all timing paths starting from FF[i]
| }
}
```

Figure 7. Proposed algorithm for peak current & IR-hot spot mitigation

We acknowledge that there is room for improving this algorithm. Rescheduling the clock arrival time of a FF will shift the timing window of all cells in its proceeding timing paths, which may result in formation of an IR hot-spot elsewhere. Although a valid concern, in practice this is not a big issue because the toggle rates drop very quickly within the first few cells of each timing path; therefore, although timing overlap may happen, considering the reduced probability of switching, the actual occurrence of simultaneous switching is far less probable. Furthermore, the algorithm could be executed multiple times to remedy the occurrence of new IR hot spots. In addition, this algorithm doesn't consider the switching activity of other cells (non-sequential cells) in the region. Although the switching activity depresses very quickly in the first few stages of combinatorial logic, considerations for expected current demand of the first few cells in each timing path, which experience higher switching activity, could improve our proposed clock arrival time scheduling algorithm and may lower the peak current and max IR drop. These issues are being addressed in our future work.

Impact on timing: Our proposed IR hot-spot mitigation technique reduces the intensity of IR hot spots and helps the circuit timing as follows (1) by removing the local hot spots, the mean voltage seen by standard cells is higher, and therefore they are faster. (2) By distributing the arrival time of the local clock, the high frequency voltage noise reduces; therefore, timing endpoint's uncertainty margin during the timing closure could be reduced. (3) The accumulative impact of distributing the arrival time of FFs, reduces the overall peak current (battery demanded current), and therefore the package RLC oscillation reduces, further reducing the cycle to cycle voltage noise, which could be modeled by reducing the uncertainty margin during the timing closure. The characterization of the timing impact of the proposed solution will be visited in our future work.

IV. Experimental Results

Our proposed peak current and IR hot-spot mitigation technique was tested on selected number of larger IWLS [13] benchmarks. Synopsys's Design Compiler Topographical (DC-Topo) [14] was used to synthesize each benchmark, and the Synopsys IC Compiler (ICC) [10] was utilized for floorplaning, PDN construction, cell placement, clock tree synthesis, and wire routing. The proposed flow is written in TCL, which is the native scripting language in ICC's shell. The runtime overhead of the scheduling algorithm is negligible (~1%) when compared to the run time of incremental CTS needed for implementation of scheduled clock arrival times. The overhead of incremental CTS, to implement the scheduled clock arrival times, varies between 5% to 40% of the run time of the original CTS. For the results reported in this section, all designs are subjected to a single round of analysis and mitigation, in which NoR is set to 5. Re-running the algorithm, or adaptively changing the NoR for each benchmark may result in better than reported results at the expense of larger analysis, optimization and/or implementation time.

The IR drop is calculated using Apache RedHawk [15]. For the purpose of this simulation, a lumped package inductance of 150pH and a lumped package resistance of 2.0mOhm is considered. For lack of space, the graphical implementation results of only one representative benchmarks (DES Cryptography engine) is illustrated, while the implementation results for other benchmarks is tabulated and offered in a table II.

A. IR drop improvement

Fig. 8 illustrates the effectiveness of our proposed algorithm in mitigating IR hot spots. In this figure the IR map of a DES Crypto Engine before and after the application of the proposed algorithm is illustrated. As demonstrated, the IR hot-spots are completely mitigated.

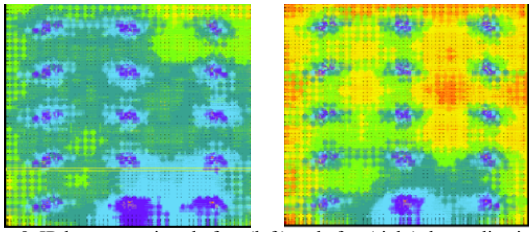

Figure 8. IR hotspot regions before (left) and after (right) the application of IR-mitigation technique.

Fig. 9 illustrates the distribution of IR-drops for all cells in the design. Application of the proposed algorithm reduces the intensity of IR drop and pulls in the tail of IR-drop distribution. In this benchmark, the worst IR-drop is improved by ~29%. For having a tighter distribution of voltages, the mean IR-drop of the entire design has also improved by ~9%.

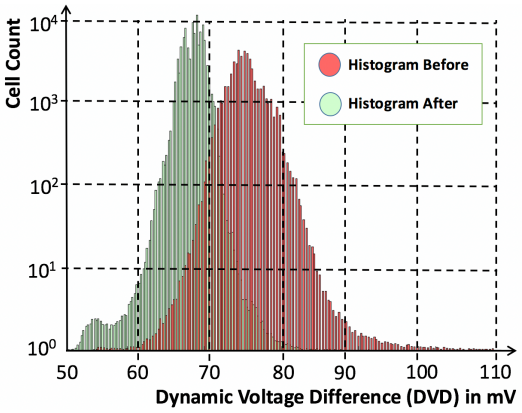

Figure 9. IR improvement after application of the proposed technique

Table II summarize the IR drop improvement obtained for the other implemented benchmarks. As demonstrated, after application of the proposed algorithm, the worst-case IR drop improves between 21%~35%, and mean IR drop improves between 7%~11%, depending on the benchmark. In addition, Table II captures the improvement in the IR drop, when it is averaged over the worst 10, worst 1000 and across all cells.

B. Peak current reduction

Although the primary objective of the propose algorithm is to reduce the intensity of IR hot-spots, still it is very effective in reducing the peak current as it widens the distribution of clock arrival times to reduce the via current

densities. Fig. 10 illustrates the impact of the proposed algorithm in reducing the peak current demand of the DES Cryptography Engine by 31%. The reduction in the peak currents of few other benchmarks are summarized in table II. The proposed technique achieves 16%~37% reduction in the peak current. Note that the proposed algorithm could be skewed to maximize the IR hot-spot mitigation or peak current minimization. However, the two are somewhat correlated.

In terms of peak current reduction, results obtained from this technique are comparable and in range of those reported in the previous work [1] [2] [5] [6] [7]. However, in the previous work there is no regard for IR hot-spot mitigation. Therefore, although it is possible for techniques proposed in the previous work to achieve comparable peak current reduction, they will not be able to minimize the local peak currents densities to mitigate local IR hot spots.

If maximum peak current reduction is desired, NoR should be set to a small number (possibly 1 or 2), and in an extreme case, the algorithm could be modified to touch a larger number of MRRs, or even every MRR in the design to minimize the peak current. However, visiting and optimizing all MRR regions, will create a heavy workload for the incremental CTS, may require very long runtime, and could result in substantial increase in the number of inserted buffers.

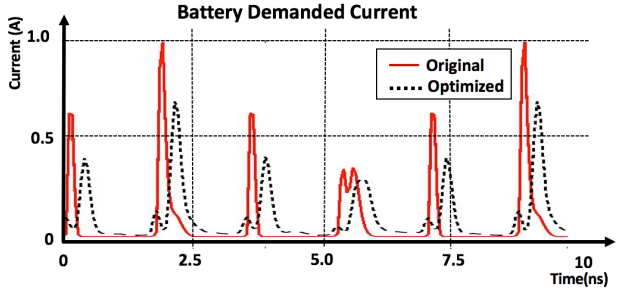

Figure 10. Reduction in the peak current demand

V. CONCLUSION

The peak current minimization problem is reformulated into many smaller problems of reducing the peak current of each via-stack that connects the M1 P/G rails in IR hot-spots to the upper layer PDN straps. By being placement and PDN aware, the clock arrival times are scheduled to reduce both temporal and spatial simultaneous switching. The proposed technique reduced the peak dynamic IR-drop by 21%~35%, and the peak current by 16~35% in the selected IWLS benchmarks.

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TABLE II. COMPARISION OF SEVERAL DESIGNS BEFORE AND AFTER APPLYING PROPOSED ALGORITHM

			Worst DVD			Percentage Reduction in			
Design	Cell Count	Reg Count	before (mv)	after (mv)	% reduction	top 10 cells	top 1K cells	all Cells	Iavg(A)
DES	45787	8808	116	82	29.31%	27.12%	16.18%	9.08%	31.12%
Ethernet Mac	33437	10545	89	58	34.83%	32.14%	19.41%	10.62%	26.11%
AES	105116	1595	82	65	20.73%	20.49%	12.09%	7.45%	16.34%
b19	12384	1485	81	57	29.63%	29.37%	21.37%	7.15%	37.04%