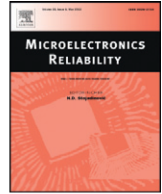
Microelectronics Reliability 62 (2016) 156–166

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr



# Reliability analysis of spin transfer torque based look up tables under process variations and NBTI aging

Ragh Kuttappa [a], Houman Homayoun [b], Hassan Salmani [c], Hamid Mahmoodi [a,*]

[a] School of Engineering, San Francisco State University, San Francisco, CA 94132, United States
[b] Department of Electrical and Computer Engineering, George Mason University, Fairfax, VA 22030, United States
[c] Department of Electrical and Computer Engineering, Howard University, Washington, DC 20059, United States

ARTICLE INFO

*Article history:*
Received 23 September 2015
Received in revised form 1 March 2016
Accepted 1 March 2016
Available online 2 May 2016

*Keywords:*
Look up table (LUT)
Magnetic tunnel junction (MTJ)
Process variations
Sense amplifier
Spin transfer torque (STT)

ABSTRACT

Spin transfer torque (STT) switching realized using a magnetic tunnel junction (MTJ) device has shown great potential for low power and non-volatile storage. A prime application of MTJs is in building non-volatile look up tables (LUT) used in reconfigurable logic. Such LUTs use a hybrid integration of CMOS transistors and MTJ devices. This paper discusses the reliability of STT based LUTs under transistor and MTJ variations in nano-scale. The sources of process variations include both the CMOS device related variations and the MTJ variations. A key part of the STT based LUTs is the sense amplifier needed for reading out the MTJ state. We compare the voltage and current based sensing schemes in terms of the power, performance, and reliability metrics. Based on our simulation results in a 16 nm bulk CMOS, for the same total device area, the voltage sensing scheme offers 17% to 28% lower failure rates under combined intra-die transistor and MTJ variations, comparable delay, and 56% lower active power compared to the current sensing scheme. Moreover, we compare the reliability of the two sensing schemes under negative bias temperature instability (NBTI) of PMOS transistors. Our results indicate that the failures rates increase over time by transistor aging for both designs, and the voltage sensing scheme maintains its improved failure rate over to the current sensing scheme.

© 2016 Elsevier Ltd. All rights reserved.

## 1. Introduction

Spin transfer torque (STT) refers to a switching mechanism resulting in change of magnetic state in a magnetic tunnel junction (MTJ) device [1]. The MTJ is composed of a fixed and free magnetic layer isolated by a thin insulator (Fig. 1) [2]. The parallel and anti-parallel magnetic state of the two layers, representing binary states, is sensed by the resulting low and high resistance across the two terminals of the MTJ [1,2]. The current passed through the MTJ for sensing its resistance (i.e. read current) has to be less than the current needed for changing its state (i.e. write or critical current) [1,2].

Due to its non-volatile nature and CMOS compatibility, STT-based memory (STT-RAM) has shown great promise in addressing the leakage barrier for SRAM. While the high write power still remains to be a major obstacle for STT-RAM [3], the application of STT-based memory in reconfigurable logic, as in field programmable gate arrays (FPGA) or reconfigurable functional units, seems more promising due to the low frequency of reconfiguration where the write power occurs [4,25,26]. Reconfigurable logic relies on implementing logic in small look-up-tables (LUT). STT-based LUTs are realized by using MTJs as storage elements and using CMOS for interface circuitry needed for read and write operations [4–7]. The CMOS interface includes a decoder/multiplexer for selecting a unique MTJ for read/write and a sense amplifier for sensing the resistance of the selected MTJ in the read mode [4–7].

Scaling of the CMOS technology to ever smaller dimensions has posed serious reliability challenge to designs. The main cause of the issue is increasing process variations (both spatial and temporal) affecting transistor characteristics, and especially the threshold voltage ($V_{th}$). Such variations include both inter- and intra-die variations. Some causes of variations such as random dopant fluctuations (RDF) exhibit uncorrelated variations from one device to another and hence fall into the intra-die category, whereas other sources such as oxide-thickness variations tend to exhibit correlations among adjacent devices and hence fall more into the inter-die variations. In addition to transistor variations, MTJs exhibit variations in their geometrical parameters such as insulator thickness and 2D area [8]. Such variations result in variations in resistance of an MTJ [9].

Negative bias temperature instability (NBTI) is another important reliability concern resulting in $V_{th}$ increase for PMOS transistors over life-time and hence impacting circuit power, performance, and reliability [12–17].

* Corresponding author at: School of Engineering, San Francisco State University, 1600 Holloway Avenue, San Francisco, CA 94132, United States.
*E-mail addresses:* ragh@mail.sfsu.edu (R. Kuttappa), hhomayou@gmu.edu (H. Homayoun), hassan.salmani@howard.edu (H. Salmani), mahmoodi@sfsu.edu (H. Mahmoodi).

http://dx.doi.org/10.1016/j.microrel.2016.03.003
0026-2714/© 2016 Elsevier Ltd. All rights reserved.

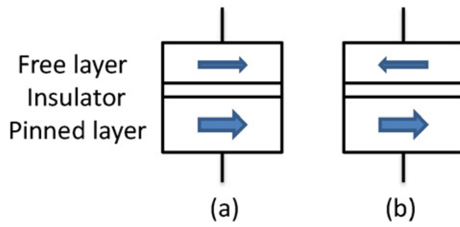



**Fig. 1.** Programmable MTJ: (a) Parallel (low resistance) and (b) anti-parallel (high resistance) states.

In this paper, we analyze the impact of CMOS/MTJ process variations and NBTI on the reliability of the STT-based LUTs. We present a comparative analysis of voltage vs. current mode sensing schemes in such LUTs. The contributions of this paper are as follows:

- Comparative reliability analysis of voltage vs. current mode sensing schemes in STT-based LUTs considering both CMOS and MTJ variations;
- Statistical transistor sizing of the designs for fair comparison under same area;
- Comparative reliability analysis of voltage vs. current mode sensing schemes in STT-based LUTs against NBTI aging.

The remainder of the paper is organized as follows. Section 2 introduces the voltage and current mode sensing schemes for STT-LUTs. Section 3 presents the modeling of process variations and statistical sizing of the designs. The results of the process variation analysis and comparisons are discussed in Section 4. Section 5 presents the NBTI modeling and analysis and comparison. Section 6 concludes the paper.

## 2. Sense amplifier schemes for STT-LUT

An n-input LUT contains $2^n$ storage elements that are accessed via a decoder/multiplexer. However, in STT-LUTs, since the storage elements are MTJs that exhibit high and low resistance states, there is also need for a sense amplifier stage to compare the resistance of the selected MTJ with a reference resistance to produce full voltage swing logic one or zero signal depending on the MTJ being in the high or low resistance state (Fig. 2) [4–7].

For high read performance and enhanced noise margin, greater difference between the low and high resistances of the MTJ is desired. This resistance differential is quantified by the tunnel magneto resistance (TMR), defined as:

$$TMR = \frac{R_{AP} - R_P}{R_P} \quad (1)$$

where $R_P$ and $R_{AP}$ are the resistances of the MTJ in the parallel and anti-parallel states, respectively. TMR is a technology parameter dependent on the MTJ geometries and materials.

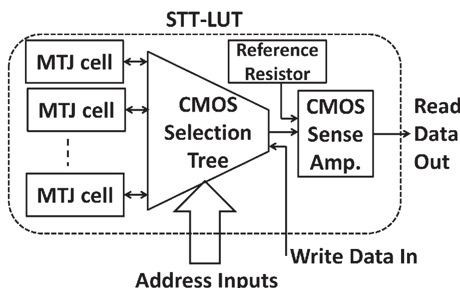



**Fig. 2.** STT-based LUT, a hybrid MTJ/CMOS design.

To translate the $R_P$ and $R_{AP}$ into a binary full swing voltage signal in the read mode, a sense amplifier is used to compare the resistance of the selected MTJ against a reference resistor (Fig. 2). The value of the reference resistor should be set to maximize the sensing margin of the sense amplifier for both MTJ states. In the read mode, the selected MTJ and the reference resistors are biased and their currents are passed to the sense amplifier stage. The sense amplifier can be designed to either directly amplify the current differential (i.e. current mode sensing) or a current-to-voltage conversion stage may precede a voltage mode sense amplifier. These two styles of sensing the MTJ resistance are discussed in further detail in the remainder of this section. Since the write paths remain identical, we will only discuss the read paths and compare the read performance of the two styles.

### *2.1. Voltage sensing mode STT-LUT*

Fig. 3 shows the schematic of a voltage sensing mode (VSM) 2-input (4-bit) STT-LUT [6]. This is a dynamic circuit that operates in a precharge ($CLK = 0$) and evaluate ($CLK = 1$) fashion. The MTJ selection is performed via a pass-transistor decoder/multiplexer (selection tree). To balance the transistor paths of the MTJs and the reference resistor ($R_{REF}$), similar transistors are inserted above the reference resistor. When CLK switches high, the current provided by the dynamic current source is divided between the selected MTJ and the reference resistor, resulting in a current differential that will be drained from the nodes DEC and REF. This current differential is converted to a low swing voltage differential on the nodes DEC and REF by the current-to-voltage converter circuit which is composed of the two cross coupled PMOSes. This voltage differential is then amplified by a voltage-mode sense amplifier to produce full swing differential outputs (Z and Z′).

Sensing margin is one of the metrics used to measure the reliability of reading the state of an MTJ cell [20,21]. The sensing margin for this scheme is defined as the minimum voltage differential between the inputs of the sense amplifier (nodes DEC and REF) in the evaluation phase (when CLK switches high), when sensing $R_{AP}$ and $R_P$:

$$SM = \min\left((V_{DEC} - V_{REF})|_{R_{AP}}, (V_{REF} - V_{DEC})|_{R_P}\right). \quad (2)$$

This quantity right at the beginning of the evaluation cycle is zero and increases as time passes. Since the sense amplifier does not start sensing until one of the voltages, $V_{DEC}$ or $V_{REF}$, falls below the PMOS threshold voltage, we measure the sensing margin at that time which is found by simulating the design under nominal process conditions.

### *2.2. Current sensing mode STT-LUT*

Fig. 4 shows the schematic of a current sensing mode (CSM) 2-input (4-bit) STT-LUT [7]. The design is similar to the VSM version except that the current differential is directly applied to a current mode sense amplifier, and hence the current-to-voltage convertor circuit is eliminated. This is also a dynamic design. When the clock is high, the sense amplifier is biased in a metastable state by shorting its outputs. The outputs approach a voltage of about $V_{dd}/2$ in this case and this voltage is also applied as bias to the MTJ and reference resistors. When the clock switches low, the cross-couple inverter in the sense amplifier will switch to one of the stable states and the direction of this switching will be determined by the current differential between the MTJ and the reference resistor. Since during the biasing of the sense amplifier in the meta-stable condition (i.e. when CLK is high), the outputs are shorted, there is considerable static short circuit power dissipated on the sense amplifier. In order to reduce this short circuit power, the CLK duty cycle (high duration) should be reduced. In this research CLK has a duty cycle of 50% to maintain uniformity in the analysis and comparisons.

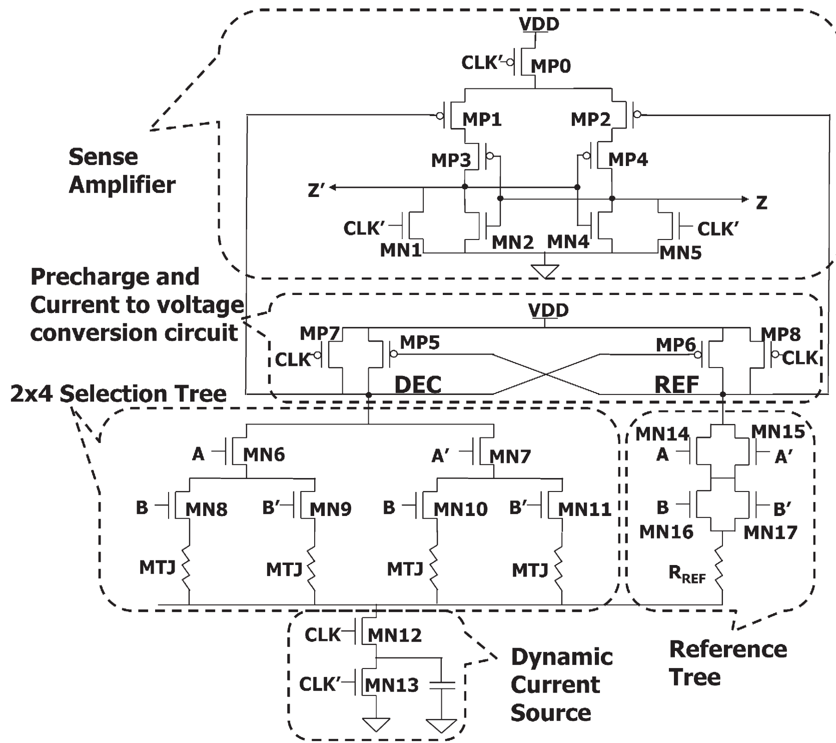



**Fig. 3.** Voltage sensing mode STT-LUT [6].

The sensing margin for this design is defined as the minimum current differential between the two legs of the sense amplifier ($I_{MTJ}$ and $I_{REF}$), when sensing $R_{AP}$ and $R_P$:

$$SM = \min\Big((I_{REF} - I_{MTJ})\big|_{R_{AP}}, (I_{MTJ} - I_{REF})\big|_{R_P}\Big). \quad (3)$$

Since the sensing starts as soon as the evaluation phase starts (CLK switches low), this quantity is measured right before or at the very beginning of the start of the evaluation phase.

## 3. Process variation modeling and analysis

### 3.1. CMOS variations

CMOS process variations have various causes that affect transistor performance. The effect of most causes of variations can be captured as $V_{th}$ variation. Some sources of variations such as RDF are random (uncorrelated) in nature, whereas some other such as oxide thickness variations are correlated. The variations can be divided into two groups of inter and intra-die variations [27]. The uncorrelated and random causes belong to the intra-die category and the correlated ones to the

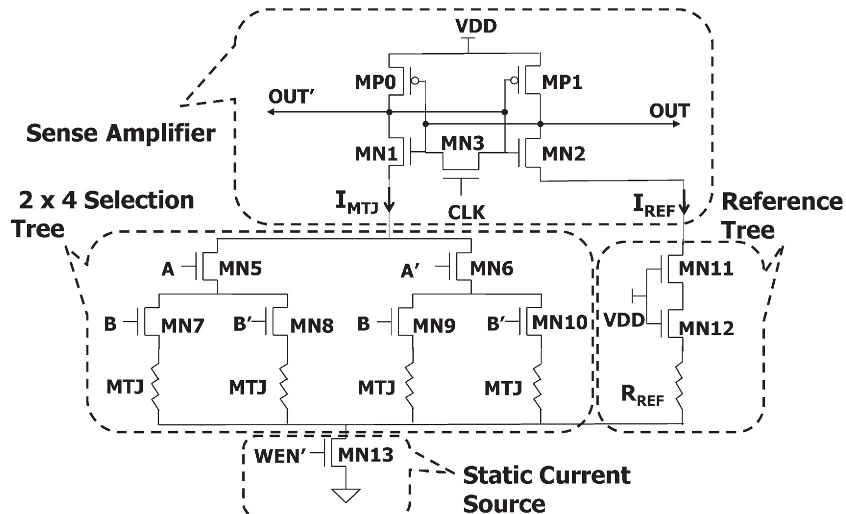



**Fig. 4.** Current sensing mode STT-LUT [7].

inter-die category. We model the $V_{th}$ variation of a transistor by adding a DC voltage source in series with the gate terminal with a parameterized voltage level that represents the total $V_{th}$ shift for a transistor. This modeling allows us to do both inter and intra-die $V_{th}$ variation analysis. The intra-die variation considered in this study is RDF due to its prominence in scaled bulk CMOS transistors. The $V_{th}$ shift by RDF is inversely related to the square root of the device area (W × L) as follows [28]:

$$\sigma_{Vt} = \left[\frac{qT_{ox}}{\varepsilon_{ox}}\sqrt{\frac{(N_a W_d)}{3L_{min}W_{min}}}\right] \times \sqrt{\frac{L_{min}W_{min}}{LW}} = \sigma_{Vt0} \times \sqrt{\frac{L_{min}W_{min}}{LW}} \quad (4)$$

where all the technology parameters are lumped into $\sigma_{vt0}$ which represents the standard deviation of $V_{th}$ variation of a minimum sized transistor with dimensions $L_{min}$ and $W_{min}$. L and W are channel length and width of the given transistor.

Sense amplifier circuits utilize differential pair transistors to do analog voltage or current comparison and hence are more sensitive to intra-die $V_{th}$ variations that cause mismatch among neighboring transistors such as those in a differential pair. Given that bigger transistors exhibit less intra-die $V_{th}$ variations (Eq. (4)), it is expected that by increasing transistor sizes (W) in the LUT designs, the delay variation and failure probability should be reduced. Hence, a fair comparison between the two LUT designs should be made under same total transistor (active) area. Moreover, for a given total area constraint, it is not optimal to uniformly allocate area to all transistors, given that the $V_{th}$ variation of some might have more influence than others on the overall failure probability. For example, it is expected that the variations of the transistors in the differential paths of the sense amplifier to be more influential than the precharge transistors. To address this problem more formally, we define the delay to $V_{th}$ sensitivity metric for a given transistor, $M_i$, in a circuit as:

$$\text{Sensitivity}_i = \frac{|T_{p0} - \text{Max}(T_{pi}, T_{p'i})|}{dVti} \quad (5)$$

where dVti is the $V_{th}$ variation applied to the transistor $M_i$, $T_{p0}$ is the nominal delay of the design, and $T_{pi}$ and $T_{p'i}$ represents the delay to the OUT and OUT′ of the LUT design after applying the $V_{th}$ variation to the given transistor, $M_i$.

Tables 1 and 2 summarize the sensitivity measurements in descending order for transistors of both LUT designs obtained by spice simulations

**Table 1**
$V_{th}$ sensitivity rankings for VSM STT-LUT.

| Ranking | Transistor name | Sensitivity (ps/mV) |
|---|---|---|
| 1 | MN1 | 5.94 |
| 1 | MN5 | 5.94 |
| 2 | MN8 | 5.18 |
| 2 | MN9 | 5.18 |
| 2 | MN10 | 5.18 |
| 2 | MN11 | 5.18 |
| 3 | MN14 | 5.16 |
| 3 | MN15 | 5.16 |
| 4 | MN6 | 5.01 |
| 4 | MN7 | 5.01 |
| 5 | MN16 | 3.49 |
| 5 | MN17 | 3.49 |
| 6 | MP5 | 1.63 |
| 6 | MP6 | 1.63 |
| 7 | MN2 | 1.47 |
| 7 | MN4 | 1.47 |
| 8 | MN13 | 0.23 |
| 9 | MP1 | 0.22 |
| 9 | MP2 | 0.22 |
| 10 | MP0 | 0.05 |
| 11 | MN12 | 0.004 |
| 12 | MP6 | 0.002 |
| 12 | MP7 | 0.002 |

**Table 2**
$V_{th}$ sensitivity rankings for CSM STT-LUT.

| Ranking | Transistor name | Sensitivity (ps/mV) |
|---|---|---|
| 1 | MN1 | 4.20 |
| 1 | MN2 | 4.20 |
| 2 | MN3 | 1.93 |
| 3 | MN5 | 1.11 |
| 3 | MN6 | 1.11 |
| 4 | MN11 | 0.94 |
| 5 | MN12 | 0.86 |
| 6 | MN13 | 0.11 |
| 7 | MN7 | 0.003 |
| 7 | MN8 | 0.003 |
| 7 | MN9 | 0.003 |
| 7 | MN10 | 0.003 |
| 8 | MP0 | 0.001 |
| 8 | MP1 | 0.001 |

in a predictive 16 nm bulk CMOS technology [10]. A transistor with higher sensitivity is given higher area (W) than another one with a lower sensitivity. The channel length of all transistors is kept at minimum. The width of the transistor $M_i$ ($W_i$) is found as follows:

$$W_i = \frac{\text{Sensitivity}_i}{\sum_{j=0}^{n}\text{Sensitivity}_j} \times W_{total} \quad (6)$$

where, $W_{total}$ represents the total width allocated for the circuit and n is total number of transistors in the circuit.

We compare the designs under same total area, and transistors are sized according to their sensitivity. This ensures that for a given total area, we have optimally sized transistors for best reliability. From the $V_{th}$ sensitivity results, it is observed that the sense amplifier transistors are the most sensitive ones and need to be given the highest portion of the area.

### *3.2. MTJ variations*

Besides transistors, MTJs also exhibit variations in their geometries, namely, the insulator thickness ($t_{ox}$) and the cross-section area (A) [8]. Such variations result in variations in critical write current as well as high and low state resistances during the read mode [9]. Since we are concerned about read failures for the LUTs, we model the MTJ variations as variations in high and low state resistances ($R_{AP}$ and $R_P$). Considering a 2D circular shape of radius r, the MTJ area A is expressed as $\pi r^2$. The relation between the resistance of the MTJ and $t_{ox}$ and r can be expressed as [18,29]:

$$R = K_1 \frac{t_{ox}}{r^2} e^{(K_2 t_{ox})} \quad (7)$$

where $K_1$ and $K_2$ represents all the remaining process parameters [29]. Notice that $t_{ox}$ and r are the major but not the only sources of variability in MTJs [20]. Here, to simplify the analysis we focus on these two primary sources. Assume $t_{ox}$ and r exhibit variations represented by dt and dr from their nominal values, respectively. Then, the MTJ resistance value R with respect to its nominal value $R_0$ can be expressed as:

$$R = R_0 \frac{\left(1 + \frac{dt}{t_{ox0}}\right)}{\left(1 + \frac{dr}{r_0}\right)^2} e^{(K_2 dt)} \quad (8)$$

where $t_{ox0}$ and $r_0$ are the nominal values of $t_{ox}$ and r, respectively. $K_2$ is 0.6483 based on [29]. Treating $dt/t_{ox0}$ and $dr/r_0$ as uncorrelated normal random variables with mean value of zero and standard deviation between 0 and 1, the statistical distributions of MTJ resistances can be obtained. Fig. 5 shows the distributions of $R_P$ and $R_{AP}$ and the reference resistor ($R_{REF}$) with 10% standard deviation applied to dt and dr (i.e. σ/

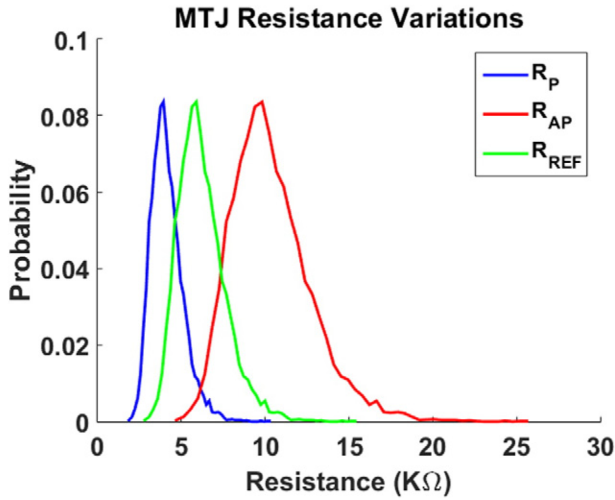



**Fig. 5.** Distributions of MTJ $R_P$ ($\mu = 4$ kΩ, $\sigma = 0.98$ kΩ), $R_{AP}$ ($\mu = 10$ kΩ, $\sigma = 2.46$ kΩ), and $R_{REF}$ ($\mu = 6$ kΩ, $\sigma = 1.47$ kΩ).

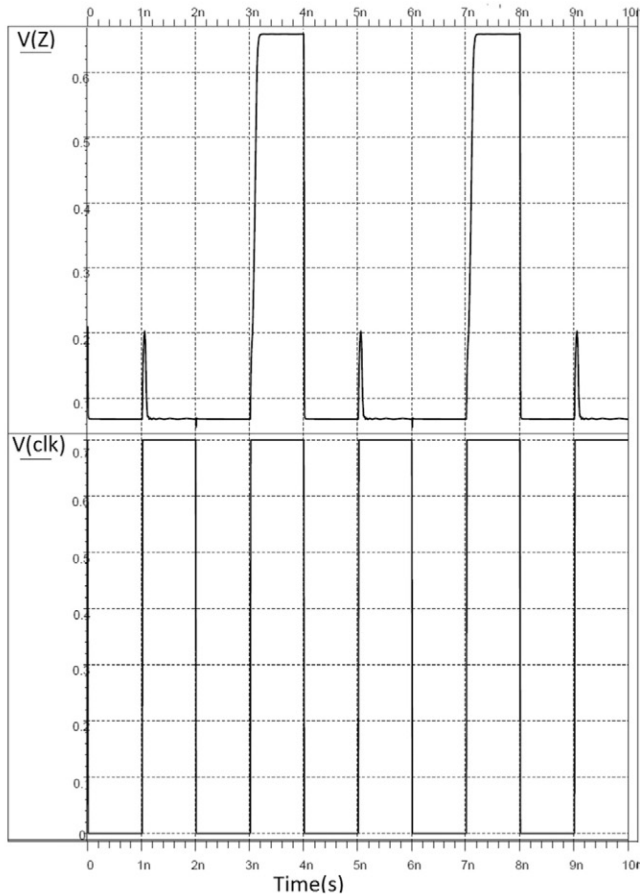
$\mu = 0.1$ for both $t_{ox}$ and r). The values of $R_{AP0}$ and $R_{P0}$ are chosen to be 10 kΩ and 4 kΩ (TMR = 150%) in the 16 nm node based on the MTJ scaling trends [11]. The nominal value of the reference resistor is chosen in each LUT such that symmetric delays to the differential outputs (Z (OUT) and Z′ (OUT′)) are obtained. The reference resistor can be constructed from series and parallel connection of MTJs [19]. Hence, we assume the reference resistor itself exhibits variations in a similar manner as the real MTJ. The read failure can occur when the $R_P$ is increased or $R_{AP}$ is decreased from their nominal values, or by variation of $R_{REF}$ in either direction.

According to Fig. 5, σ/μ ratio for resistance variation is 0.245. Since the variations in $t_{ox}$ and r affect both $R_P$ and $R_{AP}$ in the same manner as described in Eq. (8), the TMR is not affected by such variations and remains constant.

## 4. Results and discussions

The MTJs in both LUTs are programmed to have 50% of the MTJs in the $R_P$ and the rest in the $R_{AP}$ state. Simulations are performed to apply all inputs combinations and measure read delay, power, and failure rates. Fig. 6 shows typical simulation waveforms of the LUTs at the nominal process corner. Fig. 7 shows the output waveform plots obtained by Monte Carlo simulations of intra-die $V_{th}$ variation. These waveforms clearly show delay variations and failures caused by $V_{th}$ variations.

Fig. 8 shows the sensing margin distributions under intra-die MTJ variations for both STT-LUT schemes. Sensing margin falling below some minimum value (i.e. the sense amplifier offset) results in failure in the sense amplifier. The sense amplifier offset itself is subject to variations. That is why the region with negative sense margin in Fig. 8 is labeled as possible rather than definite failure region. Nonetheless, the CSM styles exhibits a wider distribution than the VSM styles, indicating that the CSM style is more sensitive to process variation and should exhibit more failures.



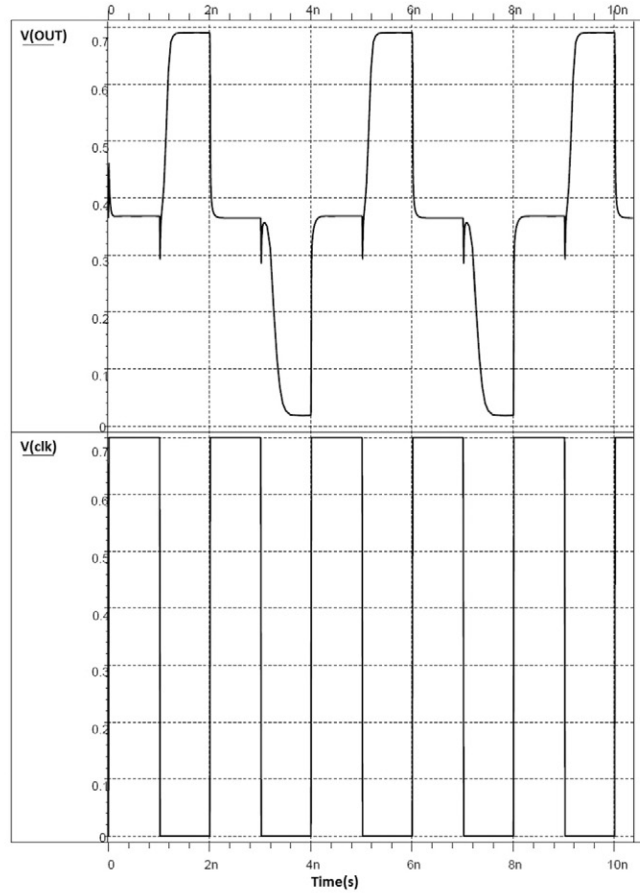




**Fig. 6.** Read waveforms showing clock and output signals for (a) VSM STT-LUT and (b) CSM STT-LUT.

**Fig. 7.** Read output waveforms from Monte Carlo $V_{th}$ variation simulation for (a) VSM STT-LUT and (b) CSM STT-LUT.

Fig. 9 shows the delay distributions obtained by Monte Carlo simulations of intra-die $V_{th}$ variations, where $\sigma_{Vt0}$ is set at 23 mV, which is 10% of the NMOS nominal threshold voltage for a minimum sized transistor and after the influence of short channel effects in the 16 nm process used. The plots are obtained for both STT-LUTs optimally designed according to the $V_{th}$ sensitivity method for the same total active (transistor) areas of 0.02856 μm$^2$ (1×) and 0.04284 μm$^2$ (50% larger or 1.5×). Any delay greater than 500 ps (half the total evaluation period) is considered as a failure and all the failure cases are lumped into a single bin at 1000 ps. It is observed that the VSM STT-LUT exhibits less failure rates despite having higher delay spread (σ/μ) for the success cases. The VSM exhibits 16% to 32% less failure rates compared to the CSM style. Moreover, comparing Fig. 9(a) and (b) shows that transistor upsizing is much more effective in reducing delay and failure rate in the VSM style as

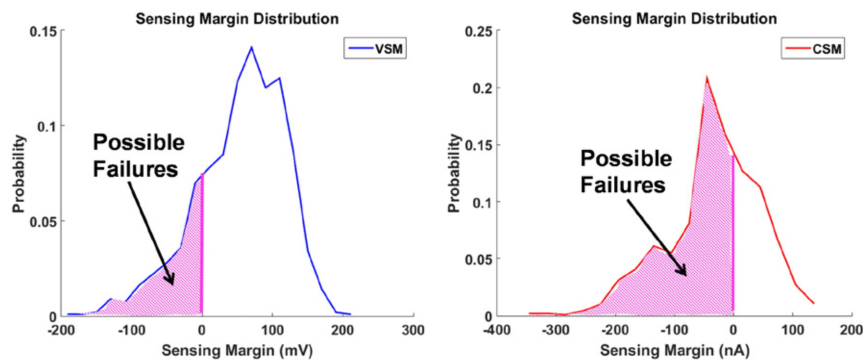
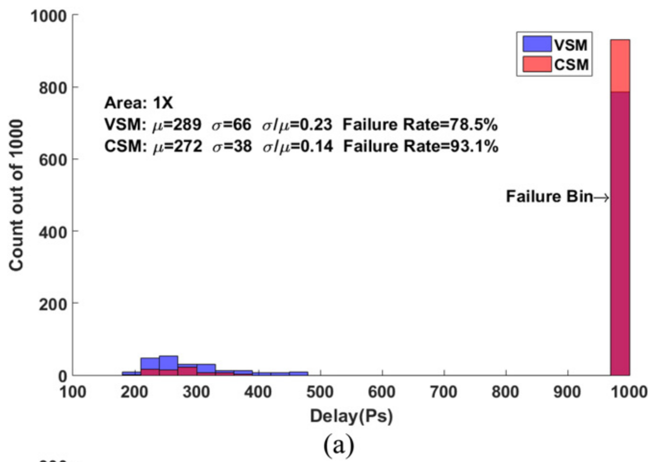



**Fig. 8.** Sensing margin distributions under intra-die MTJ $t_{ox}$ and r variations ($\sigma/\mu = 0.1$) for LUTs.



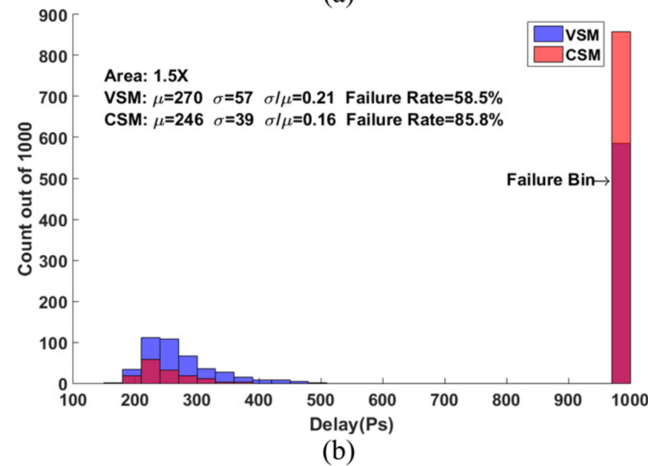
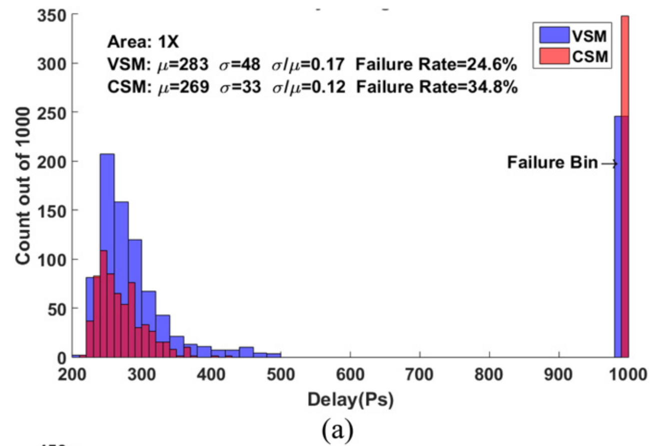




**Fig. 9.** Delay distributions under intra-die $V_{th}$ variation ($\sigma_{Vt0} = 23$ mV) for LUTs designed for same total active area of (a) 1× (b) 1.5×.



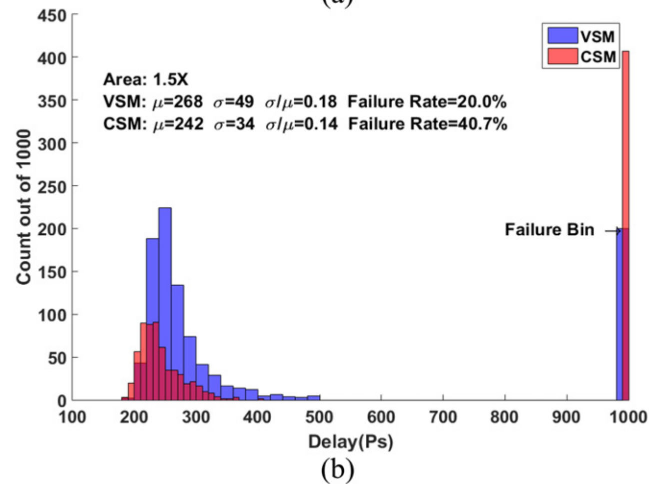




**Fig. 10.** Delay distributions under intra-die MTJ $t_{ox}$ and r variations ($\sigma/\mu = 0.1$) for LUTs designed for same total active area of (a) 1× (b) 1.5×.

compared to the CSM style. By 50% upsizing of the total active area, the failure rate of the VSM style goes down by 25% and that of the CSM style goes down by only 8%.

Fig. 10 shows the LUT delay distributions and failure rates under intra-die MTJ variations for the two active areas. The VSM style again exhibits lower failure rates. The failure rate of the VSM style is lower by 29% at the 1× area and by 51% at the 1.5× area. Area upsizing is effective in reducing the failure rate in the VSM style. By upsizing the area by 50%, the VSM failure rate decreases by 19% and that of the CSM style increases by 17%. The enhanced reliability of the VSM is attributed to its two-stage signal amplification, first by the cross-coupled PMOSes in the current to voltage convertor and then by the sense amplifier (Fig. 3).

Fig. 11 shows the delay distribution and failure rates of the LUTs under inter-die $V_{th}$ variations. Due to the differential nature of the LUT circuits, both designs exhibit good tolerance to inter-die $V_{th}$ variations, as such variation do not cause mismatch among the transistors on the same circuit. It is observed that the VSM style shows less failure rates for inter-die variations as well. The VSM style shows 99% failure reduction compared to the CSM style. Again, we also observe the effectiveness of transistor upsizing on failure rate reduction for the VSM style as its failure rate goes down to 50% by upsizing whereas that of the CSM style reduces by only 18%.

Fig. 12 shows the delay distributions under the inter-die MTJ variations. Neither of the LUTs shows any failures under the inter-die MTJ variations.

Table 3 summarizes the numerical results of the LUTs for the two active areas. The two styles show comparable delays, but the VSM style exhibits 56% reduction in active power. The CSM style however exhibits 37% less standby power. The leakage difference is due to the fact that in the CSM style the sense amplifier is stacked on top of the selection tree offering additional stacking effect causing leakage reduction on the sense amplifier circuit. However, in the VSM style, the sense amplifier has its own spectate connections to the supply lines offering less stacking effect.

It is observed that transistor variations are much more influential in causing failures in the STT-LUTs than the MTJ variations. This is true for both intra- and inter-die variations. That is because transistor variations impact the sense amplifier whereas the MTJ variation does not affect the sense amplifier.

Under combined transistor and MTJ intra-die variations, the VSM style exhibits 17% to 28% less failure rates. Under combined transistor and MTJ inter-die variations, the VSM style exhibits 96% to 98% less failure rates. These results convincingly show that the VSM style is much more robust STT-LUT under process variations.

## 5. NBTI sensitivity analysis

The bias temperature instability (BTI) is considered a major reliability concern in nano-scale CMOS technologies [12]. It is classified into negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI) [13]. NBTI impacts PMOS and PBTI impacts NMOS transistors. NTBI has been a major concern over the years especially with the emergence of high-K metal gates and the FinFET technology [14]. NBTI increases the PMOS threshold voltage resulting in current reduction and $V_{th}$ mismatch among PMOSes due to its bias and temperature dependence [15]. Therefore, NBTI results in reduction of the lifetime of a chip. This phenomenon is attributed to the $Si/SiO_2$ interface traps and the positive charges resulting from the oxide breakdown of

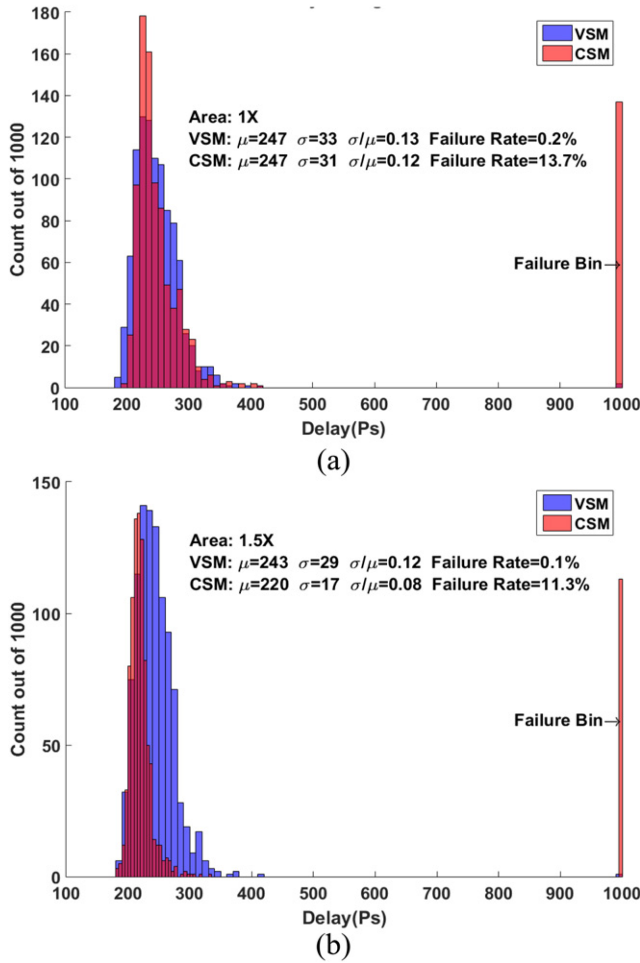



**Fig. 11.** Delay distributions under inter-die $V_{th}$ variation ($\sigma_{Vt} = 23$ mV) for LUTs designed for same total active area of (a) 1× (b) 1.5×.

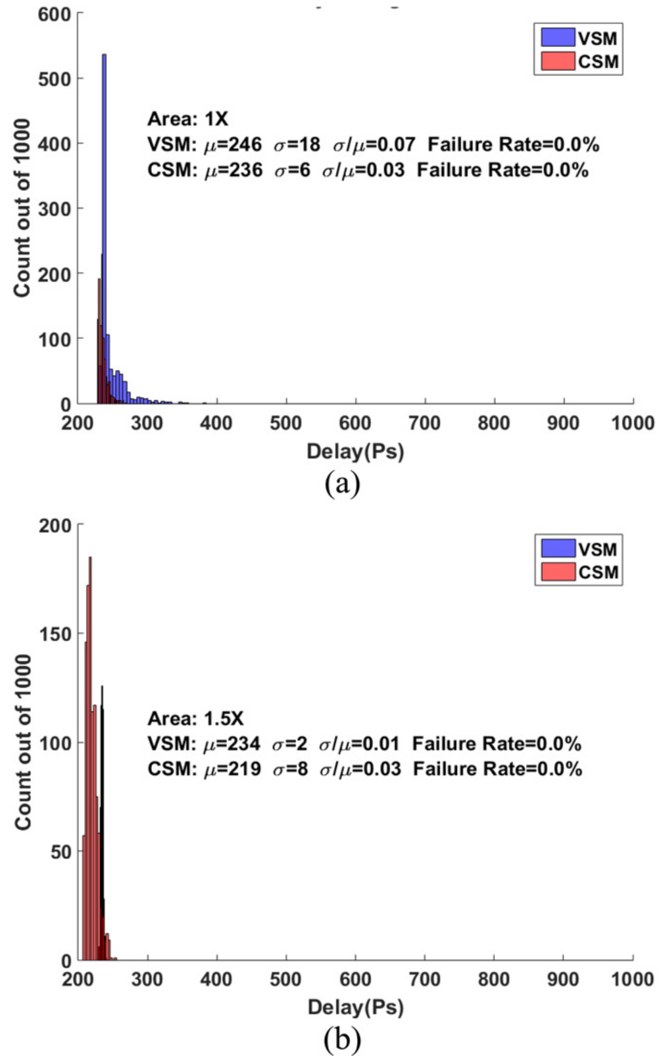



**Fig. 12.** Delay distributions under inter-die MTJ $t_{ox}$ and r variations ($\sigma/\mu = 0.1$) for LUTs designed for same total active area of (a) 1× (b) 1.5×.

Si–H bonds at the interface of Si/$SiO_2$ at high temperatures under a negative bias. It should be noted that while this paper focuses on the NBTI effect, the presented approach can be extended to analyze the impact of PBTI, or both BTI effects.

### *5.1. NBTI modeling*

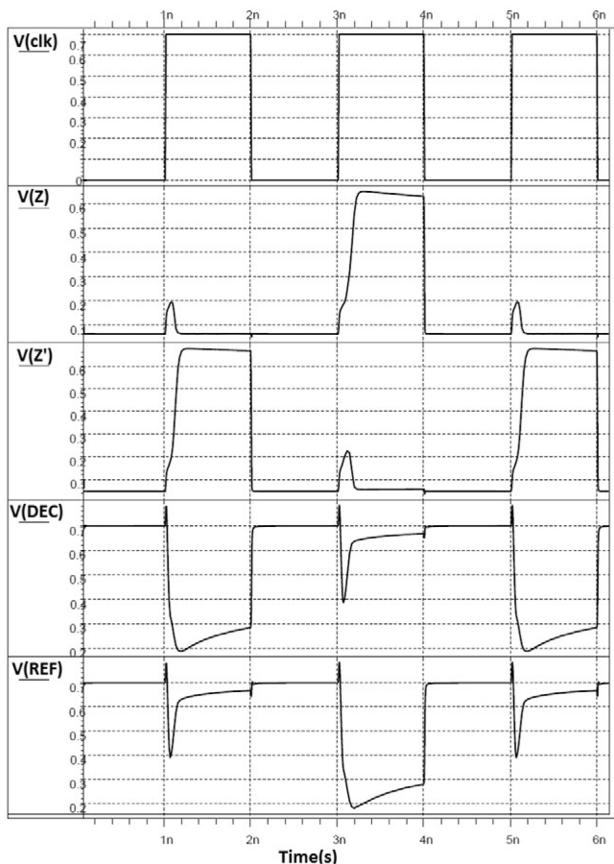
There have been several NBTI models proposed in the literature [16,17,22–24]. NBTI is stress bias dependent and is partially recoverable by reduction or removal of the stress bias. Therefore, there is a considerable difference between the NBTI caused by a constant DC stress and an AC stress-recovery pattern [22,23]. Given the dynamic operation of the STT-LUTs, the transistors experience an AC stress pattern. We use a logarithmic NBTI model for cycle-to-cycle prediction of NBTI proposed in [23]. According to this model, the threshold voltage ($V_{th}$) shift due to NBTI is bias ($V_{sg}$) and temperature (T) dependent. $V_{th}$ drift due to NBTI is modeled as follows [23]:

$$
\begin{aligned}
&\Delta V_{th}\,(t+t_0) = \Delta_1 + \Delta_2 \\
&\Delta_1 = \varphi(A + B\log(1 + C\cdot t)) \\
&\Delta_2 = \Delta V_{th}\,(t_0)\left(1 - \frac{k + \log(1 + C\cdot t)}{k + \log(1 + C\cdot (t + t_0))}\right) \\
&\varphi = \varphi_0 \exp\left(\frac{\beta V_{sg}}{T_{ox}\cdot KT}\right)\cdot \exp\left(-\frac{E_0}{KT}\right)
\end{aligned} \tag{9}
$$

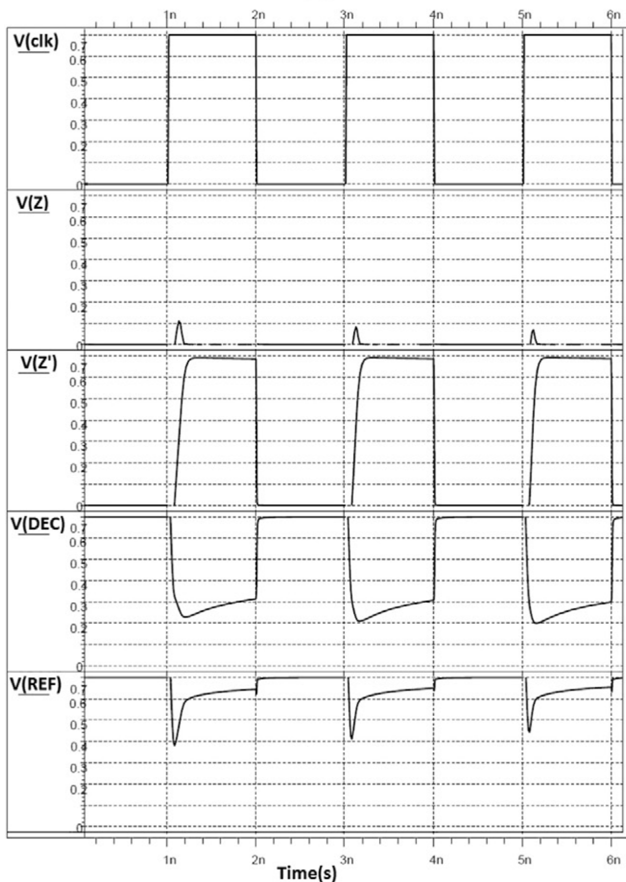
where $T_{ox}$ is the oxide thickness, K is the Boltzmann constant, T is the temperature in Kelvin, $t_0$ is the initial time of a given cycle when the voltage $V_{sg}$ is applied, and t is the time duration the voltage $V_{sg}$ is kept, $\Delta V_{th}\,(t_0)$ is initial threshold voltage shift which is the final threshold voltage shift from the previous cycle. A, B, C, β, $\varphi_0$, $E_0$, and k are

**Table 3**
Simulation results in 16 nm bulk CMOS at clock frequency = 0.5 GHz, $V_{dd} = 0.7$ V, T = 110 °C, $V_{th}$ variation: $\sigma_{Vt} = 23$ mV, $\sigma/\mu = 0.1$, MTJ $t_{ox}$ and r variation: $\sigma/\mu = 0.1$.

| Metric | Area = 1× 0.02856 $\mu m^2$ | | Area = 1.5× 0.04284 $\mu m^2$ | |
|---|---|---|---|---|
| | VSM | CSM | VSM | CSM |
| Nominal delay (ps) | 234.8 | 229.4 | 234.0 | 217.7 |
| Active power (μW) | 0.572 | 1.306 | 0.871 | 1.976 |
| PDP (aj) | 134.3 | 299.6 | 203.9 | 430.2 |
| Standby power (nW) | 6.574 | 4.149 | 10.95 | 6.933 |
| %Failure rate under intra-die $V_{th}$ variation | 78.5 | 93.1 | 58.5 | 85.8 |
| %Failure rate under intra-die MTJ $t_{ox}$ and r variations | 24.6 | 34.8 | 20.0 | 40.7 |
| %Failure rate under combined intra-die $V_{th}$ and MTJ $t_{ox}$ and r variations | 78.4 | 94.5 | 63.7 | 89.0 |
| %Failure rate under inter-die $V_{th}$ variation | 0.2 | 13.7 | 0.1 | 11.3 |
| %Failure rate under inter-die MTJ $t_{ox}$ and r variations | 0 | 0 | 0 | 0 |
| %Failure rate under combined inter-die $V_{th}$ and MTJ $t_{ox}$ and r variations | 0.6 | 14.5 | 0.2 | 10.7 |




(a)



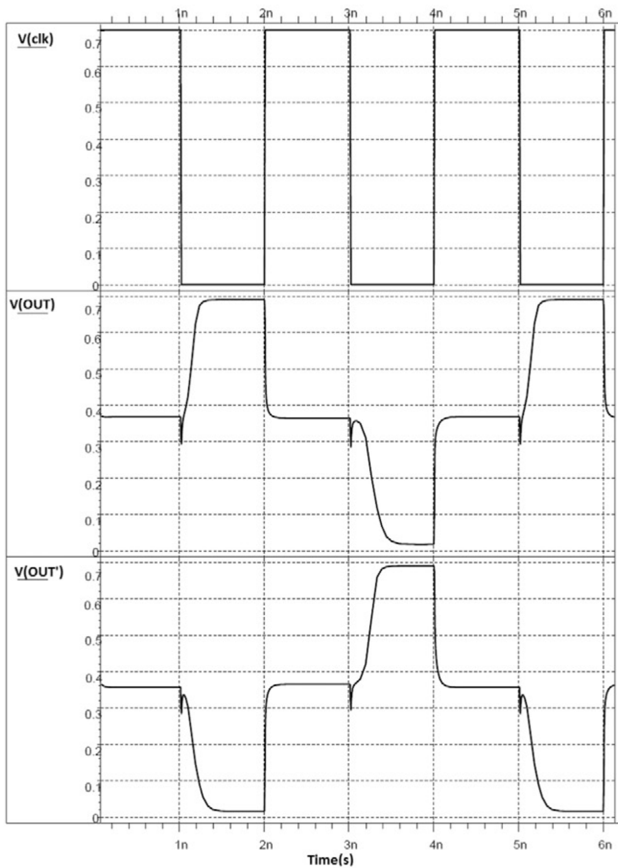

(b)

**Fig. 13.** Waveform patterns corresponding to (a) symmetric and (b) asymmetric NBTI aging in VSM STT-LUT.

constants [23]. Under the constant DC stress, the following model predicts the NBTI over time [23]:

$$\Delta V_{th}(t) = \varphi(A + B\log(1 + C \cdot t)). \tag{10}$$

In this work, we have studied the NBTI induced $V_{th}$ increase at the worst case temperature of 110 °C. For the stress time, we consider 0 (initial time), 1E+3 s (1 ks), and 1E+6 s (1 Ms). Given the bias dependence of NBTI, the actual $V_{th}$ increase depends on the PMOS biasing and activity pattern in a given circuit over long periods of time. For example, for a PMOS whose gate is connected to the clock signal (e.g. the perchance transistors MP0, MP7, and MP8 in Fig. 3) the activity pattern is very deterministic in the sense that the PMOS is under stress when the clock signal is low. Assuming a clock signal with 50% duty cycle, the precharge PMOSes are under full stress for half the clock period and under full recovery for the other half period. Eq. (9) is iteratively solved from one half clock period to another to estimate NBTI after the desired life-time. For other PMOS transistors, the stress time and voltage is data and bias dependent. For example, the output connected PMOSes in the VSM STT-LUT (MP3 or MP4 in Fig. 3) or CSM STT-LUT (MP0 or MP1 in Fig. 4), are under stress anytime the corresponding output (OUT (Z) or OUT′ (Z′)) is low, and this make their aging dependent on the output data activity pattern which is related to the data stored in the LUT and the input activity pattern. Similarly, the aging of the PMOSes connected to the selection and reference trees (MP5 and MP6 in Fig. 3) is dependent on the data activity pattern. Given the differential nature of the sensing circuits, the PMOSes that are paired (i.e. (MP3, MP4) and (MP5, MP6) in Fig. 3 and (MP0, MP1) in Fig. 4) are expected to have same driving strength (i.e. sizing and $V_{th}$) for maximum variation tolerance and yield. However, the data activity dependence of NBTI aging may result in asymmetric aging and hence increased mismatch among the paired transistors. Hence, we consider two scenario of NBTI aging: symmetric vs. asymmetric NBTI aging of the paired transistors. In the symmetric case, the output has same probability of switching to one or zero in a given clock evaluation cycle and hence the pair transistors age at the same rate. For the asymmetric case, we consider a worst case scenario that the output has 100% probability of obtaining the same logical value at every clock evaluation cycle. Another factor that influences the rate of NBTI aging is the $V_{sg}$ bias when the transistor is under stress. For the precharge transistors whose gate is connected to the clock signal, their $V_{sg}$ bias is at maximum $V_{dd}$ when the clock signal is low. Similarly for the PMOSes whose gates are connected to the outputs in the VSM-LUT circuit (MP3 and MP4 in Fig. 3), their $V_{sg}$ bias is maximum when under stress because the outputs are full swing. The $V_{sg}$ stress for the remaining PMOSes may not be full $V_{dd}$ because their gates may not experience full voltage swing. For example, nodes DEC and REF in Fig. 3 swing between $V_{dd}$ and $0.5V_{dd}$ according to the simulation waveforms (Fig. 13). Hence, when under stress, MP5 and MP6 in Fig. 3 are stressed at $V_{sg} = 0.5V_{dd}$. MP0 and MP1 in CSM STT-LUT (Fig. 4) experience stress at two possible $V_{sg}$ biases ($V_{dd}$ and $0.5V_{dd}$). In the precharge mode, when clock is high, the outputs (OUT and OUT′) are tied together and reach $0.5V_{dd}$ (see waveform in Fig. 6(b)). In this case, both MP0 and MP1 are under stress at $V_{sg} = 0.5V_{dd}$. When clock switches low, one of the outputs switches to $V_{dd}$ and the other one to zero. Therefore, when clock is low, one of the PMOSes will experience no stress and the other one stress at full $V_{sg} = V_{dd}$. With this understanding and definitions, we can now discuss the symmetric and asymmetric NBTI aging for VSM and CSM ST-LUT circuits. Due to the differential nature of the read circuit in STT-LUTs, if the outputs switch uniformly in time between logic '0' and '1' states, the PMOSes in a pair will age symmetrically. If the output predominantly switches to only one logical state in each read cycle, then the aging



(a)

(b)

**Fig. 14.** Waveform patterns corresponding to (a) symmetric and (b) asymmetric NBTI aging in CSM STT-LUT.

between the PMOSes in a pair will be asymmetric (one will age more than the other).

*5.1.1. VSM STT-LUT symmetric NBTI aging*

The output waveforms corresponding to this stress pattern are shown in Fig. 13(a). In one cycle, output (Z) switches to high and in the next cycle inverted output (Z′) does. MP3 (MP4) is under full stress ($V_{sg} = V_{dd}$) anytime Z (Z′) is low. Hence, for 1.5 clock period, MP3 (MP4) is under full $V_{dd}$ stress and for 0.5 clock period, it is under full recovery ($V_{sg} = 0$). MP5 and MP2 (MP6 and MP1) are under stress when the node REF (DEC) drops below $V_{dd} - V_{th}$. These nodes drop as low as $0.5V_{dd}$ during the evaluation phase of the clock (Fig. 13(a)). Hence, the NBTI aging of MP1, MP2, MP5 and MP6 should be estimated for a cyclic pattern composed of $V_{sg} = 0.5V_{dd}$ stress for 0.5 clock period, and full recovery for 1.5 clock period.

*5.1.2. VSM STT-LUT asymmetric NBTI aging*

The output waveforms corresponding to this stress pattern are shown in Fig. 13(b). Only one of the outputs (Z′) switches to high every cycle; while the other output (Z) stays low all the time. In this case, MP3 is constantly under full stress ($V_{sg} = V_{dd}$), while MP4 is under full stress for half the clock period and under no stress (i.e. recovery) for the other half period. In this case, MP3 ages faster than MP4 and gains higher $V_{th}$ over time, hence asymmetric aging. Similarly, since the voltage of the node REF remains at $V_{dd}$, MP2 and MP5 are not stressed at all and MP1 and MP6 are under $V_{sg} = 0.5V_{dd}$ stress for half the clock period and no stress for the other half period. This also results in asymmetric aging and hence increased mismatch of MP2 (MP5) and MP1 (MP6).

*5.1.3. CSM STT-LUT symmetric NBTI aging*

The output waveforms corresponding to this stress pattern are shown in Fig. 14(a). In one cycle, output (OUT) switches to high and the inverted output (OUT′) switches to low, and in the next cycle, the opposite transitions occur. Both MP0 and MP1 are under stress of $V_{sg} = 0.5V_{dd}$ in the precharge phase (CLK = 1) which lasts half the clock period. MP0 (MP1) is under full stress $V_{gs} = V_{dd}$ when OUT (OUT′) switches to zero, which lasts half the clock period. MP0 (MP1) is under no stress (i.e. recovery) when OUT (OUT′) switches to one, which lasts half the clock period. The period of the output waveform is twice that of the clock period. The net effect of NBTI aging is computed using the cycle-to-cycle NBTI model, where each cycle is composed of four voltage levels each lasting for half the clock period.

*5.1.4. CSM STT-LUT asymmetric NBTI aging*

The output waveforms corresponding to this stress pattern are shown in Fig. 14(b). Only one of the outputs (OUT) switches to high every cycle; while the other output (OUT′) switches low. Both outputs remain at $0.5V_{dd}$ in the precharge phase (CLK = 1). Hence, MP0 and MP1 are under $V_{sg} = 0.5V_{dd}$ stress for half the clock period. MP1 is additionally under $V_{sg} = V_{dd}$ stress for the other half period. MP0 however is under full recovery ($V_{sg} = 0$) for the other half period. This asymmetric NBTI aging between MP0 and MP1 results in increased $V_{th}$ mismatch between these two transistors.

*5.2. Failure rate analysis under NBTI*

Now we perform Monte Carlo simulations as explained in Section 4 for failure rate measurements under intra-die $V_{th}$ variations; however, after applying symmetric and asymmetric scenarios of NBTI aging for PMOSes after life-times of 0, 1 ks, and 1 Ms. For the PMOS transistors, the NBTI induced $V_{th}$ shift is added as a fixed change to the $V_{th}$ in addition to the random change caused by the intra-die $V_{th}$ variations. We

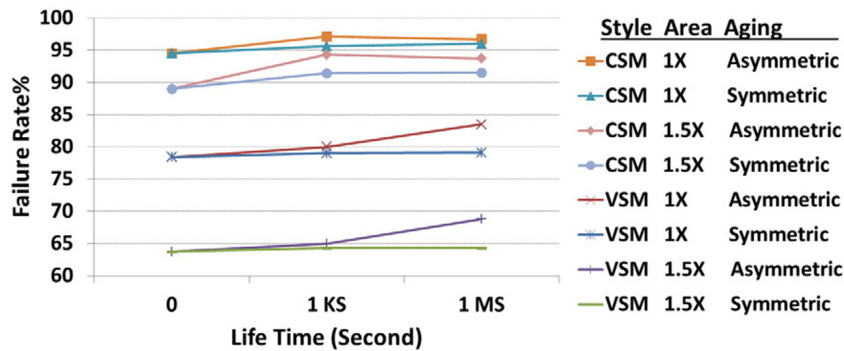



**Fig. 15.** Increase in %Failure rate (under intra-die $V_{th}$ and MTJ variations) over life time due to NBTI.

also perform this simulation for two circuit areas that were considered in Section 4. The results are shown in Fig. 15. It is observed that the failure rate increases with NBTI aging in all cases. Moreover, as expected we note that the failure rate increases at a higher rate in the asymmetric scenario of aging as compared to the symmetric scenario for all the cases. We can argue that the symmetric scenario of aging represents the best case of impact of NBTI aging on the failure rate and the asymmetric scenario represents the worst case impact. In the 1 Ms lifetime, the failure rate increase is 0.9% to 8% for the VSM STT-LUT and 1.6% to 5.3% for the CSM STT-LUT. The increasing failure rates over time do not change the relative failure rate comparisons of the VSM and CSM STT-LUTs. The results in Fig. 15 reaffirm that the VSM STT-LUT is significantly more reliable against $V_{th}$ variations and NBTI aging than the CSM STT-LUT for a given circuit area, and the reliability improves by increasing the circuit area.

## 6. Conclusion

Reliability assessment of various circuit design styles is an important consideration in nano-scale CMOS/MTJ hybrid technologies. This paper performed a comparative reliability analysis of the STT-based LUTs and determined that the VSM style shows superior reliability as compared to the CSM style under same design area. This reliability enhancement is present against not only transistor variations but also MTJ variations. The VSM improved reliability also comes with less propagation delay and active power consumption. Moreover, the improved reliability of the VSM style is maintained under NBTI aging.

## Acknowledgments

This research is funded by the Defense Advanced Research Projects Agency (DARPA-AirForce, FA8650-15-C-7569) of the USA.

## References

[1] C. Augustine, N.N. Mojumder, F. Xuanyao, S.H. Choday, S.P. Park, K. Roy, Spin-transfer torque MRAMs for low power memories: perspective and prospective, IEEE Sensors J. 12 (4) (2012) 756–766.
[2] N. Nishimura, T. Hirai, A. Koganei, T. Ikeda, K. Okano, Y. Sekiguchi, Y. Osada, Magnetic tunnel junction device with perpendicular magnetization films for high-density magnetic random access memory, J. Appl. Phys. 91 (8) (2002) 5246–5249.
[3] M. Rasquinha, D. Choudhary, S. Chatterjee, S. Mukhopadhyay, S. Yalamanchili, An energy efficient cache design using spin torque transfer (STT) RAM, ACM/IEEE International Symposium on Low-Power Electronics and Design 2010, pp. 389–394.
[4] S. Paul, et al., A circuit and architecture codesign approach for a hybrid CMOS-STTRAM nonvolatile FPGA, IEEE Trans. Nanotechnol. 10 (3) (2011).
[5] F. Ren, D. Markovic, True energy-performance analysis of the MTJ-based logic-in-memory architecture (1-bit full adder), IEEE Trans. Electron Devices 57 (5) (2010) 1023–1028.
[6] D. Suzuki, et al., Fabrication of a nonvolatile lookup-table circuit chip using magneto/semiconductor-hybrid structure for an immediate-power-up field programmable gate array, Symposium on VLSI Circuits 2009, pp. 80–81.
[7] W. Zhao, E. Belhaire, C. Chappert, Spin transfer torque (STT)-MRAM-based runtime reconfiguration FPGA circuit, ACM Trans. Embed. Comput. Syst. 9 (2) (2009).
[8] X. Wang, W. Zhu, S. Markus, D. Dimitrov, Spin torque induced magnetization switching variations, IEEE Trans. Magn. 45 (4) (Apr. 2009) 2038.
[9] Y. Zhang, X. Wang, H. Li, Y. Chen, STT-RAM cell optimization considering MTJ and CMOS variations, IEEE Trans. Magn. 47 (10) (2011) 2962–2965.
[10] PTM: predictive technology model, http://www.eas.asu.edu/~ptm.
[11] K. Chun, H. Zhao, J.D. Harms, T. Kim, J.P. Wang, C.H. Kim, A scaling roadmap and performance evaluation of in-plane and perpendicular MTJ based STT-MRAMs for high-density cache memory, IEEE J. Solid State Circuits. 48 (2) (Feb. 2013) 598–610.
[12] S. Krishnan, V. Narayanan, E. Cartier, D. Ioannou, K. Zhao, T. Ando, U. Kwon, B. Linder, J. Stathis, M. Chudzik, A. Kerber, K. Choi, Bias temperature instability in high-κ/metal gate transistors — gate stack scaling trends, IEEE International Reliability Physics Symposium (IRPS), 2012 (pp. 5A.1.1–5A.1.6).
[13] M. Cho, A. Aoulaiche, R. Degraeve, B. Kaczer, J. Franco, T. Kauerauf, P. Roussel, L.A. Ragnarsson, J. Tseng, T.Y. Hoffmann, G. Groeseneken, Positive and negative bias temperature instability on sub-nanometer eot high-K MOSFETs, IEEE International Reliability Physics Symposium (IRPS) 2010, pp. 1095–1098.
[14] K.T. Lee, et al., Technology scaling on high-K & metal-gate FinFET BTI reliability, IEEE International Reliability Physics Symposium (IRPS), 2013 (pp. 2D.1.1–2D.1.4).
[15] T.B. Chan, et al., On the efficacy of NBTI mitigation techniques, Design, Automation & Test in Europe Conference & Exhibition (DATE) 2011, pp. 1–6.
[16] Rakesh Vattikonda, Wenping Wang, Yu Cao, Modeling and minimization of PMOS NBTI effect for robust nanometer design, Design Automation Conference, July 2006.
[17] B.C. Paul, et al., Impact of NBTI on the temporal performance degradation of digital circuits, IEEE Electron Device Lett. 26 (8) (Aug 2005).
[18] Jing Li, Charles Augustine, Sayeef Salahuddin, Kaushik Roy, Modeling of failure probability and statistical design of spin-torque transfer magnetic random access memory (STT MRAM) array for yield enhancement, Design Automation Conference June 2008, pp. 278–283.
[19] Kyungmin Kim, Changsik Yoo, Variation-tolerant sensing circuit for spin-transfer torque MRAM, IEEE Trans. Circuits Syst. II Express Briefs 62 (12) (Dec. 2015) 1134–1138.
[20] Zhenyu Sun, Hai Li, Yiran Chen, Xiaobin Wang, Variation tolerant sensing scheme of spin-transfer torque memory for yield improvement, IEEE/ACM International Conference on Computer-Aided Design 2010, pp. 432–437.
[21] Wang Kang, Zheng Li, Yuanqing Cheng, J.-O. Klein, Youguang Zhang, D. Ravelosona, C. Chappert, Weisheng Zhao, A dynamic reference scheme to improve the sensing reliability of magnetic random access memory, IEEE International Conference on Solid-State and Integrated Circuit Technology 2014, pp. 1–3.
[22] K. Sutaria, A. Ramkumar, R. Zhu, R. Rajveev, Y. Ma, Y. Cao, BTI-induced aging under random stress waveforms: modeling, simulation and silicon validation, Design Automation Conference July 2014, pp. 1–6.
[23] J.B. Velamala, K.B. Sutaria, H. Shimuzu, H. Awano, T. Sato, G. Wirth, Y. Cao, Logarithmic modeling of BTI under dynamic circuit operation: static, dynamic and long-term prediction, IEEE International Reliability Physics Symposium (IRPS), 2013.
[24] K. Joshi, S. Mukhopadhyay, N. Goel, N. Nanware, S. Mahapatra, A detailed study of gate insulator process dependence of NBTI using a compact model, IEEE Trans. Electron Devices 61 (2) (2014) 408–415.
[25] A.R. Asmhamagari, H. Mahmoodi, T. Mohsenin, H. Homayoun, Reconfigurable STT-NV LUT-based functional units to improve performance in general-purpose processors, Great Lake Symposium on VLSI May 2014, pp. 1–6.
[26] A.R. Asmhamagari, H. Mahmoodi, T. Mohsenin, H. Homayoun, Exploiting STT-NV technology for reconfigurable, high performance, low power, and low temperature functional unit design, Design, Automation & Test in Europe Conference and Exhibition (DATE) Mar. 2014, pp. 1–6.
[27] Ji-Seong Doh, Dae-Wook Kim, Sang-Hoon Lee, Jong-Bae Lee, Young-Kwan Park, Moon-Hyun Yoo, Jeong-Taek Kong, A unified statistical model for inter-die and intra-die process variation, International Conference on Simulation of Semiconductor Processes and Devices 2005, pp. 131–134.
[28] Y. Taur, T.H. Ning, Fundamentals of Modern VLSI Devices, Cambridge Univ. Press, New York, 1998.
[29] Y. Zhang, et al., Compact modeling of perpendicular-anisotropy CoFeB/MgO magnetic tunnel junctions, IEEE Trans. Electron Devices 59 (3) (Mar. 2012) 819–826.