Houman Homayoun

Email: hhomayou@gmu.edu
Web: http://ece.gmu.edu/~hhomayou/
https://nsfchest.org/
Lab: ASEEC: Accelerated, Secure, and Energy-Efficient Computing Lab
Department of Electrical and Computer Engineering
Department of Computer Science (Courtesy Appointment)
Department of Information Sciences and Technology (Courtesy Appointment)
George Mason University
Office: 3223, Engineering Building, Phone: (703) 993-5430

EDUCATION

- **Postdoc** *Sept. 2010-Aug. 2012*

Department of Computer Science and Engineering, University of California, San Diego
Mentor: Prof. Dean Tullsen

- **PhD**

Department of Computer Science, University of California, Irvine. *Sept. 2006-Sept. 2010*

- Thesis: Beyond Memory Cells for Leakage and Temperature Control in SRAM-based Units, the Peripheral Circuits Story.

Advisors: Prof. Alex Veidenbaum, Prof. Jean-Luc Gaudiot, Prof. Fadi Kurdahi

- **Master of Applied Science** *September 2003-March 2005*

Electrical and Computer Engineering Department, University of Victoria, Canada.

- Thesis: Using Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation.

- **Bachelor of Science** *October 1998-May 2003*

Electrical and Computer Engineering Department, Sharif University of Technology.

EMPLOYMENT

- *Associate Professor*, University of California Davis, Department of Electrical and Computer Engineering *August 2019 - present*
- *Associate Professor*, George Mason University, Department of Electrical and Computer Engineering, Courtesy Appointment with the Department of Computer Science, Courtesy Appointment with the Department of Information Sciences and Technology *August 2018 - August 2019*
- *Advisory Committee, Research and Technology Commercialization (R&TC), Cybersecurity working group, Commonwealth of Virginia* *May 2018 - present*
- *Assistant Professor*, George Mason University, Department of Electrical and Computer Engineering, Courtesy Appointment with the Department of Computer Science, Courtesy Appointment with the Department of Information Sciences and Technology. *Aug. 2012-August 2018*
- *Board of Advisory Member*, BroadPak Corporation, Santa Clara, California, USA. *July 2012-Present*
- *NSF/CCC-CRA Computing Innovation Fellow*, University of California San Diego, Department of Computer Science and Engineering (Mentor: Dean M. Tullsen) *Sept. 2010-Aug. 2012*
- *Graduate Research Assistant*, University of California, Irvine, Department of Computer Science (Advisors: Alex Veidenbaum, Jean-Luc Gaudiot and Fadi Kurdahi) *Sept. 2006-Sept. 2010*
- *Design Architect*, Novelics Inc., Aliso Viejo, California, USA. *Jan. 2007-Oct. 2008*
- *Researcher Assistant*, McMaster University, Canada, Department of Electrical and Computer Engineering. *Oct. 2005-Apr. 2006*
- *Graduate Research Assistant*, University of Victoria, Canada, Department of Electrical and Computer Engineering. *Sept. 2003-Mar. 2005*
- *Research Assistant*, Sharif University Technology, Tehran, Electronic Research Center. *Oct. 2002-Jun. 2003*

GRANTS

Sponsored Research: Total $7,474,804.
Funding from DARPA SHIELD, DARPA SSITH, DARPA OMG, NSF CPS, NSF CNS, NSF

IUCRC, NSF CI, NIST and GM

- *"IUCRC UC Davis: Center for Hardware and Embedded System Security and Trust (CHEST)"* *2019-2023*
  https://nsfchest.org/
  NSF IUCRC, **(PI), $750,000.**
  Role: PI and UC Davis Site Director, Directing CHEST Industry-University Cooperative Research Center. Collaborating with other sites including Northeastern University, University of Connecticut, University of Texas at Dallas, University of Virginia, and University of Cincinnati to work with lead industries on challenging HW security research problems.
- *"EAGER: Run-Time Hardware-Assisted Malware Detection Using Machine Learning"* *2019-2021*
  NSF CSR-CNS, **(PI)**, **$237,134**.
  Role: Develop advance machine learning model to detect unknown malware, using microarchitecture information captured by hardware performance counters.
- *"Planning IUCRC George Mason University: Center for Hardware and Embedded System Security and Trust (CHEST)"* https://nsfchest.org/ *2018-2019*
  NSF IUCRC Planning, **(PI), $15,000.**
  Role: PI and Center Director on GMU site, A collaborative effort composed of George Mason University, Northeastern University, University of Connecticut, University of Texas at Dallas, University of Virginia, and Wright State University to establish the first NSF/AFRL center on HW and Embedded Systems Security and Trust.
- *"Obfuscated Logics to Enhance Security and Prevent Reverse Engineering"* *2018-2021*
  DARPA MTO Office, **(PI), $1,800,000.** ($600K fab cost to GF), **PM: Kerry Bernstein**
  Role: Team lead on design and fabricating obfuscated logics in 14nm with GlobalFoundries.
- *"Mobilizing the Micro-Ops: Securing Processor Architectures via Context Sensitive Decoding"* *2017-2020*
  DARPA MTO Office, **SSITH program (PI on GMU site), Total: $1,200,000. GMU share ($400,000), PM: Linton Salmon**
  Role: Leading the team to detect HW vulnerabilities in out-of-order processors
- *"Evolution of Computer Vision for Low Power Devices, Breaking its Power Wall and Computational Complexity"* *2017-2020*
  NSF CSR-CNS, **(Co-PI)**, **$500,000**.
  Role: Developing an approximate Iterative Convolutional Neural Network coprocessor that supports approximation in memory and logic.
- *"3D-Split of Obfuscation and Authentication of logic"* *2016-2017*
  DARPA MTO Office, **OMG Program (Co-PI)**, **$495,000. PM: Ken Plaks**
  Role: Developing 3D-SOUL secure-compiler for cell, route and FSM obfuscation.
- *"Persistence and Extraction of Digital Artifacts from Embedded Systems"* *2015- 2016*
  NIST, National Cybersecurity Center of Excellence,
  (Co-PI), $75,000.
  Role: Establishing the persistence of digital artifacts on embedded systems through JTAG analysis.
- *"Hybrid Spin Transfer Torque-CMOS Technology to Prevent Design Reverse Engineering"* DARPA MTO Office, **(PI), $349,000. PM: Kerry Bernstein** *2015- 2017*
  Role: Directing the project to design and deploy new circuit methods to build reconfigurable logics to enhance performance and power efficiency.
- *"Heterogeneous Ultra Low Power Accelerator for Wearable Biomedical Computing"* *2015- 2019*
  NSF CSR-CNS, **(PI),** Total **$500,000,** GMU portion **$288,000.**
  Role: Directing the project to design and deploy new circuit methods to build reconfigurable logics to enhance performance and power efficiency.
- *"A Novel Biomechatronic Interface Based on Wearable Dynamic Imaging Sensors"* *2013- 2018*
  NSF CPS – CNS, **(Co-PI) $995,000.**
  Role: Designing a heterogeneous architecture for computing intensive biomedical application, Compare with state-of-the-art heterogeneous platforms such as TI OMAP and Nvidia Tegra.
- "*Enhancing the Security on Embedded Automotive Systems*" *2013- 2016*

General Motors, **(Co-PI) $261,000.**
Role: Hacking the CAN Bus Network of GM Cars.

- "*Inter-core Selective Resource Pooling in a 3D Chip Multiprocessor*" *2010- 2012*
  NSF CI Fellow Award, NSF 1019343/CRA Sub Award CIF-B-68, (**PI), $280,000**.

Equipment Support from Industry
- Nvidia Corporation: 2 Tesla K40 GPU for CNN training, **$9,560** *2017*
- Xilinx Corporation, 12 Xilinx ZYNQ board for HW accelerated computer vision, **$5,940** *2016*
- Intel Corporation, 20 Intel Galileo and Intel Edison board for wearable computing, **$2,170** *2015*

RESEARCH INTEREST

- **Computer System Cybersecurity (Current)**
  - Online malware detection
  - Adversarial machine learning
  - Side-channel processor architecture defense and attack
  - Detecting and containing malware epidemic in IoT network
  - Reverse engineering, logic locking, obfuscation and camouflaging
  - Hardware Trojan detection
- **Applied Machine Learning (Current)**
  - Machine learning algorithm optimization for energy-efficient acceleration of Big Data
  - Deep machine learning and data mining acceleration
  - Applied machine learning for cloud workload management, scheduling and tuning
  - Run-time machine learning for malware detection
  - Machine learning security, adversarial ML
- **Heterogeneous Architecture Design and Management (Current)**
  - Design space exploration of FPGA+CPU architecture for emerging big data frameworks
  - Scheduling and resource management in heterogeneous multicore CPU+FPGA architectures
  - Accelerator design for wearable biomedical applications
  - 3D dynamic heterogeneous architecture design
- **Emerging Memory Technologies (Current)**
  - Emerging DRAM architectures in 3D (HMC, Wide I/O) for big data applications
  - Non-volatile logic and memory design
- **Power and Thermal Management**
  - Power/thermal and reliability issue in 3D architecture
  - Power management in emerging non-volatile memories
  - Power and energy optimization in VLSI circuits
  - Reliability-aware memory design
  - Dynamic power/thermal management in multi/many-core systems
  - Energy efficiency and power management in enterprise datacenter

PUBLICATIONS

Publication Summary:

Topic	Number of Publications	Conference/Journal
Computer Security	29	CHES, RAID, DAC, TODAES, ASPDAC, IOLTS, ISVLSI, ISQED, ICCD, DATE, CASES, ICCAD, GLSVLSI, TRUSTCOM
Applied Machine Learning	27	ASPDAC, CASES, DAC, DATE, ICCD, ISQED, IISWC, FCCM, ICCAD, CODES-ISSS, CCGRID, ASAP, GLSVLSI, ASPDAC, ICCD, TVLSI
Big Data Computing (energy-efficient computing,	26	CCGRID, SoCC, TSMSCS, TOMPECS, TECS, JPDC, JPDC, TMSCS, ICCD, DAC, IISWC,

hardware accelerator)		ISPASS, FCCM, Big Data, CF, SAMOS, IGSC, DATE
Resource Management	56	ISCA, HPCA, TODAES, TVLSI, JETC, TVLSI, TVLSI, MR, TECS, CAL, JSC, TVLSI, LCTES, SAMOS, IGSC, GLSVLSI, ICCD, DATE, DAC

Conference/Journal	Number of Publications	Conference/Journal	Number of Publications	Conference/Journal	Number of Publications
DAC	10	ISCA	1	CASES	7
DATE	9	HPCA	1	CODES-ISSS	2
ISLPED	3	ISPASS	1	IISWC	3
ASPDAC	5	TVLSI	10	ISQED	8
ICCD	11	GLSVLSI	8	TMSCS	2
TODAES	2	TECS	4	SoCC	1
TOMPECS	1	JETC	2	CAL	1
CHES	1	LCTES	1	ISVLSI	3
ICCAD	2	CF	3	ISCAS	3
FCCM	3	Big Data	2	CCGRID	2
RAID	1	ICDM	2	VTS	1
RECONFIG	2	BSN	1		

Journal Papers

(26) *"ICNN: The Iterative Convolutional Neural Network"* ***TECS***
Katayoun Neshatpour, **Houman Homayoun**, Avesta Sasan
IEEE Transaction on Embedded Computing Systems (TECS 2020)

(25) *"Application and Thermal-reliability-aware Reinforcement Learning Based Multi-core Power Management"* ***JETC***
Sai Manoj Pudukotai Dinakarrao, Arun Joseph, Anand Haridass, Muhammad Shafique, Jörg Henkel, **Houman Homayoun**
ACM Journal on Emerging Technologies in Computing Systems, Volume 15, Issue 4 (JETC 2019)

(24) *"SMT Attack: Next Generation Attack on Obfuscated Circuits with Capabilities and Performance Beyond The SAT Attacks"* ***CHES***
Kimia Zamiri Azar, Hadi Mardani Kamali, Avesta Sasan, **Houman Homayoun**
IACR Transactions on Cryptographic Hardware and Embedded Systems, Volume 29 (CHES 2019)

(23) *"Programmable Gates Using Hybrid CMOS-STT Design to Prevent IC Reverse Engineering"* ***TODAES***
Theodore Winograd, Hassan Salmani, Hamid Mahmoodi, Kris Gaj, **Houman Homayoun**
ACM Transactions on Design Automation of Electronic Systems, Special issue on Internet of Things System Performance, Reliability, and Security, 2018.

(22) "Optimal Allocation of Computation and Communication in an IoT Network" ***TODAES***
Abhimanyu Chopra, Hakan Aydin, Setareh Rafatirad, **Houman Homayoun**
ACM Transactions on Design Automation of Electronic Systems, Special issue on Internet of Things System Performance, Reliability, and Security, 2018.

(21) "Hardware Accelerated Mappers for Hadoop MapReduce Streaming" ***TMSCS***
Katayoun Neshatpour, Maria Malik, **Houman Homayoun**
IEEE Transactions on Multi-Scale Computing Systems, 2018.

(20) "System and Architecture Level Characterization of Big Data Applications on Big and Little Core Server Architectures" ***TOMPECS***
Maria Malik, Katayoun Neshatpour, Setareh Rafatirad, **Houman Homayoun**
ACM Transactions on Modeling and Performance Evaluation of Computing Systems, 2018.

(19) *"Low Overhead CS-based Heterogeneous Framework for Big Data Acceleration"* ***TECS***
Amey Kulkarni, Colin Shea, Tahmid Abtahi, **Houman Homayoun** and Tinoosh Mohsenin

ACM Transaction on Embedded Computing Systems, 2018.

(18) *"Big vs Little Core for Energy-Efficient Hadoop Computing"* ***JPDC***
Maria Malik; Katayoun Neshatpour; Setareh Rafatirad; Rajiv V Joshi; **Houman Homayoun**
Elsevier Journal of Parallel and Distributed Computing, Special Issue on Systems for Learning, Inferencing, and Discovering (SLID), 2017.

(17) *"Smart Grid on Chip: Work Load-Balanced On-Chip Power Delivery"* ***TVLSI***
Divya Patahk, **Houman Homayoun**, Ioannis Savidis
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, DOI: 10.1109/ TVLSI.2017.2699644, 2017

(16) *"Energy-Efficient Acceleration of MapReduce Applications Using FPGAs"* ***JPDC***
Katayoun Neshatpour; Maria Malik; **Houman Homayoun**
Elsevier Journal of Parallel and Distributed Computing, Special Issue on Systems for Learning, Inferencing, and Discovering (SLID).

(15) "*An Energy Efficient Programmable Manycore Accelerator for Personalized Biomedical Applications*" ***TVLSI***
Adam Page, Adwaya Kulkarni, Nasrin Attaran, Ali Jafari, Maria Malik, **Houman Homayoun**, and Tinoosh Mohsenin
IEEE Transactions on Very Large Scale Integration (VLSI) Systems

(14) "*Heterogeneous HMC+DDRx Memory Management for Performance-Temperature Trade-offs*" ***JETC***
Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana, Tinoosh Mohsein, **Houman Homayoun**
ACM Journal on Emerging Technologies in Computing, 2017.

(13) "*Sparse Regression Driven Mixture Important Sampling for Memory Design*" ***TVLSI***
Maria Malik, Rajiv Joshi, Rouwaida Kanj, Shupeng Sun, **Houman Homayoun**, Tong Li
IEEE Transactions on Very Large Scale Integration (VLSI) Systems.

(12) "*Hadoop Workloads Characterization for Performance and Energy Efficiency Optimizations on Microservers*" ***TMSCS***
Maria Malik, Katayoun Neshatpour, Avesta Sasan, Setareh Rafatirad, **Houman Homayoun**
IEEE Transactions on Multi-Scale Computing Systems.

(11) "*ElasticCore: A Dynamic Heterogeneous Platform with Joint Core and Voltage/Frequency Scaling*" ***TVLSI***
Mohammad Khavari Tavana, Mohammad Hossein Hajkazemi, Divya Pathak, Ioannis Savidis, **Houman Homayoun**
IEEE Transactions on Very Large Scale Integration (VLSI) Systems.

(10) "*Enhancing Power, Performance, and Energy-efficiency in Chip Multiprocessors Exploiting Inverse Thermal Dependence*" ***TVLSI***
Katayoun Neshatpour, Wane Burleson, Amin Khajeh, **Houman Homayoun**
IEEE Transactions on Very Large Scale Integration (VLSI) Systems.

(9) "*Reliability analysis of spin transfer torque based look up tables under process variations and NBTI aging*". ***MR***
Ragh Kuttappa, **Houman Homayoun**, Hassan Salmani, Hamid Mahmoodi.
Elsevier Microelectronics Reliability Journal, Volume 62, p 156-166, 2016.

(8) "*Using a Flexible Fault-Tolerant Cache to Improve Reliability for Ultra Low Voltage Operation*". ***TECS***
Abbas Banaiyanmofrad, **Houman Homayoun**, Nikil Dutt.
ACM Transactions on Embedded Computing Systems. 14, no. 2 (2015): 32.

(7) "*Resistive Computation: A Critique*". ***CAL***
Hamid Mahmoodi, Sridevi Srinivasan Lakshmipuram, Manish Arora, Yashar Asgarieh, **Houman Homayoun**, Bill Lin and Dean M.Tullsen.
IEEE Computer Architecture Letters, DOI 10.1109/L-CA.2013.23, 2014.

(6) "*Multi-Copy Cache: A Highly Energy Efficient Cache Architecture*". ***TECS***
Arup Chakraborty, **Houman Homayoun**, Amin Khejah, Nikil Dutt, Ahmed Eltawil, Fadi Kurdahi.
ACM Transactions on Embedded Computing Systems (TECS), 2014.

(5) "*Variation Trained Drowsy Cache (VTD-Cache): A History Trained Variation Aware Drowsy Cache for Fine Grain Voltage Scaling*". ***TVLSI***
Avesta Makhzan, Kiarash Amiri, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010 (TVLSI). VOL. 20, Issue 4, pp: 630-642. April 2012.

(4) "*MZZ-HVS: Multi Modes Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On-Chip SRAM Peripheral Circuits*". ***TVLSI***
Houman Homayoun, Avesta Sasan, Alex Veidenbaum, Hsin-Cheng Yao, Shahin Golshan, Payam Heydari.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (TVLSI), VOL. 19, NO. 12, December 2011.

(3) "*On Leakage Power Optimization in Clock Tree Networks for ASICs and General-Purpose Processors*" ***SUSCOM***
Houman Homayoun, Shahin Golshan, Eli Bozorgzadeh, Alex Veidenbaum, Fadi Kurdahi.
Elsevier Journal of Sustainable Computing, Volume 1, Issue 1, March 2011, Pages 75-87 **(Invited paper)**.

(2) "*Inquisitive Defect Cache: A Means of Combating Manufacturing Induced Process Variation*". ***TVLSI***
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010 (TVLSI), VOL. 19, NO. 9, SEPTEMBER 2011.

(1) "*Reducing Power in All Major CAM and SRAM Based Processor Units via Centralized, Dynamic Resource Size Management*". ***TVLSI***
Houman Homayoun, Avesta Sasan, Alex Veidenbaum, Jean-Luc Gaudiot.
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010 (TVLSI), VOL. 19, NO. 11, NOVEMBER 2011.

Conference Papers

2020

(119) *"DFSSD: Deep Faults and Shallow State Duality, A Provably Strong Obfuscation Solution for Circuits with Restricted Access to Scan Chain"* **VTS**
Shervin Roshanisefat, Hadi Mardani Kamali, Kimia Zamiri Azar, Manoj Sai, Naghmeh Karimi, **Houman Homayoun**, Avesta Sasan.
IEEE VLSI Test Symposium (VTS 2020).

(118) *"NESTA: Hamming Weigh Compression-Based Neural Proc. Engine"* **ASPDAC**
Ali Mirzaeian, **Houman Homayoun**, Avesta Sasan
25th Asia and South Pacific Design Automation Conference (ASP-DAC 2020).

(117) *"Mitigating Cache-Based Side-Channel Attacks Through Randomization: A Comprehensive System And Architecture Level Analysis"* **DATE**
Han Wang, Hossein Sayadi, Liang Zhao, Tinoosh Mohsenin, Avesta SasaN, Setareh Rafatirad, **Houman Homayoun**
Design, Automation & Test in Europe, (DATE 2020).

(116) *"Estimating the Circuit De-Obfuscation Runtime based on Graph Deep Learning"* **DATE**
Zhiqian Chen, Gaurav Kolhe, Setareh Rafatirad, Chang-Tien Lu, Sai Manoj Pudukotai Dinakarrao, **Houman Homayoun**, and Liang Zhao
Design, Automation & Test in Europe, (DATE 2020).

2019

(115) *"Security and Complexity Analysis of LUT-based Obfuscation: From Blueprint to Reality"* **(Best Paper Nominee)** **ICCAD**
Gaurav Kolhe, Hadi Mardani Kamali, Miklesh Naicker, Tyler David Sheaves, Hamid Mahmoodi, Sai Manoj Pudukotai Dinakarrao, **Houman Homayoun**, Setareh Rafatirad, Avesta Sasan.
IEEE/ACM International Conference on Computer-Aided Design, (ICCAD 2019).

(114) *"Deep Multi-attributed Graph Translation with Node-Edge Co-evolution"* **(Best Paper Award)** **ICDM**
Xiaojie Guo, Liang Zhao, Cameron Nowzari, Setareh Rafatirad, **Houman Homayoun**, Sai Manoj Pudukotai Dinakarrao
19th IEEE International Conference on Data Mining (ICDM 2019).

(113) *"DynGraph2Seq: Dynamic-Graph-to-Sequence Interpretable Learning for Health Stage Prediction in Online Health Forums"* **ICDM**
Yuyang Gao, Lingfei Wu, **Houman Homayoun**, Liang Zhao
19th IEEE International Conference on Data Mining (ICDM 2019).

(112) *"TCD-NPE: A Re-configurable and Efficient Neural Processing Engine, Powered by Novel Temporal-Carry-deferring MACs"* **RECONFIG**
Ali Mirzaeian, **Houman Homayoun** and Avesta Sasan
IEEE International Conference on Reconfigurable Computing and FPGAs, (Reconfig 2019).

(111) *"Sequence-Crafter: Side-Channel Entropy Minimization to Thwart Timing-Based Side-Channel Attacks"* **CASES**
Abhijitt Dhavlle, Sahil Bhat, Setareh Rafatirad, **Houman Homayoun**
Proceedings of the International Conference on Compliers, Architectures and Synthesis for Embedded Systems Companion (CASES 2019).

(110) *"SAT to SAT-hard Clause Translator"* **CASES**
Rakibul Hassan, Setareh Rafatirad, **Houman Homayoun**, Sai Manoj Pudukotai Dinakarrao
Proceedings of the International Conference on Compliers, Architectures and Synthesis for Embedded Systems Companion (CASES 2019).

(109) *"Resource-Efficient Wearable Computing for Real-Time Reconfigurable Machine Learning: A Cascading Binary Classification"* **BSN**
Mahdi Pedram, Seyed Ali Rokni, Marjan Nourollahi, **Houman Homayoun**, Hassan Ghasemzadeh
16th IEEE International Conference on Wearable and Implantable Body Sensor Networks. (BSN 2019).

(108) *"Parallel Multi-View Graph Matrix Completion for Large Input Matrix"* **CCWC**
Arezou Koohi, **Houman Homayoun**
2019 IEEE 9th Annual Computing and Communication Workshop and Conference (CCWC 2019).

(107) *"Pyramid: Machine Learning Framework to Estimate the Optimal Timing and Resource Usage of a High-Level Synthesis Design"* **FPL**
Hosein Mohammadi Makrani, Farnoud Farahmand, Hossein Sayadi, Sara Bondi, Sai Manoj Pudukotai Dinakarrao, **Houman Homayoun**, Setareh Rafatirad
29th International Conference on Field Programmable Logic and Applications. (FPL 2019)

(106) *"Mitigating the Performance and Quality of Parallelized Compressive Sensing Reconstruction Using Image Stitching"* **GLSVLSI**
Mahmoud Namazi, Hosein Mohammadi Makrani, Zhi Tian, Setareh Rafatirad, Mohamad Hosein Akbari, Avesta Sasan, **Houman Homayoun**
ACM Great Lakes Symposium on VLSI. (GLSVLSI 2019).

(105) *"Threats on Logic Locking: A Decade Later"* **GLSVLSI**
Kimia Zamiri Azar, Hadi Mardani Kamali, **Houman Homayoun**, Avesta Sasan
ACM Great Lakes Symposium on VLSI. (GLSVLSI 2019).

(104) *"On Custom LUT-based Obfuscation"* **GLSVLSI**

Gaurav Kolhe, Sai Manoj P. D., Setareh Rafatirad, Hamid Mahmoodi, Avesta Sasan, **Houman Homayoun**
ACM Great Lakes Symposium on VLSI. (GLSVLSI 2019).

(103) *"ECoST: Energy-Efficient Co-Locating and Self-Tuning MapReduce Applications"* **ICPP**
Maria Malik, Hassan Ghasemzadeh, Tinoosh Mohsenin, Rosario Cammarota, Liang Zhao, Avesta Sasan, **Houman Homayoun**, Setareh Rafatirad
48th International Conference on Parallel Processing. (ICPP 2019).

(102) *"COMA: Communication and Obfuscation Management Architecture"* **RAID**
Kimia Zamiri Azar, Farnoud Farahmand, Hadi Mardani Kamali, Shervin Roshanisefat, **Houman Homayoun**, William Diehl, Kris Gaj, Avesta Sasan
22nd International Symposium on Research in Attacks, Intrusions and Defenses. (RAID 2019).

(101) *"Adversarial Attack on Microarchitectural Events based Malware Detectors"* **DAC**
Abhijit Dhalve, Sairaj Kiran Amberkar, Sahil Bhat, Hossein Sayadi, Nisarg Patel, Sai Manoj P. D., Avesta Sasan, Setareh Rafatirad, **Houman Homayoun**
ACM/IEEE 56th Design Automation Conference. (DAC 2019).

(100) *"Full-Lock: Hard Distributions of SAT instances for Obfuscating Circuits using Fully Configurable Logic Blocks"* **DAC**
Hadi Mardahi, **Houman Homayoun,** Avesta Sasan
ACM/IEEE 56th Design Automation Conference. (DAC 2019).

(99) *"On the Complexity Reduction of Dense Layers from O(N^2) to O(N logN) with Cyclic Sparsely Connected Layers"* **DAC**
S. Morteza Hoseini, Mark Horton, Hirenkumar Paneliya, Uttej Kallakuri, **Houman Homamyoun**, Tinoosh Mohsenin
ACM/IEEE 56th Design Automation Conference. (DAC 2019).

(98) *"2SMaRT: A Two-Stage Machine Learning-Based Approach for Run-Time Specialized Hardware-Assisted Malware Detection"* **DATE**
Hossein Sayadi, Hosein Mohammadi Makrani, Sai Manoj Pudukotai Dinakarrao, Tinoosh Mohsenin, Avesta Sasan, Setareh Rafatirad and **Houman Homayoun**
Design, Automation & Test in Europe, (DATE 2019)

(97) *"Lightweight Node-level Malware Detection and Network-level Malware Confinement in IoT Networks"* **DATE**
Sai Manoj Pudukotai Dinakarrao, Hossein Sayadi, Hosein Mohammadi Makrani, Cameron Nowzari, Setareh Rafatirad and **Houman Homayoun**
Design, Automation & Test in Europe, (DATE 2019)

(96) *"XPPE: a cross platform performance estimation of OpenCV kernels on FPGA devices"* **ASPDAC**
Hosein Makrani, Sara Bondi, **Houman Homayoun (Invited Talk)**
24th Asia and South Pacific Design Automation Conference, (ASPDAC 2019)

(95) *"IR-ATA: IR Annotated Timing Analysis, A Flow for Closing the Loop Between PDN design, IR Analysis & Timing Closure"* **ASPDAC**
Ashkan Vakil, **Houman Homayoun,** Avesta Sasan
24th Asia and South Pacific Design Automation Conference, (ASPDAC 2019)

(94) *"Exploiting Energy-Accuracy Trade-off through Contextual Awareness in Multi-Stage Convolutional Neural Networks"* **ISQED**
Katayoun Neshatpour, **Houman Homayoun** , Avesta Sasan **(Invited Talk)**
20th International Symposium on Quality of Electronic Design, (ISQED 2019)

2018

(93) *"Ensemble Learning for Hardware-Based Malware Detection: A Comprehensive Analysis and Classification"* **DAC**
Hossein Sayadi, Nisarg Patel, Sai Manoj P. D., Avesta Sasan, Setareh Rafatirad, **Houman Homayoun**

ACM/IEEE 55th Design Automation Conference. (DAC 2018).

(92) *"ICNN: An Iterative Implementation of Convolutional Neural Networks to Enable Energy and Computational Complexity Aware Dynamic Approximation"* **DATE**
Katayoun Neshatpour, Farnaz Behnia, **Houman Homayoun**, Avesta Sasan
Design, Automation & Test in Europe, (DATE 2018).

(91) *"Efficient Utilization of Adversarial Training towards Robust Machine Learners and its Analysis".* **ICCAD**
Sai Manoj P D, Sairaj Amberkar, Setareh Rafatirad, **Houman Homayoun**.
IEEE/ACM International Conference on Computer Aided Design, Special Session (ICCAD 2018).

(90) *"Hardware-Assisted Security: Understanding Security Vulnerabilities, Emerging Attacks and Existing Defenses"* **CASES**
Sai Manoj Pudukotai Dinakarrao, Ferdinand Brasser, Lucas Davi, Abhijitt Dhavlle, Tommaso Frassetto, Setareh Rafatirad, Ahmad-Reza Sadeghi, Hossein Sayadi, and Shaza Zeitouni, **Houman Homayoun**
In Proceedings of the 2018 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, (CASES 2018).

(89) "*Power Conversion Efficiency-Aware Mapping of Multithreaded Applications on Heterogeneous Architectures: A Comprehensive Parameter Tuning*" **ASPDAC**
Hossein Sayadi, Divya Pathak, Ioannis Savidis, **Houman Homayoun**
23rd Asia and South Pacific Design Automation Conference, (ASPDAC 2018)

(88) "Design Space Exploration for Acceleration of Machine Learning Applications". **FCCM**
Katayoun Neshatpour, **Houman Homayoun**.
The 26th IEEE International Symposium on Field-Programmable Custom Computing Machines, (FCCM 2018).

(87) "Main-Memory Requirements of Big Data Applications on Commodity Server Platform". **CCGRID**
Hosein Mohammadi Makrani, Setareh Rafatirad and **Houman Homayoun**.
18th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing, (CCGRID 2018).

(86) *"Energy-aware and Machine Learning-based Resource Provisioning of In-Memory Analytics on Cloud".* **SOCC**
Hosein Mohammadi Makrani, Hossein Sayadi, Devang Motwani, Han Wang, Setareh Rafatirad, **Houman Homayoun.**
ACM Symposium on Cloud Computing 2018 (SoCC 2018)

(85) *"A Scalable and Low Power DCNN for Multimodal Data Classification"* **RECONFIG**
Ali Jafari, Morteza Hosseini, **Houman Homayoun** and Tinoosh Mohsenin
IEEE International Conference on Reconfigurable Computing and FPGAs, (Reconfig 2018)

(84) "Comprehensive Assessment of Run-Time Hardware-Supported Malware Detection Using General and Ensemble Learning". **CF**
Hossein Sayadi, Sai Manoj, Setareh Rafatirad, **Houman Homayoun**.
ACM International Conference on Computing Frontiers (CF 2018).

(83) *"Understanding and Benchmarking the Capabilitiesand Limitations of SAT Solvers in DefeatingObfuscation Schemes"* **IOLTS**
Shervin Roshanisefat, Harshith Thirumala, **Houman Homayoun**, Kris Gaj, Avesta Sasan
24th IEEE International Symposium on On-Line Testing and Robust System Design. (IOLTS 2018)

(82) *"Architectural Considerations for FPGA Acceleration of Machine Learning Applications in MapReduce".* **SAMOS**
Katayoun Neshatpour,Hosein Mohammadi Mokrani, Avesta Sasan, Hassan Ghasemzadeh, Setareh Rafatirad, **Houman Homayoun**.
International Symposium on Systems, Systems, Architectures, Modeling and Simulation. *SAMOS XVIII 2018*, Samos, Greece.

(81) *"A comprehensive Memory Analysis of Data Intensive Workloads on Server Class Architecture".* **MEMSYS**
Hosein Mohammadi Makrani, Hossein Sayadi, Sai Manoj Pudukotai Dinakarra, Setareh Rafatirad,

Houman Homayoun.
The International Symposium on Memory Systems (MEMSYS 2018).

(80) *"Compressive Sensing on Storage Data: An Effective Solution to Alleviate I/O Bottleneck in Data Intensive Workloads"*. **ASAP**
Hosein Mohammadi Makrani, Hossein Sayadi, Sai Manoj Pudukotai Dinakarrao, Setareh Rafatirad, **Houman Homayoun**.
The 29th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2018)

(79) *"LUT-Lock: A Novel LUT-based Logic Obfuscation for FPGA-Bitstream and ASIC-Hardware Protection"*. **ISVLSI**
Hadi Mardani Kamali, Kimia Zamiri Azar, Kris Gaj, **Houman Homayoun,** Avesta Sasan.
IEEE Computer Society Annual Symposium on VLSI, (ISVLSI 2018).

(78) *"Customized Machine Learning-Based Hardware-Assisted Malware Detection in Embedded Devices"*. **TRUSTCOM**
Hossein Sayadi, Hosein Mohammadi Makrani, Onkar Randive, Sai Manoj Pudukotai Dinakarrao, Setareh Rafatirad, **Houman Homayoun**.
17th IEEE International Conference On Trust, Security And Privacy In Computing And Communications (TrustCom).

2017

(77) *"MeNa: A Memory Navigator for Modern Hardware in Scale-out Environment"* **IISWC**
Hosein Makrani, **Houman Homayoun**
2017 IEEE International Symposium on Workload Characterization, (IISWC 2017).

(76) *"Co-Locating and Concurrent Fine-Tuning MapReduce Applications on Microservers for Energy Efficiency"* **IISWC**
Maria Malik, Dean Tullsen, **Houman Homayoun**
2017 IEEE International Symposium on Workload Characterization, (IISWC 2017).

(75) *"Memory Requirements of Hadoop, Spark, and MPI Based Big Data Applications on Commodity Server Class Architecture"* **IISWC**
Hosein Makrani, **Houman Homayoun**
2017 IEEE International Symposium on Workload Characterization, (IISWC 2017).

(74) *"Analyzing Hardware Based Malware Detectors"* **DAC**
Nisarg Patel and **Houman Homayoun**
ACM/IEEE 54th Design Automation Conference. (DAC 2017).

(73) "*Big vs Little Core for Energy-Efficient Hadoop Computing*" **DATE**
Maria Malik, Katayoun Neshatpour, Tinoosh Mohsenin, Avesta Sasan and **Houman Homayoun**
Design, Automation & Test in Europe, (DATE 2017).

(72) "*LESS: Big Data Sketching and Encryption on Low Power Platform*" **DATE**
Amey Kulkarni, Colin Shea, **Houman Homayoun** and Tinoosh Mohsenin
Design, Automation & Test in Europe, (DATE 2017).

(71) *"Spatial and Temporal Scheduling of Clock Arrival Times for IR Hot-Spot Mitigation, Reformulation of Peak Current Reduction"* **ISLPED**
Bhoopal Gunna, Lakshmi Bhamidipati, **Houman Homayoun** and Avesta Sasan
ACM/IEEE International Symposium on Low Power Electronics and Design, (ISLPED 2017).

(70) *"A Power Delivery Network and Cell Placement Aware IR-Drop Mitigation Technique: Harvesting Unused Timing Slacks to Schedule Useful Skews"* **ISVLSI**
Lakshmi Bhamidipati, Bhoopal Gunna, **Houman Homayoun**, Avesta Sasan
IEEE Computer Society Annual Symposium on VLSI, (ISVLSI 2017).

(69) "Machine Learning-based Approaches for Energy Efficiency Prediction and Scheduling in Composite Cores Architectures" **ICCD**
Hossein Sayadi, Avesta Sasan, **Houman Homayoun**

IEEE International Conference on Computer Design (ICCD 2017).

(68) "Understanding the Role of Memory Subsystem on Performance and Energy-Efficiency of Hadoop Applications" (**Invited Talk**) **IGSC**
Hosein Makrani, Shahab Tabatabaei, Setareh Rafatirad and **Houman Homayoun**
The Eighth International Green and Sustainable Computing Conference, (IGSC 2017).

(67) "Scheduling Multithreaded Applications onto Heterogeneous Composite Cores Architectures" **IGSC**
Hossein Sayadi, **Houman Homayoun**
The Eighth International Green and Sustainable Computing Conference, (IGSC 2017).

(66) *"Work Load Scheduling For Multi Core Systems With Under-Provisioned Power Delivery"* **GLSVLSI**
Divya Pathak, **Houman Homayoun**, Ioannis Savidis
27th ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI 2017).

2016

(65) "*Big Data Analytics on Heterogeneous Accelerator Architectures*" (**Invited Talk**) **CODES+ISSS**
Katayoun Neshatpour, Avesta Sasan, **Houman Homayoun**
IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis, (CODES+ISSS) 2016.

(64) "*Dynamic Single and Dual Rail Spin Transfer Torque Look Up Tables with Enhanced Robustness under CMOS and MTJ Process Variations*" **ICCD**
Aliyar Attaran, Hassan Salmani, **Houman Homayoun** and Hamid Mahmoodi
IEEE International Conference on Computer Design (ICCD), 2016.

(63) "*Hybrid STT-CMOS Designs for Reverse-Engineering Prevention*" **DAC**
Ted Winograd, Hassan Salmani, Hamid Mahmoodi, Kris Gaj, **Houman Homayoun**
ACM/IEEE 53rd Design Automation Conference. (DAC 2016).

(62) "*Characterizing Hadoop Applications on Microservers for Performance and Energy Efficiency Optimizations*" **ISPASS**
Maria Malik, Setareh Rafatirad, Rajiv Joshi, **Houman Homayoun**
IEEE International Symposium on Performance Analysis of Systems and Software, (ISPASS) 2016.

(61) "*Comparative Analysis of Hybrid Magnetic Tunnel Junction and CMOS Logic Circuits*". **SOCC**
Darya Almasi, **Houman Homayoun**, Hassan Salmani, Hamid Mahmoodi
29th IEEE International System-on-Chip Conference (SOCC), 2016.

(60) "*Heterogeneous Chip Multiprocessor Architectures for Big Data Applications*". (**Invited Talk**) **CF**
Houman Homayoun
ACM International Conference on Computing Frontiers (CF) 2016.

(59) "*Low-Power ManyCore Accelerator for Personalized Biomedical Applications*"**(Best Paper Award)** **GLSVLSI**
Adam Page, Nasrin Attaran, Colin Shea, **Houman Homayoun,** Tinoosh Mohsenin
ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI) 2016.

(58) "*Architecture Exploration for Energy-Efficient Embedded Vision Applications: From General Purpose Processor to Domain Specific Accelerator*". **ISVLSI**
Maria Malik, Farnoud Farahmand, Paul Otto, Nima Akhlaghi, Tinoosh Mohsenin, Siddhartha Sikdar, **Houman Homayoun**.
IEEE Computer Society Annual Symposium on VLSI, (ISVLSI 2016).

(57) "*Load Balanced On-Chip Power Delivery for Average Current Demand*" **GLSVLSI**
Divya Pathak, Mohammad Hajkazemi, Mohammad Tavana, Houman Homayoun and Ioannis Savidis
ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI) 2016.

(56) "*Reliability Analysis of Spin Transfer Torque Based Look Up Tables Under Process Variations*" **ISCAS**
Ragh Kuttappa, Hassan Salmani, Hamid Mahmoodi, **Houman Homayoun**
IEEE International Symposium on Circuits and Systems, (ISCAS) 2016.

(55) "*Energy Efficient On-Chip Power Delivery with Run-Time Voltage Regulator Clustering*" **ISCAS**
Divya Pathak, Mohammad Khavari Tavana, Mohammad Hossein Hajkazemi, **Houman Homayoun**

and Ioannis Savidis
IEEE International Symposium on Circuits and Systems, (ISCAS) 2016.

(54) "*Big Biomedical Image Processing Hardware Acceleration: A Case Study for K-means and Image Filtering* ". **(Invited Special Session Talk)** **ISCAS**
Katayoun Neshatpour, Arezou Koohi, Maria Malik, Setareh Rafatirad, Avesta Sasan, **Houman Homayoun**
IEEE International Symposium on Circuits and Systems, (ISCAS) 2016.

(53) "*Preventing Design Reverse Engineering with Reconfigurable Spin Transfer Torque LUT Gates*". **ISQED**
Ted Winograd, Hasan Salmani, Hamid Mahmoodi, **Houman Homayoun**
17th International Symposium on Quality of Electronic Design, (ISQED) 2016.

(52) "*Co-Clustering Of Diseases, Genes, And Drugs For Identification Of Their Related Gene Modules*". **ICACI**
Arezou Koohi, **Houman Homayoun**, Jie Xu, Mahdi Orooji
Eighth International Conference on Advanced Computational Intelligence, (ICACI 2016).

2015

(51) "*System and Architecture Level Characterization of Big Data Applications on Big and Little Core Server Architectures*". **BIGDATA**
Maria Malik, Setareh Rafatirad, **Houman Homayoun**
IEEE BigData Conference 2015.

(50) "*Energy-Efficient Acceleration of Big Data Analytics Applications Using FPGAs*". **BIGDATA**
Katayoun Neshatpour, Maria Malik, Mohammad Ali Ghodrat, Avesta Sasan, **Houman Homayoun**.
IEEE BigData Conference 2015.

(49) "*Wide I/O or LPDDR? Exploration and Analysis of Performance, Power and Temperature Trade-offs of Emerging DRAM Technologies in Embedded MPSoCs*". **ICCD**
Mohammad Hossein Hajkazemi, Mohammad Khavari Tavana and **Houman Homayoun**
IEEE International Conference on Computer Design (ICCD), 2015.

(48) "*Big Data on Low Power Cores Are Low Power Embedded Processors a Good Fit for the Big Data Workloads?*". **ICCD**
Maria Malik and **Houman Homayoun**
IEEE International Conference on Computer Design (ICCD), 2015.

(47) "*Realizing Complexity-Effective On-Chip Power Delivery for Many-Core Platforms by Exploiting Optimized Mapping*". **ICCD**
Mohammad Khavari Tavana, Divya Pathak, Mohammad Hossein Hajkazemi, Maria Malik, Ioannis Savidis and **Houman Homayoun**
IEEE International Conference on Computer Design (ICCD), 2015.

(46) "*Power and Performance Characterization, Analysis and Tuning for Energy-efficient Edge Detection on Atom and ARM Based Platforms*". **ICCD**
Paul Otto, Maria Malik, Nima Akhlaghi, Rebel Sequeira, **Houman Homayoun** and Siddhartha Sikdar
IEEE International Conference on Computer Design (ICCD), 2015.

(45) "*Accelerating Big Data Analytics Using FPGAs*". **FCCM**
Katayoun Neshatpour, Maria Malik, Mohammad Ali Ghodrat, **Houman Homayoun**.
The 23rd IEEE International Symposium on Field-Programmable Custom Computing Machines, (FCCM 2015).

(44) "*ElasticCore: Enabling Dynamic Heterogeneity with Joint Core and Voltage/Frequency Scaling*". **DAC**
Mohammad Khavari Tavana, Mohammad Hajkazemi, Divya Pathak, Ioannis Savidis, **Houman Homayoun**
ACM/IEEE 52TH Design Automation Conference. (DAC 2015).

(43) "*Just-in-time component-wise power and thermal modeling*" **CF**
Shah Mohammad Faizur Rahman, Qing Yi, **Houman Homayoun**
2015 ACM International Conference on Computing Frontiers, (CF 2015).

(42) "*Accelerating Machine Learning Kernels in Hadoop Using FPGAs*". **CCGRID**
Katayoun Neshatpour, Maria Malik, Mohammad Ali Ghodrat, **Houman Homayoun**
15th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing, 2015.

(41) "*Adaptive Bandwidth Management for Performance-Temperature Trade-offs in Heterogeneous HMC+DDRx Memory*". **GLSVLSI**
Mohammad Hossein Hajkazemi, Michael Chorney, Reyhaneh Jabbarvand Behrouz, Mohammad Khavari Tavana and **Houman Homayoun**.
25th ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI 2015).

(40) "*Revisiting Dynamic Thermal Management Exploiting Inverse Thermal Dependence*". **GLSVLSI**
Katayoun Neshatpour, Amin Khajeh-Djahromi, Wayne Burleson, **Houman Homayoun**.
25th ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI 2015).

2014

(39) "*Energy-efficient mapping of biomedical applications on domain-specific accelerator under process variation*". **ISLPED**
Mohammad Khavari Tavana, Amey M. Kulkarni, Abbas Rahimi, Tinoosh Mohsenin, **Houman Homayoun**.
ACM/IEEE International Symposium on Low Power Electronics and Design, (ISLPED 2014).

(38) "*Exploiting STT-NV Technology for Reconfigurable, High Performance, Low Power, and Low Temperature Functional Unit Design*". **DATE**
Adarsh Reddy Ashammagari, Hamid Mahmoodi, **Houman Homayoun**.
Design, Automation & Test in Europe, (DATE 2014).

(37) "*Enabling Dynamic Heterogeneity Through Core on Core Stacking*". **(Special Session Talk)** **DAC**
Dean Tullsen, **Houman Homayoun**.
ACM/IEEE 51TH Design Automation Conference. (DAC 2014).

(36) "*Modeling and Analysis of Phase Change Materials for Efficient Thermal Management*". **ICCD**
Fulya Kaplan, Charlie De Vivero, Samuel Howes, Manish Arora, **Houman Homayoun**, Wayne Burleson, Dean Tullsen, Ayse Coskun.
International Conference on Computer Design (ICCD 2014).

(35) "*A Parallel and Reconfigurable Architecture for Efficient OMP Compressive Sensing Reconstruction*". **GLSVLSI**
Amey Kulkarni, **Houman Homayoun** and Tinoosh Mohsenin.
24th ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI 2014).

(34) "*Reconfigurable STT-NV LUT-based Functional Units to Improve Performance in General-Purpose Processors*". **GLSVLSI**
Adarsh Reddy, Ashammagari, Hamid Mahmoodi, Tinoosh Mohsenin, Houman Homayoun.
24th ACM International Conference of the Great Lakes Symposium on VLSI, (GLSVLSI 2014).

(33) "*NVP: Non-uniform Voltage and Pulse width Settings for Power Efficient Hybrid STT-RAM*". **IGCC**
Reyhaneh Jabbarvand Behrouz, **Houman Homayoun**.
International Green Computing Conference, (IGCC 2014).

2013

(32) "*VAWOM: Temperature and Process Variation Aware WearOut Management in 3D Multicore Architectures*" **DAC**
Hossein Tajik, **Houman Homayoun**, Nikil Dutt
ACM/IEEE 50TH Design Automation Conference, (DAC 2013).

(31) "*Low-Current Probabilistic Writes for Power-Efficient MRAM Caches*". **ICCD**
Nikolaos Strikos, Vasileios Strikos, Xiangyu Dong, **Houman Homayoun**, Dean Tullsen.
International Conference on Computer Design (ICCD), 2013.

(30) "*REMEDIATE: A Scalable Fault-tolerant Architecture for Low-Power NUCA Cache in Tiled CMPs*". **IGCC**
Abbas Banaiyanmofrad, **Houman Homayoun**, Nikil Dutt.

International Green Computing Conference. (IGCC 2013).

(29) *"Heterogeneous Memory Management for 3D-DRAM and External DRAM with QoS"* **ASPDAC**
Le-Nguyen Tran, **Houman Homayoun**, Fadi Kurdahi, Ahmed Eltawil.
18th Asia and South Pacific Design Automation Conference (ASP-DAC 2013).

(28) *"Temperature Aware Thread Migration in 3D Architecture with Stacked DRAM"* **ISQED**
Dali Zhao, **Houman Homayoun**, Alex Veidenbaum.
International Symposium on Quality of Electronic Design (ISQED) 2012.

(27) *" A Many-core Platform for Biomedical Signal and Image Processing"* **ISQED**
Jordan Bisasky, Tinoosh Mohsenin and **Houman Homayoun**.
International Symposium on Quality of Electronic Design (ISQED) 2012.

2012

(26) *"Managing Distributed UPS Energy for Effective Power Capping in Data Centers"* **ISCA**
Vasileios Kontorinis, Baris Aksanli, **Houman Homayoun**, John Sampson, Tajana S. Rosing, and Dean M. Tullsen.
International Symposium on Computer Architecture, ISCA 2012. Portland, Oregon.

(25) *"Dynamically Heterogeneous Cores Through 3D Resource Pooling"* **HPCA**
Houman Homayoun, Vasileios Kontorinis, Ta-Wei Lin, Amirali Shayan and Dean M. Tullsen.
International Symposium on High-Performance Computer Architecture, HPCA 2012. New Orleans, Louisiana.

(24) *"Hot Peripheral Thermal Management to Mitigate Cache Temperature Variation"* **ISQED**
Houman Homayoun, Mehryar Rahmatian, Vasileios Kontorinis, Shahin Golshan, Dean Tullsen.
13th International Symposium on Quality of Electronic Design (ISQED) 2012.

(23) *"History & Variation Trained Cache (HVT-Cache):A Process Variation Aware and Fine Grain voltage Scalable Cache with Active Access History Monitoring"* **ISQED**
Avesta Sasan, **Houman Homayoun**, Kiarash Amiri, Ahmed Eltawil and Fadi Kurdahi.
13th International Symposium on Quality of Electronic Design (ISQED) 2012.

2011

(22) *"FFT-Cache: A Flexible Fault-Tolerant Cache Architecture for Ultra Low Voltage Operation"* **CASES**
Abbas Banaiyan, **Houman Homayoun** and Nikil Dutt.
In Proceedings of the 2011 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, CASES 2011. Taipei, Taiwan.

(21) *"Reliability-Aware Placement in SRAM-based FPGA for Voltage Scaling Realization in the Presence of Process Variations"* **CODES**
Shahin Golshan, Amin Khajeh, **Houman Homayoun**, Eli Bozorgzadeh, Ahmed Eltaweel and Fadi Kurdahi.
In Proceedings of the 9th International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2011. Taipei, Taiwan.

2010

(20) *"RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor*". **HIPEAC**
Houman Homayoun, Aseem Gupta, Alex Veidenbaum, Fadi J. Kurdahi, Nikil Dutt.
5th International Conference of High Performance Embedded Architectures and Compilers, HiPEAC-2010. Italy.

(19) *"Post-Synthesis Sleep Transistor Insertion for Leakage Power Optimization in Clock Tree Networks*". **ISQED**
Houman Homayoun, Shahin Golshan, Eli Bozorgzadeh, Fadi Kurdahi, Alex Veidenbaum.
11th IEEE International Symposium on Quality Electronic Design, *ISQED-2010*. San Jose, California.

(18) *"Multiple Sleep Modes Leakage Control In Peripheral Circuits Of A All Major SRAM-Based* **CF**

Processor Units".
Houman Homayoun, Avesta Sasan, Aseem Gupta, Alex Veidenbaum, Fadi Kurdahi, Nikil Dutt.
2010 ACM International Conference on Computing Frontiers, *CF-2010*. Bertinoro, Italy.

(17) *"Exploiting Power Budgeting in Thermal-Aware Dynamic Placement for Reconfigurable Systems"* **ISLPED**
Shahin Golshan, Kazutoshi Wakabayashi, Benjamin Carrión Schäfer, **Houman Homayoun**, Elaheh Bozorgzadeh.
ACM/IEEE International Symposium on Low Power Electronics and Design, *ISLPED 2010*.

(16) *"E < MC^2 : Less Energy through Multi-Copy Cache"*. **CASES**
Arup Chakraborty, **Houman Homayoun**, Amin Khejah, Nikil Dutt, Ahmed Eltawil, Fadi Kurdahi.
In Proceedings of the 2010 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, *CASES 2010*. Scottsdale, Arizona.

2009

(15) *"Process Variation Aware Cache for Aggressive Voltage-Frequency Scaling*". **DATE**
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
Design, Automation & Test in Europe, *DATE 2009*, Nice, France.

(14) *"A Fault Tolerant Cache Architecture for Sub 500mV Operation: Resizable Data Composer Cache (RDC-Cache)*". **CASES**
Avesta Makhzan, **Houman Homayoun**, Ahmed Eltawil, Fadi J. Kurdahi.
In Proceedings of the 2009 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, *CASES 2009*. Grenoble, France.

2008

(13) *"Dynamic Register File Resizing and Frequency Scaling to Improve Embedded Processor Performance and Energy-Delay Efficiency".* **DAC**
Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum.
ACM/IEEE 45TH Design Automation Conference, *DAC 2008*. Anaheim, U.S.A.

(12) *"Multiple Sleep Mode Leakage Control for Cache Peripheral Circuits in Embedded Processors".* **CASES**
Houman Homayoun, Mohammad Makhzan and Alex Veidenbaum.
In Proceedings of the 2008 International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, *CASES 2008*. Atlanta, U.S.A.

(11) *"Adaptive Techniques for Leakage Power Management in L2 Cache Peripheral Circuits".* **ICCD**
Houman Homayoun, Alex Veidenbaum and Jean-Luc Gaudiot.
In Proceedings of XXVI IEEE International Conference on Computer Design, *ICCD 2008*. Lake Tahoe, U.S.A.

(10) *"Improving Performance and Reducing Energy-Delay with Adaptive Resource Resizing for Out-Of-Order Embedded Processors".* **LCTES**
Houman Homayoun, Sudeep Pasricha, Mohammad A. Makhzan, Alexander V. Veidenbaum.
ACM SIGPLAN/SIGBED 2008 Conference on Languages, Compilers, and Tools for Embedded Systems, *LCTES 2008.*

(9) *"ZZ-HVS: Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On-Chip SRAM Peripheral Circuits".* **ICCD**
Houman Homayoun, Mohammad Makhzan and Alex Veidenbaum.
In Proceedings of XXVI IEEE International Conference on Computer Design, *ICCD 2008*. Lake Tahoe, U.S.A.

(8) *"A Centralized Cache Miss Driven Technique to Improve Processor Power Dissipation".* **SAMOS**
Houman Homayoun, Mohammad Makhzan, Jean-Luc Gaudiot, and Alex Veidenbaum.
International Symposium on Systems, Systems, Architectures, Modeling and Simulation. *SAMOS VIII 2008*, Samos, Greece.

2007

(7) *"Reducing Leakage Power in Peripheral Circuit of L2 Caches".* **ICCD**

Houman Homayoun and Alexander V. Veidenbaum.
In Proceedings of IEEE International Conference on Computer Design, *ICCD 2007*. Lake Tahoe, U.S.A.

2006

(6) "*Using Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation"*. **ISPASS**
Houman Homayoun and Amirali Baniasadi.
The 2nd workshop on unique chips and systems, in conjunction with IEEE International Symposium on Performance Analysis of Systems and Software, *IEEE-ISPASS 2006*, Austin, U.S.A.

(5) "*Reducing Execution Unit Leakage Power in Embedded Processors*". **SAMOS**
Houman Homayoun and Amirali Baniasadi.
The 6th International Conference on Embedded Computer Systems, *SAMOS VI-2006*. Samos, Greece.

(4) "*Reducing the Instruction Queue Leakage Power in Superscalar Processor*". **CCECE**
Houman Homayoun and Ted H. Szymanski.
The 19th Annual Canadian Conference on Electrical and Computer Engineering, *CCECE-2006*, Ottawa, Canada.

2005

(3) "*Analysis of Functional Unit Power Gating in Embedded Processors*". **VLSISOC**
Houman Homayoun and Amirali Baniasadi.
IFIP International Conference on Very Large Scale Integration System on Chip *IFIP VLSI-SOC 2005*. Perth, Wetsren Australia.

(2) "*Thread Scheduling Based on Low Quality Instruction Prediction for Simultaneous Multithreaded Processors*". **NEWCAS**
Houman Homayoun, Kin F. Li and Setareh Rafatirad.
The 3rd International IEEE NorthEast Workshop on Circuits and Systems, *IEEE-NEWCAS 2005*. Montreal, Canada.

(1) "*Functional Unit Power Gating in Simultaneous Multithreaded Processors*". **PACRIM**
Houman Homayoun, Kin F. Li. and Setareh Rafatirad.
The IEEE Pacific Rim Conference on Communications, Computers and Signal Processing *IEEE-PACRIM 2005*. Victoria, Canada.

PATENT

(1) Vanishable Logic To Enhance Circuit Security, U.S. Patent 10430618, App. 15290871, 2019/10/1, **Houman Homayoun** and Hamid Mahmoodi.
(2) Work Load Scheduling For Multi Core Systems With Under-Provisioned Power Delivery, 2018/11/1, US Patent App. 15968348, Ioannis Savidis, Divya Pathak, **Houman Homayoun**

HONORS/AWARDS

- **Best Paper Award**, 19th IEEE International Conference on Data Mining (ICDM). *2019*
- **Best Paper Award Nominee**, International Conference on Computer Aided Design (ICCAD). *2019*
- **NSF IUCRC Center Award**, Center for HW Security. *2019-2024*
- **General Chair**, IEEE/ACM 29th ACM Great Lakes Symposium on VLSI. *2019*
- **Technical Program Co-Chair**, IEEE/ACM 28th ACM Great Lakes Symposium on VLSI. *2018*
- **"Associate Editor"**, IEEE Transactions on VLSI. *January 2017-January 2019*
- "**Best Paper Award**", 26th ACM Great Lakes Symposium on VLSI, GLSVLSI. *May-2016*
- "**National Science Foundation 2010 CI Fellowship Award**", **280,000**$ (for two years). *September-2010*
  NSF Award 1019343/CRA Sub Award CIF-B-68
  Funded Project: Inter-core Selective Resource Pooling in a 3D Chip Multiprocessor.

- **"ACM Doctoral Dissertation Nominee"**, UC-Irvine School of Information and Computer Science. *September-2010* (2 out of 31 PhD Dissertations were Nominated)
- **"Outstanding Graduate Student Award",** (APSIH-2010) *June-2010*
- "**4-Years Chair Fellowship Award**", University of California Irvine , **160,000**$ *September 2006-September 2010* Computer Science Department.
- **"DAC Student Mentor**" Award, Design Automation Conference (DAC), *June-2010*
- "**First Place**", IEEE Orange County and Western Digital Student Design Contest. *November-2009* 8th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California.
- "**First Place**", IEEE Orange County and Western Digital Student Design Contest. *November-2008* 7th International System-on-Chip Conference, Exhibit & Workshops, Newport Beach, California.
- **"DAC Student Mentor**" Award, Design Automation Conference (DAC), *June-2008*
- "**University Scholarship***"*, McMaster University, Canada. *September 2005-August 2006*
- "**NAHAAL Scholarship***"* for Excellence in Education and Research. *September 2001-August 2002*
- "**National Ranking***"*, Rank 55 among more than 500,000 participants. *September -1998* Iran Nationwide Universities Entrance Exam.

STUDENTS

PhD Students (Current)

1. Hosein Makrani, ECE Department, University of California Davis, Fall 2015-Fall 2020 (expected), Emerging Memory Technologies for Big Data
2. Gaurav Kolhe, ECE Department, University of California Davis, Summer 2018 – Summer 2022 (expected)
3. Han Wang, ECE Department, University of California Davis, Fall 2017-Fall 2021 (expected)
4. Ted Winograd, ECE Department, George Mason University, Fall 2013-Fall 2020 (expected), (co-advise with Kris Gaj), Hybrid CMOS+STT Technology for Hardware Security and Trust
5. Ashkan Vakil, ECE Department, George Mason University, Fall 2016 (co-advised with Avesta Sasan), Fall 2016-Fall 2020 (expected)
6. Farnaz Behniya, ECE Department, George Mason University, Spring 2017 (co-advised with Avesta Sasan), Fall 2016-Fall 2020 (expected)
7. Rakib Hassan, ECE Department, George Mason University, (co-advised with Sai Manoj), Fall 2018-Fall 2022 (expected)
8. Ali Mirzaeian, ECE Department, George Mason University, (co-advised with Avesta Sasan), Fall 2017-Fall 2021 (expected), Accelerating Convolutional Neural Networks

Alumni

PhD

1. Hossein Sayadi, ECE Department, Summer 2019
   Dissertation: Towards Hardware Cybersecurity: Challenges and Solutions
   First job: Assistant Professor (tenure-track), California State University, Long Beach
2. Maria Malik, ECE Department, Fall 2013-Spring 2018, System
   Dissertation: Architectural and Application level analysis of Big Data Applications for Performance and Energy-Efficiency
   First Job: Intel
3. Katayoun Neshatpour, ECE Department, Fall 2013-Summer 2018
   Dissertation: Acceleration of Machine-Learning Algorithms for Big Data Applications
   First Job: Cadence
4. Arezou Koohi, ECE Department, Fall 2013-Fall 2018
   Dissertation: Multi-view Graph Co-clustering and Matrix Completion
   First Job: MITRE

Master (with thesis)

1. Sammy Lin, Summer 2019
   Thesis: Experimental Testbed for FPGA Acceleration of Apache Spark Machine Learning Workloads

Current job:

2. Sara Bondi Ogburn, Spring 2019
   Thesis: Understanding Design Space Exploration of FPGAs for Efficient Accelerated Core Processing
   Current job: Boeing
3. Onkar Mahadev Randive, Master of Science, Summer 2018
   Thesis: Analyzing Hardware Based Malware Detectors Using Machine Learning Techniques
   Current job: USAID
4. Gaurav Kolhe, Master of Science, Summer 2018
   Thesis: Security And Complexity Analysis Of LUT-Based Obfuscation: A Comprehensive Study
   Current job: PhD Student at GMU
5. Devang Motwani, Master of Science, Summer 2018
   Thesis: Comparison of Performance of Big Data Applications in Different Environments
   Current job:
6. Saurabh Satish Deshpande, Master of Science, Summer 2018
   Thesis: Android Development for Housing Analytics
   Current job:
7. Abhimanyu Chopra, Master of Science, Summer 2017
   Thesis: Optimal Allocation of Computation in IoT Network
   Current job: Software Engineer at Machfu Inc.
8. Gaurav Shenoy, Master of Science, Summer 2016
   Thesis: Implementation And Evaluation Of Sat-Based Attacks On Hybrid STT-CMOS Circuits For Reverse Engineering
   Current job: Firmware Engineer at SK Hynix Memory Solutions
9. Matthew Drummond, Master of Science, Summer 2015
   Thesis: Power and Performance Characterization of Splash2 Benchmarks on Heterogeneous Architecture
   Current job: Software Engineer at Boeing
10. Adarsh Reddy Ashammagari, Master of Science, Fall 2013
    Thesis: Dynamic Functional Unit Reconfiguration using STT-RAM based Logic for Improving Performance and Mitigating Temperature Rise in Processor Architecture
    Current job: Software Engineer at Narvar

Postdoc

1. Sai Manoj Pudukotai DinakarRao, September 2017-August 2019
   First job: Assistant Professor (tenure track), George Mason University

Visiting Scholar

1. Professor Cheol Hong Kim, School of Electronics and Computer Engineering at Chonnam National University, South Korea, Visiting GOAL lab at GMU August 2016-August 2017.

Undergraduate Student

1. Osaze Sheer (Undergraduate Research Scholars Program (URSP))
2. Nima Namazi (Undergraduate Research Scholar and Senior Design Project)
3. Tatiana Rodrigez (Undergraduate Research Scholar)
4. David Andritsis (Undergraduate Research Scholar and Senior Design Project)
5. Michael Reyes (Senior Design Project)
6. Marjorie Guillen (Senior Design Project)
7. Chris Hall (Senior Design Project)
8. Henry Pham (Senior Design Project)
9. William Johnson (Senior Design Project)
10. Graham Page (Senior Design Project)
11. Mingyu Kim (Senior Design Project)
12. Shayan Mahmoudi (Senior Design Project)
13. Jimmy Mejia (Senior Design Project)
14. Dong Pham (Senior Design Project)
15. Narek Vanetsyan (Senior Design Project)
16. Ismael Khalique (Senior Design Project)

17. Steven Wu (Senior Design Project)
18. Dai Dinh (Senior Design Project)
19. Alexander Tran (Senior Design Project)
20. Daniel Pham (Senior Design Project)

PhD Committee Member

1. Myeong Lim (Advisor: Jim Jones)
2. Mohamed Elsabagh (Adviosr: Angelos Stavrou)
3. Malik Umar Sharif (Advisor: Kris Gaj)
4. Rabia Shahid (Advisor: Kris Gaj)
5. Ahmad Salman (Advisor: Jens Peter Kaps)
6. Bilal Habib (Advisor: Kris Gaj)
7. Fengwei Zhang (Adviosr: Angelos Stavrou)
8. Mohammad Atiq Haque (Advisor: Hakan Aydin)
9. Nariman Mirzae (Advisor: Sam Malek)
10. Ehsan Kouroshfar (Advisor: Sam Malek)
11. Pouyan Ahmadi (Advisor: Bijan Jabbari)

Senior Design Project

1. True Optical Pointer
   David Stein, Darren Korch, Namhee Kim, Brandon Cary, Dondre Sheridan, Joey Vipperman
2. High Frame Rate Embedded Vision for UAVs with FPGA
   M. Guillen, Ch. Hall, W. Johnson, G. Page, H. Pham, and M. Reyes
3. Compressive Sensing for Biomedical Data Acceleration on Embedded Low-Power FPGAs
   M. Kim and M. Namazi
4. Remote Motion Controller Using Leap
   D. Andritsis, D. Dinh, D. Pham, A. Tran, S. Wu
5. Remote Sensing and Processing with Low Power Bluetooth and ARM Cortex
   Sh. Mahmoudi, J. Mejia, D.H. Pham, N. Vanetsyan, and I. Khalique

TEACHING EXPERIENCE

Average Teaching Rating: 4.31, Average Course Rating: 4.17

- **Instructor**, ECE-590/499 (graduate and Undergraduate-level course), Parallel Computing, Department of Electrical and Computer Engineering, George Mason University *Spring 2019*
  Number of students: 23
- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University *Fall 2018*
  Number of students: 12, Number of responses: 10
  Overall Teaching rating: 4.4, Overall for the course: 4.3/5
- **Instructor**, ECE-611 (graduate-level course), Advanced Microprocessors, Department of Electrical and Computer Engineering, George Mason University *Spring 2018*
  Number of students: 17, Number of responses: 12
  Overall Teaching rating: 3.92/5, Overall for the course: 3.83/5
- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University *Fall 2017*
  Number of students: 19, Number of responses: 18
  Overall Teaching rating: 4.1, Overall for the course: 4.00/5
- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University *Fall 2016*
  Number of students: 23, Number of responses: 22
  Overall Teaching rating: 4.73/5, Overall for the course: 4.65/5

- **Instructor**, ECE-445 (Undergraduate-level course), Computer Organization, Department of Electrical and Computer Engineering, George Mason University *Fall 2016*
  Number of students: 57, Number of responses: 29
  Overall Teaching rating: 3.34/5, Overall for the course: 3.36/5
- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University *Fall 2015*
  Number of students: 13, Number of responses: 13
  Overall Teaching rating: 4.31/5, Overall for the course: 4.38/5
- **Instructor**, ECE-699 (graduate-level course), Heterogeneous and Green Computing, Department of Electrical and Computer Engineering, George Mason University *Spring 2015*
  Number of students: 9, Number of responses: 9
  Overall Teaching rating: 4.5/5, Overall for the course: 4.38/5
- **Instructor**, ECE-611 (graduate-level course), Advanced Microprocessors, Department of Electrical and Computer Engineering, George Mason University *Spring 2015*
  Number of students: 16, Number of responses: 12
  Overall Teaching rating: 4.08/5, Overall for the course: 3.92/5
- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University *Fall 2014*
  Number of students: 23, Number of responses: 19
  Overall Teaching rating: 4.84/5, Overall for the course: 4.58/5
- **Instructor**, ECE-611 (graduate-level course), Advanced Microprocessors, Department of Electrical and Computer Engineering, George Mason University *Spring 2014*
  Number of students: 26, Number of responses: 20
  Overall Teaching rating: 4.55/5, Overall for the course: 4.24/5
- **Instructor**, ECE-681 (graduate-level course), VLSI Design for ASICs, Department of Electrical and Computer Engineering, George Mason University *Fall 2013*
  Number of students: 13, Number of responses: 11
  Overall Teaching rating: 4.09/5, Overall for the course: 3.92/5
- **Instructor**, ECE-611 (graduate-level course), Advanced Microprocessors, Department of Electrical and Computer Engineering, George Mason University *Spring 2013*
  Number of students: 11, Number of responses: 11
  Overall Teaching rating: 4.18/5, Overall for the course: 4.00/5
- **Instructor**, ECE-641 (graduate-level course), Computer System Architecture, Department of Electrical and Computer Engineering, George Mason University *Fall 2012*
  Number of students: 15, Number of responses: 14
  Overall Teaching rating: 4.50/5, Overall for the course: 4.36/5
- **Group Leader Teaching Assistant**, leadership, management, and manufacturing engineering, University of California, Irvine, The Paul Merage School of Business *Fall 2010*
- **Teaching Assistant,** Fundamental Data Structures *Summer 2010*
  University of California Irvine, Computer Science Department.
- **Teaching Assistant**, Logic Design Lab *Spring 2010*
  University of California Irvine, Computer Science Department.
- **Teaching Assistant**, Senior Design Project *Fall 2009*
  University of California Irvine, Computer Science Department.
- **Teaching Assistant,** Introduction to Computer Design *Fall 2007*
  University of California Irvine, Computer Science Department.
- **Laboratory and Tutorial Instructor**, Advanced Internet Communications *Spring 2006*
  McMaster University, Electrical and Computer Engineering Department.

- **Laboratory instructor**, General Physics *Fall 2004*
  University of Victoria, Physics Department**.**
- **Laboratory and Tutorial instructor**, Linear Circuit I *Summer 2004*
  University of Victoria, Electrical and Computer Engineering Department.
- **Laboratory instructor**, Electronic Circuit I *Spring 2004*
  University of Victoria, Electrical and Computer Engineering Department.
- **Laboratory instructor**, Microprocessor Systems *Fall 2003*
  University of Victoria, Electrical and Computer Engineering Department.
- **Tutorial instructor**, Digital Circuit Design *Summer 2002*
  Sharif University of Technology, Electrical and Computer Engineering Department.

PRESENTATIONS/INVITED TALKS/TUTORIALS

✓ *Towards Hardware Cybersecurity*	***August-2019*** ***Technical University of Crete***
✓ *Towards Hardware Cybersecurity*	***April-2019*** ***UC-Davis***
✓ *Towards Hardware Cybersecurity*	***March-2019*** ***Virginia Tech***
✓ *Towards Hardware Cybersecurity*	***Nov-2018*** ***UC Santa Barbara***
✓ *Towards Hardware Cybersecurity*	***April 2018*** ***Johns Hopkins University***
✓ *Towards Hardware Cybersecurity*	***March-2018*** ***UC Irvine***
✓ *Design Space Exploration of Server Architecture for Big Data Applications*	***May 2017*** ***Masdar University***
✓ *Energy-Efficient Acceleration of Big Data Applications on Heterogeneous Architectures*	***May-2016*** ***Karlsruhe Institute of Technology***
✓ *Big Data on Heterogeneous Architectures*	***May-2016*** ***TU Dresden***
✓ *Heterogeneous Chip Multiprocessor Architectures for Big Data Applications*	***May-2016*** ***Politecnico di Milano***
✓ *Dynamic Heterogeneous Architectures in 3D*	***April-2015*** ***University of Victoria***
✓ *Heterogeneous Architectures in 3D for Next Generation Big Data Server Platform*	***Nov-2014*** ***IBM-GMU Big Data Symposium***
✓ *Big Data Applications Benchmarking and Characterization*	***Sep-2014*** ***IBM TJ Watson***
✓ *A Uniform Approach to Heterogeneity? Architectures, Tools, and Workloads for Heterogeneous Computing* ***(Special Session)***	***June-2014*** ***DAC Conference***
✓ *Dynamic Heterogeneous Architectures to Address the Efficiency Crisis* ***(Tutorial)***	***March-2014*** ***DATE***

✓ *Enabling Dynamic Heterogeneity in 3D*	***March-2014*** ***Barcelona Supercomputing Center***
✓ *Heterogeneous Architecture to Address the Efficiency Challenge!* ***(DAC Summer School)***	***June-2013*** ***DAC***
✓ *System-Level Exploration of Power, Performance, and Area for Multicore Architectures* ***(Tutorial)***	***June-2012*** ***DAC***
✓ *Future of Heterogeneous Architectures* ***(Keynote Invited Talk)***	***May-2013*** ***United States Patent Office (USPTO)***
✓ *3D Chip Multiprocessor Design*	***March-2013*** ***Virginia Tech (CESCA)***
✓ *Heterogeneous cores through 3D resource pooling* ***(Invited Interview Talk)***	***Jan-April 2012*** ***University of Wisconsin Madison, University of Central Florida, Arizona State University, University of South Florida, University of Texas San Antonio, George Mason University***
✓ *"Multiple Sleep Modes Leakage Control in Peripheral Circuits of All Major SRAM-Based Processor Units"*	***August-2011*** ***Florida International University***
✓ *"FFT-Cache:A Flexible Fault-Tolerant Cache Architecture for Low Voltage Operation"*	***November-2011*** ***9th SOC Conference***
✓ *"Beyond Memory Cells for Leakage and Temperature Control in SRAM-based Units, the Peripheral Circuits Story"*	***November-2010*** ***Arizona State University***
✓ *"Power Management in High Performance Processors through Dynamic Resource Adaptation and Multiple Sleep Mode Assignments"*	***November 2010*** ***8th SOC Conference***
✓ *"Temperature-Aware SoC Optimization Framework"*	***SRC-2010*** ***Pittsburgh***
✓ *"Architectural and Circuit-Levels Design Techniques for Power and Temperature Optimizations in On-Chip SRAM Memories"*	***April-2010*** ***University of Southern California***
✓ *"Power, Temperature, Reliability and Performance - Aware Optimizations in On-Chip SRAM-based Caches"*	***May-2010*** ***UCSD***
✓ *"RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor".*	***January-2010*** ***HiPEAC***
✓ *"Dynamic Register File Resizing and Frequency Scaling to Improve Embedded Processor Performance and Energy-Delay Efficiency".*	***June-2008*** ***DAC***
✓ *"Multiple Sleep Mode Leakage Control for Cache Peripheral Circuits in Embedded Processors".*	***October-2008*** ***CASES***

- ✓ *"Adaptive Techniques for Leakage Power Management in L2 Cache Peripheral Circuits".* ***October-2008 ICCD***
- ✓ *"Improving Performance and Reducing Energy-Delay with Adaptive Resource Resizing for Out-Of Order Embedded Processors".* ***June-2008 LCTES***
- ✓ *"ZZ-HVS: Zig-Zag Horizontal and Vertical Sleep Transistor Sharing to Reduce Leakage Power in On Chip SRAM Peripheral Circuits".* ***October-2008 ICCD***
- ✓ *"A Centralized Cache Miss Driven Technique to Improve Processor Power Dissipation".* ***July-2008 SAMOS***
- ✓ *"Reducing Leakage Power in Peripheral Circuit of L2 Caches".* ***October-2007 ICCD***
- ✓ *"Lazy Instruction Prediction to Reduce Processor Wakeup Power Dissipation".* ***March-2006 UCAS2-ISPASS***

EXTERNAL SERVICE/CONFERENCE COMMITTEE MEMBER/REVIEWER

- **Steering Committee Member,** ACM Great Lake Symposium on VLSI ***2019-Present***
- **General Chair,** IEEE/ACM 29th Great Lake Symposium on VLSI. ***GLSVLSI-2019***
- **Technical Program Committee Co-Chair,** IEEE/ACM 28th Great Lake Symposium on VLSI. ***GLSVLSI-2018***
- **Associate Editor,** IEEE Transactions on VLSI**.** ***2017-2019***
- **Associate Editor***,* Journal of Low Power Electronics and Applications ***2019***
- **National Science Foundation Panelist**. ***2013, 2014, 2015,2018, 2019***
- **Department of Energy Panelist.** ***2013***
- **Proceeding Chair,** 27th Great Lake Symposium on VLSI. ***GLSVLSI-2017***
- **Publicity Chair**, IEEE International Conference on Big Data. ***IEEE BigData-2016***
- **Publicity Chair**, IEEE Global Communications Conference. ***GLOBECOM-2016***
- **Web Chair**, IEEE International Symposium on Performance Analysis of Systems and Software. ***ISPASS-2016***
- **Web Chair**, IEEE International Symposium on Performance Analysis of Systems and Software. ***ISPASS-2015***
- **TPC Co-Chair for SDM track,** IEEE International Symposium on Quality Electronic Design. ***ISQED 2015***
- **Special Session Organizer**, Is Adversarial Learning a Threat for Machine Learning? Defense Strategies and Design of Better Machine Learners, IEEE/ACM International Conference on Computer-Aided Design ***ICCAD-2018***
- **Special Session Organizer,** Harnessing the Power of Big Data – Computing Technology to Transform Big Data into Insight, the International Conference on Hardware/Software Codesign and System Synthesis. ***CODES+ISSS-2016***
- **Special Session Organizer,** A Uniform Approach to Heterogeneity**,** Design Automation Conference. ***DAC-2014***
- **Conference Session Chair,** DAC, DATE, ICCD, ISLPED, ISQED, GLSVLSI, CODES-ISSS
- **Technical Program Committee**, The International Conference on Hardware/Software Codesign and System Synthesis ***CODES-2020***
- **Technical Program Committee,** Design, Automation & Test in Europe Conference. ***DATE-2020***
- **Technical Program Committee**, IEEE International Symposium on Performance Analysis of Systems and Software. ***ISPASS-2020***
- **Technical Program Committee**, The International Conference on Hardware/Software Codesign and System Synthesis ***CODES-2019***
- **Technical Program Committee,** The 37th IEEE International Conference on Computer Design. ***ICCD-2019***
- **Technical Program Committee,** Design, Automation & Test in Europe Conference. ***DATE-2019***
- **Technical Program Committee**, IEEE International Symposium on Hardware Oriented Security and Trust ***HOST-2018***
- **Technical Program Committee**, The 55st Design Automation Conference. ***DAC-2018***
- **Technical Program Committee**, The International Conference on Hardware/Software Codesign and System Synthesis ***CODES-2018***
- **Technical Program Committee,** IEEE International Parallel & Distributed Processing Symposium. ***IPDPS-2018***
- **Technical Program Committee,** Design, Automation & Test in Europe Conference. ***DATE-2018***

- **Technical Program Committee,** The 35th IEEE International Conference on Computer Design. ***ICCD-2017***
- **Technical Program Committee**, The 8th Green and Sustainable Computing Conference. ***IGSC-2017***
- **Technical Program Committee,** the International Conference on Hardware/Software Codesign and System Synthesis. ***CODES+ISSS-2017***
- **Technical Program Committee**, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems ***CASES-2017***
- **Technical Program Committee**, The 54st Design Automation Conference. ***DAC-2017***
- **Technical Program Committee**, Design, Automation & Test in Europe Conference. ***DATE-2017***
- **Technical Program Committee**, The 2017 ACM International Conference on Computing Frontiers. ***CF-2017***
- **Technical Program Committee**, IEEE International Symposium on Hardware Oriented Security and Trust ***HOST-2017***
- **Technical Program Committee**, Workshop on Attacks and Solutions in Hardware Security. ***ASHES-CCS-2017***
- **Technical Program Committee,** Euromicro Conference on Digital System Design ***DSD-2017***
- **Technical Program Committee**, The 53st Design Automation Conference. ***DAC-2016***
- **Technical Program Committee**, The 34th IEEE International Conference on Computer Design. ***ICCD-2016***
- **Technical Program Committee**, IEEE International Symposium on Performance Analysis of Systems and Software. ***ISPASS-2016***
- **Technical Program Committee**, 24th IEEE International Symposium on Field-Programmable Custom Computing Machines. ***FCCM-2016***
- **Technical Program Committee**, The International Conference on Hardware/Software Codesign and System Synthesis ***CODES+ISSS-2016***
- **Technical Program Committee**, The 26th Great Lake Symposium on VLSI. ***GLSVLSI-2016***
- **Technical Program Committee**, The 7th Green and Sustainable Computing Conference. ***IGSC-2016***
- **Technical Program Committee**, The 33nd IEEE International Conference on Computer Design. ***ICCD-2015***
- **Technical Program Committee**, The 25th Great Lake Symposium on VLSI. ***GLSVLSI-2015***
- **Technical Program Committee**, The 52st Design Automation Conference. ***DAC-2015***
- **Technical Program Committee**, The 6th Green and Sustainable Computing Conference. ***IGSC-2015***
- **Technical Program Committee**, The 32nd IEEE International Conference on Computer Design. ***ICCD-2014***
- **Technical Program Committee**, The 24th Great Lake Symposium on VLSI. ***GLSVLSI-2014***
- **Technical Program Committee**, The Fourth International Green Computing Conference. ***IGCC-2014***
- **Technical Program Committee**, The IEEE International Symposium on Quality Electronic Design. ***ISQED-2014***
- **Technical Program Committee**, The Fourth International Green Computing Conference. ***IGCC-2013***
- **Program Session Chair** of The IEEE International Symposium on Quality Electronic Design. ***ISQED-2013***
- **Technical Program Committee**, The IEEE International Symposium on Quality Electronic Design. ***ISQED-2013***
- **Technical Program Committee**, The International Symposium on Low Power Electronics Design. ***ISLPED-2012***
- **Technical Program Committee**, The IEEE International Symposium on Quality Electronic Design. ***ISQED-2012***
- **Technical Program Committee**, The 2011 ACM International Conference on Computing Frontiers. ***CF-2011***
- **Technical Program Committee**, The IEEE International Symposium on Quality Electronic Design. ***ISQED-2011***
- **Technical Program Committee**, The 9th IEEE International Conference on Computer Systems and Applications ***AICCSA-2011***
- **Reviewer,** International Symposium on High-Performance Computer Architecture. ***HPCA-2012***
- **Reviewer,** Design, Automation & Test in Europe. ***DATE-2012***
- **Reviewer**, The 19th International Conference on Parallel Architectures and Compilation Techniques. ***PACT-2010***
- **Reviewer**, The First International Green Computing Conference. ***IGCC-2010***
- **Reviewer,** The 23rd International Conference on Supercomputing. ***ICS*-2009**
- **Reviewer**, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems. ***CASES*-2009**
- **Reviewer**, The 35th International Symposium on Computer Architecture. ***ISCA-2008***
- **Reviewer**, The XXVI IEEE International Conference on Computer Design. ***ICCD-2008***
- **Reviewer**, The ACM International Conference on Computing Frontiers. ***CF-2008***
- **Reviewer**, International Symposium on Computer Architecture and High Performance Computing. ***SBAC-PAD-2007***
- **Reviewer**, International Symposium on Low Power Electronics and Design. ***ISLPED*-2009**
- **Reviewer**, the ACM Transactions on Embedded Computing Systems. ***TECS***
- **Reviewer**, The ACM Transactions on Design Automation of Electronic Systems. ***TODAES***

- **Reviewer**, The IEEE Transactions on COMPUTER-AIDED DESIGN of Integrated Circuits and Systems. ***TCAD***
- **Reviewer**, The International Journal of Parallel Programming. ***IJPP***
- **Reviewer**, The IEEE Transactions on Very Large Scale Integration (VLSI) Systems. ***TVLSI***
- **Reviewer**, The IEEE Computer Architecture Letters ***CAL***
- **Reviewer**, IEEE Transactions on Parallel and Distributed Systems. ***TPDS***
- **Reviewer**, ACM Transactions on Architecture and Code Optimization. ***TACO***
- **Reviewer**, IEEE Transactions on Parallel and Distributed Systems. ***TPDS***
- **Reviewer,** IEEE Embedded Systems Letters. ***ESL***
- **Technical Program Committee member**, International Millennium Seminar on Electrical Engineering. ***IMSEE'2000***
- **Technical Program Committee member**, The First Educational Seminar and Specialized Course for Simulink, Electrical Engineering Department, Sharif University of Technology, *23-24 October 2000*.

UNIVERSITY SERVICE

- **Member of Undergraduate Program,** Electrical and Computer Engineering Department, UC Davis, 2019-2020
- **Member of IT Website and Social Media,** Electrical and Computer Engineering Department, UC Davis, 2019-2020
- **Member of Graduate Admission,** Electrical and Computer Engineering Department, UC Davis, 2019-2020
- **Member of Tenure and Promotion Committee***,* Electrical and Computer Engineering Department, GMU, Fall 2018
- **Member of graduate recruitment committee,** Department of Electrical and Computer Engineering, GMU, 2017-present
- **Member of PhD committee,** Department of Electrical and Computer Engineering, GMU, 2016-present
- **Member of Advisory Committee***,* Research and Technology Commercialization (R&TC), Cybersecurity working group, Commonwealth of Virginia, 2018
- **Member of advisory to department chair committee,** Department of Electrical and Computer Engineering, GMU, 2015-2016
- **Founding Chair of distinguished talk series committee,** Department of Electrical and Computer Engineering, GMU, 2015-present
- **Member of new faculty search committee,** Department of Electrical and Computer Engineering, Computer Engineering Program, GMU, 2015
- **Member of new faculty search committee,** Department of Electrical and Computer Engineering, Computer Engineering Program GMU, 2016
- **Presentation Judge, Presenter and Advisor,** Louis Stokes Alliance for Minority Participation (LSAMP), 2015.
- **Member of PhD student proposal/dissertation committees**, Department of Electrical and Computer Engineering, Department of Computer Science, Department of Information Science and Technology, 2013-present
- **IT PhD program graduate advising**, 2015-present
- **Mentor for Office of Student Scholarship, Creative Activities, and Research (OSCAR),** Mentored undergraduate student for research in big data technology and hardware security and trust, 2016 and 2017
- **Contributed in the development of CYSE 475 Cyber Physical Systems course**, Part of new BS in Cyber Security program
- **Coordinator for computer engineering technical qualifying exam,** Department of Electrical and Computer Engineering, GMU, 2016