CURRICULUM VITAE
HUSSAIN AL-ASAAD

1. CONTACT INFORMATION

- *Work*:
  Department of Electrical & Computer Engineering
  University of California, One Shields Avenue, Davis, CA 95616-5294
  Tel: (530) 752-5545 and *Fax*: (530) 752-8428
  E-mail: halasaad@ece.ucdavis.edu
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- *Home*:
  4900 Natomas Blvd. Apt 828, Sacramento, CA 95835
  Tel: (916) 419-2839

2. PROFESSIONAL EXPERIENCE

- *Associate Professor* (July 2008- present)
  University of California, ECE Department, Davis, California.
  Conducting teaching and research in the areas of computer-aided design verification and testing, fault tolerant computing, and VLSI architectures.
- *Assistant Professor* (October 1998- June 2008)
  University of California, ECE Department, Davis, California.
  Conducting teaching and research in the areas of computer-aided design verification and testing, fault tolerant computing, and VLSI architectures.
- *Research Assistant* (May 1994 - August 1998)
  University of Michigan, EECS Department, ACAL Laboratory, Ann Arbor, Michigan.
  Conducted research in the areas of design verification, built-in self-test, delay computation, and safety critical applications.
- *Teaching Assistant* (April 1992 - September 1993)
  Northeastern University, ECE Department, Boston, Massachusetts.
  Served as an instructor for a circuits & systems laboratory.
  Served as an instructor and developer of a digital system design laboratory.
  Graded a digital circuit design course.
- *Teaching Assistant* (February 1991 - July 1991)
  American University of Beirut, Lebanon.
  Served as an instructor for a logic design laboratory.
  Served as a lecturer for a PASCAL & BASIC programming course.
  Graded an engineering mathematics course.
- *Programmer (Summer Training)* (July 1990 - October 1990)
  Intelligent Systems Co., Beirut, Lebanon.
  Developed an accounting program using Foxpro database language.

3. EDUCATION

- *University of Michigan*, Ann Arbor, Michigan. (September 1993 - August 1998)
  Doctor of Philosophy in Computer Science and Engineering.
  Dissertation advisor: John P. Hayes.
  Dissertation title: "Lifetime validation of digital systems via fault modeling and test generation".
- *Northeastern University*, Boston, Massachusetts. (September 1991 - July 1993)
  Master of Science in Electrical Engineering. Major: Computer Engineering.
  Thesis title: "On the design of fault-tolerant VLSI and WSI non-homogenous multipipelines".
- *American University of Beirut*, Lebanon. (February 1991 - June 1991)
  Attended one graduate term in Electrical Engineering.
- *American University of Beirut*, Lebanon. (September 1986 - September 1990)
  Bachelor of Engineering in Computer and Communications.
  Project title: "Design, implementation, and computer simulation of a traffic light controller".

4. AWARDS, SCHOLARSHIPS, FELLOWSHIPS, AND HONORS

- Listed in Who's Who in Engineering, 2007.
- Listed in Who's Who in America, 2006-2007.
- IEEE Senior Member, 2005.
- National Science Foundation CAREER Award, 2001-2006.
- Certificate of outstanding contribution, International Test Conference, 2003 and 2006.
- Certificate of appreciation, Autotestcon, 2000, 2003, and 2004.
- Certificate of outstanding contribution, Northwest Test Workshop, 2001-2002.
- Professor of the Year Award, Department of ECE, University of California, Davis, 2001.
- Certificate of appreciation, VLSI Test Symposium, 1993 and 2000.
- Certificate of appreciation, International High-Level Design Validation & Test Workshop, 1997.
- Student Travel Grant, International Conference on Computer-Aided Design, 1995.
- EECS Summer Fellowship, University of Michigan, 1994.
- Bachelor of Engineering with distinction, 1990.
- Dean's honor list: All the semesters of undergraduate study, 1986 - 1990.
- Winner of the four-year Aramco scholarship, 1986 - 1990.
- Full tuition scholarship at the American University of Beirut, 1986 - 1990.
- Ranked first in class, High school, 1984 - 1986.

5. PROFESSIONAL ACTIVITIES

- *Organizing Committee Member:* International High Level Design Validation and Test Workshop (2008), International Conference on Computer Design—ICCD (2009).
- *Program Committee Member:* International Conference on Circuits, Signals, and Systems (2005, 2006, 2007, 2010), International Conference on Computer Design—CDES (2005, 2006, 2007, 2008, 2010), International High Level Design Validation and Test Workshop (2004, 2005, 2006, 2007), International Conference on VLSI (2003, 2004), Microprocessor Test and Verification Workshop (1999, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011), International Conference on Parallel and Distributed Processing Techniques and Applications (2007, 2010).
- *Technical paper referee*: International Conference on Circuits, Signals, and Systems (2005, 2006, 2007, 2010), International High Level Design Validation and Test Workshop (2004, 2005, 2006), Microprocessor Test and Verification Workshop (2011), International On-Line Testing Symposium (2003), Defect and Fault Tolerance Symposium (2002), International Test Conference (1996, 1998, 2000-2010), VLSI Test Symposium (1996-1998, 2000, 2005), Design Automation Conference (1998-1999, 2001-2003), IEEE Transactions on Circuits & Systems-II (2000), Journal of Electronic

Testing (1996, 2001, 2004, 2005, 2009), Journal of Supercomputing (2004, 2005), IEEE Transactions on Computers (1997, 2005, 2006, 2007, 2008), IEEE Transactions on CAD (2000, 2002, 2006), IEEE Transactions on VLSI (2000, 2005, 2007, 2010), ACM Transactions on Design Automation of Electronic Systems (2007), Microelectronics Journal (2008).

- *Technical Panel Member*: System Level Design Panel for the Information Sciences & Engineering directorate of the National Science Foundation (2004), Test Panel for the Design Automation Program of the National Science Foundation (2001).
- *Technical Proposal Reviewer*: Natural Sciences and Engineering Research Council of Canada (2003), Design Automation Program of the National Science Foundation (2002), University of California MICRO Program (2000), U.S. Civilian Research & Development Foundation—Cooperative Grants Program (2006), France-Berkeley Fund (2006).
- *Technical Book Reviewer*: IEEE Press (2002), Thomson Nelson – Higher Education (2004), Morgan Kaufmann Publishers (2005-2006), John Wiley & Sons, Inc. (2005).
- *Technical Session Chair*: VLSI Test Symposium (2005), International Conference on Computer Design—ICCD (2005), International Conference on Computer Design—CDES (2005, 2006, 2007, 2009, 2010), International Test Conference (2003, 2006), International Conference on VLSI (2002-2004), International Test Synthesis Workshop (2004), International Conference on Circuits, Signals, and Systems (2005, 2006), Microprocessor Test and Verification Workshop (2005), International High Level Design Validation and Test Workshop (2006).
- *Professional Society Member*: IEEE and Sigma Xi.

6. RESEARCH INTERESTS

My research interests are in the areas of computer-aided design verification and testing, fault-tolerant computing, and VLSI architectures. Currently, my research focuses on the comprehensive lifetime validation of digital systems that uses fabrication fault testing and simulation techniques and accounts for design errors, fabrication faults, and operational faults. The specific contributions of my publications can be organized in the following categories:

- Simulation-Based Design Verification
- Post Silicon Verification
- On-Line Testing
- Global Fault Collapsing
- Functional Testing and Verification
- Fault Tolerant Computing
- Low-Power Design

7. PUBLICATIONS

[1] A. Sayed and H. Al-Asaad, "Low-power flip-flops: survey, comparative evaluation, and a new design", *IACSIT International Journal of Engineering and Technology*, Vol. 3, No. 3, pp. 279-286, June 2011.

[2] H. Al-Asaad, "Efficient techniques for reducing error latency in on-line periodic BIST", *IEEE Instrumentation and Measurement magazine*, Vol. 13, No. 4, pp. 28-32, August 2010.

[3] H. Al-Asaad, "Time-redundant logic-level protection mechanisms from soft errors in digital systems", *Proc. International Conference on Computer Design* (CDES), 2010, pp. 17-21.

[4] C. Chiem and H. Al-Asaad, "A comparison of NMOS to PMOS starved buffer implementations for the delay line in a PWM DC-DC converters", *Proc. International Conference on Computer Design* (CDES), 2010, pp. 10-16.

[5] H. Al-Asaad, "New global fault collapsing techniques for combinational library modules", *International Journal on Modeling and Simulation*, Vol. 30, No. 1, pp. 30-37, 2010.

[6] H. Al-Asaad, "Efficient techniques for reducing error latency in on-line periodic BIST", *Proc. Autotestcon*, 2009, pp. 173-177.
[7] H. Al-Asaad, "Detection and isolation of faulty processors in multiprocessor systems via TMR-based time redundant task scheduling", *Proc. International Conference on Computer Design* (CDES), 2009, pp. 42-47.
[8] C. Chiem and H. Al-Asaad, "Low power methodologies and challenges for PWM DC-DC converters", *Proc. International Conference on Computer Design* (CDES), 2009, pp. 70-75.
[9] J. Campos and H. Al-Asaad, "A novel mutation-based validation paradigm for high-level hardware descriptions", *IEEE Transactions on VLSI*, Vol. 16, No. 11, pp. 1499-1512, November 2008.
[10] S. Aldeen and H. Al-Asaad, "A new method for power estimation and optimization of combinational circuits", *Proc. International Conference on Microelectronics*, 2007, pp. 395-398.
[11] H. Al-Asaad, "Efficient global fault collapsing for combinational library modules", *Proc. International Conference on Computer Design* (CDES), 2007, pp. 37-43.
[12] A. Sayed and H. Al-Asaad, "A new statistical approach for glitch estimation in combinational circuits", *Proc. International Symposium on Circuits and Systems*, 2007, pp. 1641-1644.
[13] J. Campos and H. Al-Asaad, "Circuit profiling mechanisms for high-level ATPG", *Proc. Microprocessor Test & Verification Workshop*, 2006, pp. 9-14.
[14] H. Al-Asaad, "AGFC: An approximate simulation-based global fault collapsing tool for combinational circuits", *Proc. International conference on Circuits, Signals, & Systems*, 2006, pp. 248-253.
[15] H. Al-Asaad and P. Moore, "Non-concurrent on-line testing via scan chains", *Proc. Autotestcon*, 2006, pp. 683 - 689.
[16] A. Sayed and H. Al-Asaad, "A new low power high performance flip-flop", *Proc. International Midwest Symposium on Circuits and Systems*, 2006, pp. 723-727.
[17] A. Sayed and H. Al-Asaad, "Survey and evaluation of low-power flip-flops", *Proc. International Conference on Computer Design* (CDES), 2006, pp. 77-83.
[18] J. Campos and H. Al-Asaad, "Search-space optimizations for high-level ATPG", *Proc. Microprocessor Test & Verification Workshop*, 2005, pp. 84-89.
[19] J. Campos and H. Al-Asaad, "MVP: A mutation-based validation paradigm", *Proc. International High-Level Design Validation & Test Workshop*, 2005, pp. 27-34.
[20] H. Al-Asaad, "EGFC: An exact global fault collapsing tool for combinational circuits", *Proc. International Conference on Circuits, Signals, & Systems*, 2005, pp. 56-61.
[21] H. Al-Asaad, G. Valliappan, and L. Ramirez, "A novel functional testing and verification technique for logic circuits", *Proc. International Conference on Computer Design (CDES)*, 2005, pp. 129-135.
[22] H. Arteaga and H. Al-Asaad, "On Increasing the Observability of Modern Microprocessors", *Proc. International Conference on Computer Design (CDES)*, 2005, pp. 91-96.
[23] J. Campos and H. Al-Asaad, "Mutation-based validation of high-level microprocessor implementations", *Proc. International High-Level Design Validation & Test Workshop*, 2004, pp. 81-86.
[24] J. Campos and H. Al-Asaad, "Concurrent design error simulation for high-level microprocessor implementations", *Proc. Autotestcon*, 2004, pp. 382-388.
[25] H. Arteaga and H. Al-Asaad, "Approaches for monitoring vectors on microprocessor buses", *Proc. International Conference on VLSI*, 2004, pp. 393-398.
[26] A. Sayed and H. Al-Asaad, "Survey and evaluation of low-power full-adder cells", *Proc. International Conference on VLSI*, 2004, pp. 332-338.
[27] H. Al-Asaad, "A novel Markov model for the reliability prediction of fault tolerant non-homogenous multipipelines", *Proc. Autotestcon*, 2003, pp. 664-669.
[28] H. Al-Asaad and A. Sarvi, "Fault tolerance for multiprocessor systems via time redundant task scheduling", *Proc. International Conference on VLSI*, 2003, pp. 51-57.
[29] H. Al-Asaad and R. lee, "Simulation-based approximate global fault collapsing", *Proc. International Conference on VLSI*, 2002, pp. 72-77.

[30] H. Al-Asaad and J. P. Hayes, "Logic design verification via simulation and automatic test pattern generation", *Journal of Electronic Testing: Theory and Applications*, Vol. 16, No. 6, pp. 575-589, December 2000.
[31] H. Al-Asaad and M. Shringi, "On-line built-in self-test for operational faults", *Proc. Autotestcon*, 2000, pp. 168-174.
[32] H. Al-Asaad and J. P. Hayes, "ESIM: A multimodel design error and fault simulator for logic circuits", *Proc. VLSI Test Symposium*, 2000, pp. 221-228.
[33] H. Al-Asaad, J. P. Hayes, and T. Mudge, "Modeling and detecting control errors in microprocessors", *Digest of Papers: International Congress on Dynamics & Control of Systems*, 1999, pgs 8.
[34] H. Al-Asaad, B. T. Murray, and J. P. Hayes, "On-line BIST for embedded systems", *IEEE Design and Test of Computers*, Vol. 15, No. 4, pp. 17-24, November 1998.
[35] D. Van Campenhout, H. Al-Asaad, J. P. Hayes, T. Mudge, and R. Brown, "High-level design verification of microprocessors via error modeling", *ACM Transactions on Design Automation of Electronic Systems*, Vol. 3, No. 4, pp. 581-599, October 1998.
[36] H. Al-Asaad, *Lifetime Validation of Digital Systems via Fault Modeling and Test Generation*, Ph.D. Dissertation, University of Michigan, Ann Arbor, September 1998.
[37] H. Al-Asaad, J. P. Hayes, and B. T. Murray, "Scalable test generators for high-speed datapath circuits", *Journal of Electronic Testing: Theory and Applications*, Vol. 12, Nos. 1/2, pp. 111-125, February 1998. (Reprinted in M. Nicolaidis, Y. Zorian, and D. K. Pradhan (editors), *On Line-Testing for VLSI*, Kluwer Academic Publishers, Boston, 1998.)
[38] H. Al-Asaad, D. Van Campenhout, J. P. Hayes, T. Mudge, and R. Brown, "High-level design verification of microprocessors via error modeling", *Digest of Papers: International High-Level Design Validation & Test Workshop*, 1997, pp. 194-201.
[39] H. Al-Asaad, J. P. Hayes, and B. T. Murray, "Design of scalable hardware test generators for on-line BIST", *Digest of Papers: International On-Line Testing Workshop*, 1996, pp. 164-167.
[40] H. Al-Asaad and J. P. Hayes, "Design verification via simulation and automatic test pattern generation", *Proc. International Conference on Computer-Aided Design*, 1995, pp. 174-180.
[41] H. Al-Asaad, M. Vai, and J. Feldman, "Distributed reconfiguration of fault tolerant VLSI multipipeline arrays with constant interstage path lengths", *Proc. International Conference on Computer Design*, 1994, pp. 75-78.
[42] H. Al-Asaad, *On the Design of Fault-Tolerant VLSI and WSI Non-Homogenous Multipipelines*, M.S. Thesis, Northeastern University, Boston, September 1993.
[43] H. Al-Asaad and E. S. Manolakos, "A two-phase reconfiguration algorithm for VLSI and WSI linear arrays out of two-dimensional architectures", *Proc. International Workshop on Defect &Fault Tolerance in VLSI Systems*, 1993, pp. 56-63.
[44] H. Al-Asaad and E. Czeck, "Concurrent error correction in iterative circuits by recomputing with partitioning and voting", *Proc. VLSI Test Symposium*, 1993, pp. 174-177.
[45] H. Al-Asaad and M. Vai, "A real time reconfiguration algorithm for VLSI and WSI arrays", *Proc. International Workshop on Defect & Fault Tolerance in VLSI Systems*, 1992, pp. 52-59.

8. SOFTWARE TOOLS

- ESIM: A simulation tool that integrates logic fault and design error simulation for logic circuits. ESIM was distributed to several researchers that used it in their research.
- AGFC: An approximate global fault collapsing tool for combinational circuits. AGFC is useful for both research and education purposes.
- EGFC: An exact global fault collapsing tool for combinational circuits. EGFC is useful for both research and education purposes.

9. PRESENTATIONS AND INVITED LECTURES

[1] "Time-redundant logic-level protection mechanisms from soft errors in digital systems", Presented at *International Conference on Computer Design* (CDES), July 2010.
[2] "A comparison of NMOS to PMOS starved buffer implementations for the delay line in a PWM DC-DC converters", Presented at *International Conference on Computer Design* (CDES), July 2010.
[3] "Efficient techniques for reducing error latency in on-line periodic BIST", Presented at *Autotestcon*, September 2009.
[4] "Detection and isolation of faulty processors in multiprocessor systems via TMR-based time redundant task scheduling", Presented at *International Conference on Computer Design* (CDES), July 2009.
[5] "Efficient global fault collapsing for combinational library modules", Presented at *International Conference on Computer Design* (CDES), June 2007.
[6] "Circuit profiling mechanisms for high-level ATPG", Presented at *Microprocessor Test & Verification Workshop*, December 2006.
[7] "Hardware mechanisms for system-level test and post-silicon validation", Presented at Intel Corp., Santa Clara, CA, November 2006.
[8] "AGFC: An approximate simulation-based global fault collapsing tool for combinational circuits", Presented at *International conference on Circuits, Signals, & Systems*, November 2006.
[9] "Survey and evaluation of low-power flip-flops", Presented at *International Conference on Computer Design* (CDES), June 2006.
[10] "Search-space optimizations for high-level ATPG", Presented at *Microprocessor Test & Verification Workshop*, November 2005.
[11] "EGFC: An exact global fault collapsing tool for combinational circuits", Presented at *International conference on Circuits, Signals, & Systems*, October 2005.
[12] "A novel functional testing and verification technique for logic circuits", Presented at *International Conference on Computer Design (CDES)*, June 2005.
[13] "Concurrent design error simulation for high-level microprocessor implementations", Presented at *Autotestcon*, September 2004.
[14] "Approaches for monitoring vectors on microprocessor buses", Presented at *International Conference on VLSI*, June 2004.
[15] "A novel Markov model for the reliability prediction of fault tolerant non-homogenous multipipelines", Presented at *Autotestcon*, September 2003.
[16] "Fault tolerance for multiprocessor systems via time redundant task scheduling", Presented at *International Conference on VLSI*, June 2003.
[17] "Simulation-based approximate global fault collapsing", Presented at *International Conference on VLSI*, June 2002.
[18] "A comprehensive high-level design validation approach for microprocessors", Presented at *Industrial Affiliates Conference*, University of California, Davis, January 2001.
[19] "On-line built-in self-test for operational faults", Presented at *Autotestcon*, September 2000.
[20] "ESIM: A multimodel design error and fault simulator for logic circuits", Presented at *VLSI Test Symposium*, May 2000.
[21] "Modeling and detecting control errors in microprocessors", Presented at *International Congress on Dynamics & Control of Systems*, August 1999.
[22] "Lifetime validation of digital systems via fault modeling and test generation", Presented at Hewlett-Packard Corp., Roseville, CA, and Intel Corp., Folsom, CA, February 1999.
[23] "Lifetime validation of digital systems via fault modeling and test generation", Presented at Advanced Computer Architecture Laboratory, University of Michigan, August 1998.

[24] "Scalable test generators for high-speed datapath circuits", Presented at *Annual Industrial Partners of Computer Science and Engineering Review*, University of Michigan, March 1998.
[25] "High-level design verification of microprocessors via error modeling", Presented at *International High-Level Design Validation & Test Workshop*, November 1997.
[26] "Hardware design verification via error modeling and test generation", *Computer-Aided Design Verification of Digital Systems course (EECS-578)*, University of Michigan, October 1997.
[27] "Error modeling and test generation", Presented at *DARPA Design Verification Project Review*, University of Michigan, April 1997.
[28] "Test generation and fault simulation tools", *Digital System Testing course (EECS-579)*, University of Michigan, February 1997.
[29] "Design verification via testing and simulation", Presented at *Annual Industrial Partners of Computer Science and Engineering Review*, University of Michigan, March 1996.
[30] "Design verification via simulation and automatic test pattern generation", Presented at *International Conference on Computer-Aided Design*, November 1995.
[31] "Distributed reconfiguration of fault tolerant VLSI multipipeline arrays with constant interstage path lengths", Presented at *International Conference on Computer Design*, October 1994.
[32] "Concurrent error correction in iterative circuits by recomputing with partitioning and voting", Presented at *VLSI Test Symposium*, April 1993.
[33] "A real time reconfiguration algorithm for VLSI and WSI arrays", Presented at *International Workshop on Defect and Fault Tolerance in VLSI Systems*, November 1992.

10. TECHNOLOGY TRANSFER

PATENTS

- J. Campos and H. Al-Asaad, "Automatically generating an input sequence for a circuit design using mutation-based verification", Patent No. US 7694253 B2, April 2010.

START-UP COMPANY

- Mutant Logic (2006-2008): Founded in 2006 as a spin-off of my research with my Ph.D. student Jorge Campos. Mutant Logic licensed our MVP technology from UC Davis.

11. TEACHING ACTIVITIES AT UC-DAVIS (JANUARY 1999 — JUNE 2011)

- *Undergraduate Courses Taught*
  - Digital Systems I (EEC180A): Twelve Quarters/Sessions.
  - Digital Systems II (EEC180B): Four Quarters.
  - Testing and Verification of Digital Systems (EEC183): Eleven Quarters.
  - Computer Structure and Assembly Language (EEC70): Three Quarters/Sessions.
  - Circuits I (ENG 17): Three Sessions.
  - Freshman Seminar (FRS003): Three Quarters.
- *Graduate Courses Taught*
  - Advanced Design Verification of Digital Systems (EEC283): Eight Quarters.
  - Digital System Testing (EEC286): Five Quarters.
- *Course Development*: EEC183, EEC283, and FRS003.

12. STUDENT SUPERVISION AT UC-DAVIS (JANUARY 1999 — JUNE 2011)

- Luis Bustamante (Ph.D. student): Graduation expected in 2013.
- Calvin Chiem (M.S. student): Graduated 03/10.
- Manish Muttreja (M.S. student): Graduated 06/09.
- Ahmed Sayed (Ph.D. student): Graduated 06/07.

- Jorge Campos (Ph.D. student): Graduated 03/07.
- Hector Arteaga (M.S. student): Graduated 03/06.
- Stefanie Poon (M.S. student): Graduated 06/06
- Ganesh Valliappan (M.S. student): Graduated 08/05.
- Ra Roath (M.S. student): Graduated 12/04.
- Nadav Kanarik (M.S. student): Graduated 06/04.
- Alireza Sarvi (M.S. student): Graduated 06/02.
- Paolo Moore (M.S. student): Graduated 12/01.
- Raymond Lee (M.S. student): Graduated 12/01.
- Lourdes Ramirez (M.S. student): Graduated 12/01.
- Prabhjot Singh (M.S. student): Graduated 06/00.

13. COMMITTEE SERVICE AT UC-DAVIS (JANUARY 1999 — JUNE 2011)

- *Department-Level*
  - Undergraduate Programs Committee, 1998-2003 and 2006-2007.
  - Computer Usage Committee, 1998-2001.
  - Graduate Study Committee, 2003-2004.
  - Preliminary Examination Committee, 1999-2005, 2007-2008, and 2010-2011.
  - Faculty Search Committee, 2003-2004.
  - Teaching Assignment Committee, 2005-2007.
  - Computer and Information Technology Committee, 2008-2010.
  - Safety Committee, 2008-2010.
  - Honors and awards Committee, 2009-2011.
  - Ph.D. Thesis and Master Plans Committees: Served on 24 committees, 1999-2010.
  - Ph.D. Qualifying Committees: Served on 11 committees, 1999-2010.
- *College-Level*
  - Program Planning and Assessment Committee, 2001-2003.
- *University-Level*
  - Committee on Undergraduate Scholarships, Honors & Prizes, 2006-2009 and 2010-2011.