CURRICULUM VITAE

NAME: ROBERT W. BOWER

EDUCATION:

Primary and Secondary Education: Los Angeles, California
Served in the United States Air Force from 1954 to 1958
AB Honors Physics-University of California, Berkeley-1962
MS EE-California Institute of Technology-1963
Ph.D. Applied Physics-California Institute of Technology-1973

PROFESSIONAL EXPERIENCE:

1994- Expert witness in device physics and high technology patent cases before federal court of the U.S.A.

2009-2011 Senior Director Product Innovation, EPIR Technologies

2008- Member of the Strategy Advisory Board EPIR Technologies

2003- President of Bower Technology Inc. (BTI)

2003- Distinguished Visiting Fellow, Physics Dept. Queens University, Belfast University.

2000- Emeritus Professor, University of California, Davis. Research activities a variety of Ion Cut technologies and structures, in three-dimensional microstructures, semiconductor devices, solid-state sensors and actuators. Direct Bonding and SOI.

1995- President and CEO of Device Concept Inc.

1987-2000 Professor, Electrical and Computer Engineering Department. University of California, Davis. Research activities a variety of Ion Cut structures and Technologies, in three-dimensional microstructures, semiconductor devices, solid-state sensors and actuators. Direct Bonding and SOI.

1986-1987 Visiting Professor-Technical university of Munich. Research in biosensors and recrystallized silicon.

1979-1985 Advanced Micro Devices Inc. Served as a Senior Scientist and Manager of Bipolar Device Technology. In this capacity responsible for all new technology and design development and responsible for maintaining yield, reliability and performance standards on existing products in the division. Earlier work in the MOS division included manager of flash and redundancy technologies and development of nonvolatile RAMS.

1977-1978 Associate Professor, Electrical Science and Engineering Department, UCLA. Taught courses in circuit theory, semiconductor devices physics and VLSI methodology.

1975-1977 Mnemonics Inc.-General Partner, Vice President and then President of this CCD memory systems company. This company developed the first 64k CCD memory chips.

1970-1975 Consultant to TRW, Intel, Honeywell, GCA, AMD, Xerox, Hughes, U.S. Army, Universal Design, Nitron, Motorola, Datapoint, ITT, High Voltage Engineering and Eurocil. this consulting work spanned the areas of metal-semiconductor reliability, ion implantation, MOS memories, CMOS, silicon gate processing and CCD development.

1965-1970 Hughes A.C. Assistant Division Manager, MOS Division. Directed engineering and assisted in building MOS business at Hughes, which grew to be the most successful division in this billion-dollar corporation. Manager of the Applied Solid State Research Department of the Hughes Research laboratories. Directed all MOS, Microwave Solid State and Ion Implantation activities. Work in this department led to the commercial use of ion implantation in semiconductor processing. This work provided Hughes with a leadership position in CMOS watch circuitry that allowed them to become the largest producer of watch circuits in the world. The work resulting in the self-aligned gate ion implanted MOSFET was accomplished in this department.

HONORS AND AWARDS:
Elected Life Fellow of the IEEE, 2005

Elected a Fellow of the American Physical Society in 2004, "For the invention and development of the self-aligned gate transistor and major innovative contributions in the CCD, metal silicide and three-dimensional device technologies."

Presented a Distinguished Visiting Fellow Award, Physics Department, Queens University, Belfast. Granted to Researchers with an international reputation in areas of research in Physics at Queens University. Work on innovative methods of creating ion cut structures and technologies.

Presented the Alexander von Humbolt Research Award, April 2001. The Alexander von Humboldt Foundation (AvH) grants Humboldt Research Awards annually to foreign scholars with internationally recognized academic qualifications. The award is intended as a lifelong tribute to the past academic accomplishments of award winners. Work on Ion Cut 3-dimensional structures and processes.

Presented the Distinguished Alumni Award for year 2001 from the California Institute of Technology. This award is the most prestigious honor presented by the Institute. This award was initiated as a part of Caltech's 75th anniversary celebration in 1966 to recognize outstanding contributions of our alumni in business, community and professional life.

Elected a member of the National Academy of Engineering 1999. Dr. Robert W. Bower, Elected Feb. 16, 1999
Election to the National Academy of Engineering is among the highest professional distinctions accorded an engineer. Academy membership honors those who have made "important contributions to engineering theory and practice, including significant contributions to the literature of engineering theory and practice," and those who have demonstrated "unusual accomplishment in the pioneering of new and developing fields of technology."

In 1997, I was inducted as a member of the National Inventors Hall of Fame, for my invention of the self-aligned-gate ion-implanted MOSFET. The National Inventors Hall of Fame had only previously inducted about 130 members including such well know inventors as Edison, Bell, Steinmetz, Fermi, Pasteur, Tesla, Land, Ford, Marconi and Westinghouse. In the field of semiconductor devices and technology only five inventors (related to two inventions) had been previously inducted: Bardeen, Bratten and Schockley for the transistor and Kilby and Noyce for the integrated circuit.

In 1997 the Commerce Department of the United States Government presented Robert W. Bower with the Ronald H. Brown American Innovator Award.

Elected a Fellow of the IEEE in 1986 and later a Life Fellow , "For inventing the self-aligned

gate ion implanted MOSFET and for establishing ion implantation to fabricate semiconductor integrated circuits".

Elected Semiconductor Hall of Fame, 2003

Elected Hall of Scientists and Inventors

Paper selected as the most significant device paper of the 1966 International Electron Device Meeting (IEDM), "Insulated Gate Field Effect Transistors Fabricated Using the Gate as Source-Drain Mask". This device is used by the millions in virtually all modern integrated circuits is known as the Self-Aligned Gate (SAG) MOSFET. This appeared in the special 40th Anniversary Commemorative Edition of the IEDM where the most significant and interesting papers of the last 40 years were chosen from 1955 through 1994.

Member: Phi Beta Kappa, Sigma Xi, American Association for the Advancement of Science, American Physical Society.
Scientific Member: Boehmische Physical Society
HIGHLIGHTS OF MY CAREER DISCRIBED IN NUMEROUS PUBLICATIONS AND PATENTS:

- My career began with the invention and development of the Self-Aligned gate FET (SAGFET) The first 18 papers and patents 84, 85, 86, 87, 89, 90, 91, 92 & 93 of this CV describe this work as well as related topics of ion implantation applied to MOS and microwave devices a Several early papers and patents on the subjects of ion implanted semiconductor devices and methods of ion implantation and study of defect structures. The early SAGFET used the yet undeveloped method of ion implantation to produce this device structure. This required the development of an ion implanter (commercial implanters were not yet available), invention of a flood gun for implantation and discovery of a methodology to induce solid state epitaxial regrowth of implanted region.
- In the next phase of my career I developed and utilized RBS and several other analytical techniques to study defects, investigate phase changes and study growth kinetics of semiconductor and metal silicide and aluminide structures. This work was discussed in detail in my PhD thesis at Cal Tech which included an analysis of the widely used Al-Ti-Si contact system. This work is also described publications 19, 20, 23, 24 & 25 in this CV.
- While completing my PhD at Cal Tech I also served as a consultant to TRW where I invented and developed a very high-density form of a CCD called the Offset Gate CCD. This structure was used in surveillance satellites and was to as the key structure in Mnemonics where I served as a general partner and later CEO of this CCD memory company. Publications 26-30 and patents 95 & 96 of this CV described this work.
- I later served as a senior scientist and department manager at AMD where I worked on nonvolatile memory devices and advanced bipolar device technology. This work is described in patents 97-102 of this CV. Other inventions at AMD were kept as trade secrets.
- For a period of years I was a visiting professor at the Technical University in Munich, Germany and a professor at U.C. Davis. During this time my worked focused on wafer bonding, 3-dimensional structures, sensors and actuators, light emission in CMOS structures and then centered on activities related to Ion Cut technology and devices.
- This Ion Cut technology and devices work then continued in Berlin, Germany as an Alexander von Humbolt Research Award winner and Queen's University, Belfast as a Distinguished Visiting Fellow. My work during the years in Munich, UCD, Berlin and Belfast related to Ion Cut technology and devices is described in publications 40-43, 45-47, 49-72 & 75-81 and patents 103-109 & 112-114 in this CV. Light emission is described in patents 110 & 111 in this CV. Sensors and actuators are described in publications 33-39 of this CV.
- My current work is focused on solar cell development and light emission at EPIR technologies. Patent applications related to solar cells include 114-117 where 114

describes Ion Cut used in solar cell formation and 115-117 described methods of forming back contacts and tunnel junctions in tandem II-VI silicon solar cells.

Holder of 30 issued U.S. patents and author of 81 journal publications and conference proceedings. Author of chapters in three books, one on Ion Implantation (15) and two on Vascular Access Surgery (31).

RECENT OUTSIDE ACTIVITIES:

1. Invited to present the National Academy of Engineering Grand Challenges presentation entitled "The Challenges of Economical Solar Energy" at NMSU, March 2011.
2. Reviewer, National Research Council reports.
3. Reviewer APS journals
4. Guest Editor MRS Bulletin on SOI Technologies.
5. Invited participant in the Helsinki Materials Conference. Presentation on Ion Implantation and Ion Cut in Formation of 3-D structures.
6. NSF Reviewer.
7. Member IEEE Intellectual Property Committee
8. Invited to write Materials Science and Engineering Report (Elsevier) entitled "Low Temperature Direct Bonding".
9. Invited Speaker at the Beijing International Conference on Solid-State and Integrated Circuit Technology Oct. 21-23, 1998.
10. Invited paper MRS Bulletin, Tong and Bower, "Advances in Smart Cut Technology" Dec. 1998
11. Recent Invited Speaker, Berlin, Gottenberg, Hong Kong, Auckland, 2002-2008 on Ion Cut technologies, 3-dimensional circuits and light emission from silicon integrated circuits

LISTING OF PUBLICATIONS AND PATENTS:

1. R. W. Bower, R. Baron, J. W. Mayer and O. J. Marsh, DEEP (1-10 μm) PENETRATION OF ION-IMPLANTED DONORS IN SILICON. Applied Physics Letters, Vol. 9, No. 5, pp. 203-205, 1966.
2. R. W. Bower and H. G. Dill INSULATED GATE FIELD EFFECT TRANSISTORS FABRICATED USING THE GATE AS SOURCE-DRAIN MASK, Paper 16.6 International Electron Device Meeting, Washington, D.C., 1966.

3. J. W. Mayer, O. J. Marsh, R. Mankarious and R. Bower, Zn AND Te IMPLANTATIONS INTO GaAs, Journal of Applied Physics, Vol. 38, No. 4, pp. 1975-1976, 1967.

4. Ramzy G. Mankarious, Robert S. Ying, Robert W. Bower and David L. English HIGH POWER IMPATT DIODES UTILIZING ION IMPLANTATION, Paper 7.2 International Electron Devices Meeting, October 1967.

5. R. W. Bower, H. G. Dill and K. G. Aubuchon, "Characterization of MOSFETS formed by the Gate Masked Ion Implantation Technique" Paper 6.7, IEEE International Electron Devices Meeting Oct. 1967.

6. R. W. Bower, H. G. Dill, K. G. Aubuchon and S. A. Thompson. MOS FIELD EFFECT TRANSISTORS FORMED BY GATE MASKED ION IMPLANTATION. IEEE Transactions on Electron Devices, Vol. ED-15, No. 10, pp. 757-761, 1968.

7. R. W. Bower, K. G. Aubuchon and H. G. Dill, "Ion Implantation Techniques promise High Speed MOS Ics," Paper 14.7, IEEE International Electron Devices Meeting, Oct. 1968.

8. Robert S. Ying, Ramzy G. Mankarious, David L. English, Robert W. Bower and Leo E. Coerver CHARACTERIZATION OF ION-IMPLANTED IMPATT OSCILLATORS, IEEE Journal of Solid-State Circuits, Vol. SC-3 No. 3, September 1968.

9. R. S. Ying, R. G. Mankarious and R. W. Bower. HIGH-EFFICIENCY SUBHARMONIC OSCILLATIONS FOR SILICON DIODES AT FREQUENCIES UP TO 6 Ghz. IEEE Journal of Solid-State Circuits, Vol. SC-4, No. 6, pp. 388-391, 1969.

10. H. G. Dill, R. W. Bower, K. G. Aubuchon and T. N. Toombs ANOMALOUS BEHAVIOR IN STACKED-GATE MOS TETRODES Technical Paper WPM 4.4 ISSCC 1969, pp. 44-45.

11. R. W. Bower, H. G. Dill and M. R. MacPherson, 'Characterization of Ion-Implanted Planar Junctions', Paper 171, Electrochemical. Soc. Meeting Oct. 1969. Detroit,

Michigan.

12. N. E. Moyer, R. W. Bower and H. G. Dill, 'High-Speed MOS Integrated Circuits Utilizing Ion-Implantation', pp. 180-182, GOMAC Conference, Sept. 1969.

13. R. W. Bower 'Applications of Ion Implantation Doping to the Planar MOS Integrated Circuit Technology', NEREM RECORD 1969, pp. 120-121.

14. L. O. Bauer, R. W. Bower, E. Wolf, R. Haldman and R. Burns, "Junction Field Effect Microwave Switch Fabricated with Electron Beam Exposure and Ion Implantation Doping", Paper 20.4, IEDM, 1969.

15. R. W. Bower, DEVICE CONSIDERATIONS AND APPLICATIONS - Ion Implantation in Semiconductors, Academic Press, Chapter 6, pp. 224-249, 1970.

16. E. D. Wolf, L. O. Bauer, R. W. Bower, H. L. Garvin and C. R. Buckey. 'Electron Beam and Ion Beam Fabricated Microwave Switch'. IEEE Transactions on Electron Devices, Vol. ED-17, No. 6, pp. 446-449, 1970.

17. H. G. Dill, R. W. Bower and T. N. Toombs. 'Ion-Implanted MOS Technology', pp. 349-361, Ion Implantation Ed by F. Eisen and L. Chadderton, Gorden and Breach Science Publishers, 1970.

18. Robert W. Bower, ‘Applications of the Ion Implantation Technology to Semiconductor Devices’, Invited Paper, Colloque International Sur La Microelectronique Avancee’, Proceedings, April 1970.

19. R. W. Bower and J. W. Mayer. GROWTH KINETICS OBSERVED IN THE FORMATION OF METAL SILICIDES ON SILICON. Appl. Phys. Lett., Vol. 20, No. 9, pp. 359-361, 1971.

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21. A. M. Mohsen, R. W. Bower, and T. C. McGill. ‘Overlapping-Gate Buried-Channel Charge-Coupled Devices’, Electronics Letters, Vol. 9, No. 17, pp. 396-398. 1974.

22. R. W. Bower, T. A. Zimmerman and A. M. Mohsen. A HIGH DENSITY OVERLAPPING GATE CHARGE COUPLED DEVICE ARRAY Paper 2.6, IEEE International Electron Devices Meeting, Oct. 1973.

23. D. Sigurd, R. W. Bower, W. F. Van Der Weg and J. W. Mayer. CHARACTERIZATION OF POLYCRYSTALLINE LAYERS BY CHANNELLING

MEASUREMENTS. Thin Solid Films, Vol. 19, pp. 319-328, 1973.

24. R. W. Bower. CHARACTERISTICS OF ALUMINUM-TITANIUM ELECTRICAL CONTACTS ON SILICON. Appl. Phys. Lett., Vol. 23, No. 2, pp. 99-101, 1973.

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26. R. W. Bower, T. A. Zimmerman and A. M. Mohsen. THE TWO-PHASE OFFSET GATE CCD. IEEE Transactions on Electron Devices, ED-22, pp. 70-72, 1974.

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28. R. W. Bower, T. A. Zimmerman and A. M. Mohsen. PERFORMANCE CHARACTERISTICS OF THE OFFSET-GATE CHARGE-COUPLED DEVICE. IEEE Transaction on Electron Devices, ED-22, pp. 72-74, 1975.

29. Amr M. Mohsen, R. W. Bower, E. M. Wilder and D. M. Erb. A 64-kbit BLOCK ADDRESSED CHARGE-COUPLED MEMORY. IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 1, pp. 49-58, 1976.

30. Robert W. Bower. CCD LARGE-SCALE MEMORY. Paper 23.1, pp. 1-4, 1976 Wescon Digest of Professional Papers, 1976.

31. S. E. Wilson, M. L. Owens, R. W. Bower. PHYSIOLOGY OF ARTERIOVENOUS FISTULAS. Vascular Access Surgery, YearBook Medical Publishers, Chapter 6, revised 1985, pp. 101-114.

32. K. Haberber, P. Panish, R. Buchner, H. Steinberger and R. W. Bower. HIGH THROUGHPUT C02 LASER RECRYSTALIZATION FOR 3-D INTEGRATED DEVICES. Proceedings of Energy Pulse and Particle Beam Modification of Materials Conference, Dresden, DDR, 1987.

33. C. E. Hunt, J. N. Churchill, R. W. Bower and I-W Chao. TRANSIENT SPECTROSCOPY TECHNIQUES IN SILICON ON INSULATOR MATERIALS. Digest of Technical Papers, Euro-SOI"88", March 15, 3 pages, 1988.

34. R. W. Bower, R. Spencer and D. D. Lee, NONPLANAR SILICON STRAIN SENSORS. 1988 Solid-State Sensors Workshop Journal, June 6-9, Hilton Head, SC, pp. 39-42, 1988.

35. Michael Schwemberger and Robert W. Bower, "Modulated Enzyme Activity Biosensor", Proceedings of the Biomedical Engineering Symposium, Davis, Calif.

1989.

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37. Robert W. Bower, "The Design and Fabrication of a Self-Aligned Rigid Suspended Plate", Transducers 89, The International Symposium of Sensors, Actuators and Transducers.

38. Robert W. Bower, "The Compatibility of PECVD Diamond in the Design and Fabrication of a Self-Aligned Rigid Suspended Plat." Sensors and Actuators, Jan. 1990.

39. R. L. Smith, R. W. Bower and S. D. Collins. 'The Design and Fabrication of a Magnetically Actuated Micromachined Flow Valve'. Sensors and Actuators A, pp. 57-53, 1990.

40. M. S. Ismail, R. W. Bower, J. L. Veteran and O. J. Marsh. "Silicon Nitride Direct Bonding", Electronics Letters, July 1990, Vol. 26, No. 14, pp. 1045-1046.

41. R. W. Bower, M. S. Ismail and S. N. Farrens. "Aligned Wafer Bonding: A Key to Three-Dimensional Microstructures", *Journal of Electronics Materials*, Vol. 20, No. 5, pp. 383-387. June 1991.

42. M. S. Ismail and R. W. Bower, "Technological Considerations of Three-Dimensional CMOS Devices Formed With Aligned Wafer Bonding", Proc. the First Int. Symp. on Semiconductor Wafer Bonding Science, Technology and Applications, Electrochem. Soc. Mtng., Phoenix, AZ, Oct. 13-17, 1991, p. 474.

43. M. S. Ismail and R. W. Bower. "Platinum Silicide Fusion Bonding", *Electronics Letters*, Vol. 27, No. 13, pp. 1153-1155, 1991.

44. R. W. Bower and S. D. Collins, "Fractal Transitions in Diffusion-Limited Cluster Formation". *Physical Review A*, Vol. 43, No. 6, pp. 3165-3167, 1991.

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47. S. N. Farrens, B. Roberds, M. C. Boettcher, M. S. Ismail, R. W. Bower, C. Desmond

and C. E. Hunt, 'Mechanical Testing of Bonded Silicon on Insulator Wafers', presented at Material Research Society Mtng., Boston, MA, Dec. 1991.

48. R. Rofan, R. W. Bower, P. Kelly and J. Getty, "Photoelectric Measurement and Study of Diamond-Like Carbon Thin Films", *Journal of Electronic Materials*, Vol. 21, No. 1, 1992.

49. M. S. Ismail, R. W. Bower, B. E. Roberds, 'Polysilicon and Titanium Silicide+Polycide Fusion Bonding for 3-D Microdevices Applications', Technical Digest Solid-State Sensor and Actuator Workshop, Hilton Head, SC, pp. 86-89, June 1992.

50. R. W. Bower, M. S. Ismail and B. E. Roberds, 'Low Temperature Si_3N_4 Direct Bonding'. Published in *Appl. Phys. Lett., 28 June 1993 pp. 2485-3487*.

51. R. W. Bower, M. S. Ismail, B. E. Roberds and S. N. Farrens, 'One-Step Direct Bonding Process of Low Temperature Si_3N_4 and TiN Technology'. Conference on Solid-State Sensors and Actuators (Transducers 93), Yokohama, Japan. Published in the Journal of Transducers 93 June (1993).

52. Victor H. C. Watt, David Hwang, Mansour Moinpour, Reza Sadjadi, Gabi Neubauer and Robert W. Bower, Surface Roughness Investigation of SiO_2 Deposited from N_2O and SiH_4, Mat. Res. Soc. Symp. Vol 355, 1995 Materials Research Society.

53. Victor H. C. Watt, Robert W. Bower and Mansour Moinpour, “Atomic Force Microscopy, A key to direct wafer bonding”, Journal of Materials Science Letters 14 (1995) 96-98.

54. Robert W. Bower, Victor H. C. Watt, Rajagopal Sundararaman and Winnie Chan, Applications of Low Temperature direct Bonding in Microsensor structures, proc. of the 1994 ISHM Symp., Bos., MA, Nov. 15-17

55. Victor H. C. Watt and Robert Bower, Low Temperature direct bonding of non-hydophilic surfaces, Electronic Letts., April 1994, Vol. 30, No. 9, 693-695

56. R. W. Bower, W. Chan, L. Hong and V. H. C. Watt, mechanical properties of low temperature bonded materials. Volume 95-7, pp 107-114, Oct. 1995, Oct. 1995.

57. V.H.C. Watt, R. Bower, W. Chan, L. Hong, and M. Moinpour, “Direct Bonding of LPCVD Silicon Oxide Thin Films Deposited from N_2O and SiH_4”, Electoctrochemical Society Proceedings Volume 95-7, pp573-578, Oct. 1995

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59. Peer reviewed invited conference paper (see Invited talks #5) in The International Photonics Conference Journal PHOTONICS -96. R. Bower, "Low Temperature Direct Bonding Technology in Photontic Devices". pp 145-155, Dec. 1996

60. R. W. Bower & F. Y. -J. Chin, "Low Temperature Direct Silicon Wafer Bonding Using Ar Activation", Japanese Journal of Applied Physics, vol.36, No.5A, pp.L527-L528. 1997

61. Y.A. Li and R.W. Bower, "Low Temperature Direct Bonding using Pressure and Temperature". Proceedings of SPIE, Vol. 3184, pp 124-128, June 1997.

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65. Y. A. Li & R. W. Bower, "Systematic Low Temperature Single Crystal Silicon Direct Bonding Process using Pressure and Temperature", vol. 37, No.3, March 1998, Japanese Journal of Applied Physics (6 pages).

66. Robert W. Bower, Louis LeBoeuf and Y. Albert Li, "Transposed Splitting of Silicon Implanted with Spatially Offset Distributions of Hydrogen and Boron". Publiblished, Il Nuovo Cimento Dec 1997, Vol. 19 D, N. 12, pp 1871-1873.

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68. Y. Albert Li, Robert W. Bower & Izak Bencurya, "Low Temperature Cu Direct Bonding", Puplished in JJAP 1998.

69. Jean-Pierre Colinge and Robert W. Bower, Guest Editors "Silicon-On-Insulator Technology", Invited Special edition of the MRS Bulletin Dec. 1998.

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71. Robert W. Bower, U. S.-Finland Workshop on Microstructuring Science and Technology, Hotel Haikko Manor, Porvoo, Finland Aug. 5-7, 1998. Elements of Three Dimensional Microstructure Technology.

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PATENTS:

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103. R. W. Bower and M. S. Ismail. ALIGNED WAFER BONDING. Patent U.S. 5,236,118, filed May 12, 1992 issued August 17, 1993.

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106. Robert W. Bower, Method of Transferring Thin Films of Processed Materials, Filed Dec. 2, 1998.

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111. Robert W. Bower, Light Emission from Semiconductor Integrated Circuits, Filed July 3, 2006. Patent allowed May 5, 2009. U.S. 7,586,115, CIP of U. S. 7,061,006 B1.

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115. Peter Dreiske, Robert W. Bower , Sivalingan Sivananthan, Backside Contact Process for Single and Multi-Junction II-VI Solar Cells using silicon, patent applied for August 2009.

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SHORT COURSES:

Frank B. Micheletti, Robert Bower, Daryl T. Butcher, Robert W. Dutton, Vincent

Nickel, Leo Rideout, Michael Splinter, Al Tasch and Roderick Watts, "Very Large Scale Integration", UCLA Extension, 1979-1981

Gideon D. Amir, Robert W. Bower, Derek T. Bray and Michael Feuer "Gate Arrays: The Semi-Custom LSI Approach" Continuing Education Institute 1984

In the course of Dr. Bower's career he has made over 100 invited and contributed talks at conferences, universities and in industry.

RECENT INVITED TALKS:

1. Invited presentation, National Academy of Engineering Grand Challenges presentation entitled "The Challenges of Economical Solar Energy" at NMSU, March 2011.
2. Invited talks on 3 dimensional integrated devices and light emission from silicon integrated circuits, at universities in Singapore, Hong Kong, Australia and Belfast, Vienna, Berlin and NZ 2001-present.
3. Invited paper: Robert W. Bower Tuscon Precision Engineering Conference. "Low Temperature Direct Bonding of Silicon" Jan. 1995.
4. Invited Seminar, Advanced Micro Devices Inc. Technical Excellence Seminar Series: "Semiconductor Technology: From Self Aligned Gate to Bonded Structure" May 1995.
5. Invited participatant in the California State Bar Association's "Life Cycle of a Patent" April 1995, San Francisco, California.
6. Invited talk, Condensed Matter Seminar, Physics Department, University of California: "Low and High Temperature Direct Bonding of Semiconductor Materials" April 1996 Davis, CA.
7. Invited lecture series, Tsinghua University, Beijing, China. Three talks on Low Temperature Bonding and Applications. Oct. 1996
8. Invited lecture, Peking University, Low Temperature Bonding. Oct. 1996
9. Invited lectures, Fudan University, Low Temperature Bonding and Applications to Smart Cut, 2 invited talks. Oct. 1996
10. Invited talk, Shanghai Institute of Science and Technology, Low Temperature Bonding. Oct. 1996
11. Invited talk, Hong Kong Science and Technology University, Bonding Technology and applications to SOI. Nov. 1996
12. Invited talk, City University of Hong Kong, Bonding technology and Smart Cut. Nov. 1996
13. Invited lectures, Burapha University, Thailand, Semiconductor Devices and Bonding Technology. Nov. 1996
14. Invited talk, National Science and Technology Development Agency, History of Integrated Circuits from transistors to three-dimensional structures. Nov. 1996
15. Invited talk, NTU University, Singapore, "The Evolution of Three Dimensional Microelectronics from Early Transistors to Aligned Bonded Structures", Dec 1996
16. Invited Paper, International Photonics Conference, "LowTemperatureDirect Bonding Technology in Photontic Devices", Madras,India,Dec.1996.

17. Invited talk, University of Illinois, Chicago, Joint Colloquium of Physics and Engineering, "Low Temperature Aligned Bonding of semiconductor Surfaces and Applications to Three Dimensional Microstructures" 1997
18. Invited talk ECE Dept. UCSD, "Ion Cut and Low Temperature Direct Bonding" 1997
19. Boemische Annual Meeting, Mesa, Arizona, 1997
20. Fujitsu conference, "3-d integration" UCD 1998
21. Invited workshop, Finland. 1998
22. Invited talk, Beijing, China Oct 1998
23. Invited talk, Univ. of California, Dept. of Chemical Engineering and Material Science. Innovation and the Self-Aligned Gate Transistor, March 1998.
24. Invited talk, University of Ill., Physics Dept. Chicago. Interactions of Implanted Ions in the Formation of Thin Film Layers of Condensed Matter, February 1998.
25. Invited talk, University of the West Indies, Mona. From Transistors to Three Dimensional Integrated Circuits, March 1998.
26. Invited talk, University of the West Indies, Mona. Microelectronics and Your Wildest Dreams, March 1998.
27. Invited Talk, Technical University of Munich, Munich Germany,
28. Invited Talk, Technical University of Berlin, Berlin Germany,
29. Invited Talk, U. S.-Finland Workshop on Microstructuring Science and Technology, Hotel Haikko Manor, Porvoo, Finland Aug. 5-7, 1998. (see paper)
30. Invited Talk, Firth International Conference on Solid-State and Integrated-Circuit Technology, 3-Dimensional microelectronic integration, Oct. 21-23, 1998 Beijing, China (see paper).
31. Invited Talk, Bejing Academy of Sciences, Beijing, China, Vertically Stacked Microelectronics. 1999
29. Invited Talks, 3-d nanostructures; Berlin, Germany; Modena, Italy; Vienna, Austria; Guttenberg, Sweden; Belfast, Northern Ireland 2003- 2004.