Memories

I. Single - Bit
   A) Clock - less
   B) Transient latch
   C) Edge triggered
      Flip - flop

II. Array

reg Q_i;
always @(posedge clk) begin
    Q = D_i;
end

"=" blocking assignment

reg b, c;
always @(posedge clk) begin
    b = a_i;
    c = b_i;
end
"<=" non-blocking assignment

\[ b \leq a; \]
\[ c \leq b; \]

Rule #1 - Always use FFs

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Rule #2

For combinational logic, always use "="

\[ a = b \land c; \]

Rule #3

For FF always block, always use "<="

\[ \text{sum} \leq \text{#1} \land \text{sum-c}; \]

Rule #4

Add #1 clk delay for G

Synthesis - warning
(Guideline) Rule #5

Normally do not include any logic in FFs, always block

(Suggestion) Rule #6

For a large design, group logic + its FFs

Rule #7 - Robust clock design

A) Only clock signals may connect to FF

B) Clock signals may not connect to any node, other than the FF's clock.

C) There are exceptions

-> circuit issues
Rule #8 - Suggestion

Signal naming convention

Input A

Use FF resets only where needed

- multi-cycle reset
- lots of reset wires
- larger FFs
Asynchronous reset
- take effect w/o regard of clk

Rule 49 - never use these in class

Critical Timing Relationship (41)

1 GHz
period = \frac{1}{10^{12}} = 10^{-9} \text{ sec} = 1 ns

Clock

\[ \text{clk} \]
a) clock edge + output $t_{\text{clk-to-out}}$

b) logic delay (max) $t_{\text{logic max}}$

c) data before clock edge $t_{\text{setup}}$

$t_{\text{clk-to-a}} + t_{\text{logic max}} + t_{\text{setup}} \leq t_{\text{cycle}} \leq 1/f_{\text{freq}}$

Diagram:
- **Verilog** $\rightarrow$ Design
  - Compiler
    - *vgh (gates)*
    - reports
  - dc Compile
  - std cell lib