Jan. 20

Verilog that is ok in a testbench, not in HW

- # delay
  (except for `clk-to-φ`

- signed wire
  `φ`

- for

- # write
  # display

- @ (posedge `clock`) // always
  e (nosedge `clock`)

- repeat (50) @ (posedge `clk`)

- `# stop`
  `# finish`

- `time scale`
Testbench Approach #1

Testbench Approach #2
Faster CFA adder

0) Ripple-Carry

1) Carry-Select

[51:16] [15:0]