Today

• Administrative items
• Syllabus and course overview
• My background
• Digital signal processing overview
• Read *Programmable DSP Architectures, Part I* by E. A. Lee
Course Communication

- Email
  - Urgent announcements

- Web page
  - http://www.ece.ucdavis.edu/~bbaas/281/

- Office hours
  - Tentatively Monday 4pm – 5pm
  - After lecture Tuesday
  - After lecture Thursday
Course Workload

• **4 unit** graduate course

• This course requires significant effort and time
  – Multi-disciplinary field coverage
    • DSP algorithms
    • Digital processor architectures
    • Arithmetic
  – Utilizes robust industry-standard CAD tools (but we will make use of only the core essential features)
    • Verilog
    • Synthesis tool
    • Matlab
Course Readings

- No required textbook
- Over 800 slides posted as handouts on the course web page
  - You should fully understand all material in these handouts
- A few required papers
- Several posted tutorials with example code
  - You should fully understand these
- Several optional references
Main Course Material

• The main body of material is presented in the lectures, readings, and handouts

• Generally speaking, the hwk/projets complement the main material
  – They go into a much greater depth on specific topics
  – They give design experience
  – They give significant practical application of theory

• The Quizzes generally focus on the main body of material
Breadth and Depth

- Breadth and Depth
Course Overview

- EEC 281 web page contents
  - Reading materials and references
  - Hwk/Project descriptions
  - Handouts
Course Overview

• Canvas
  – Grades posted here
    • Let me know if you ever see a score different than you expect
  – Upload electronic portions of hwk/projects here

• Syllabus
  – Posted on course web page
Lectures

• Ask questions at any time

• How about we all turn on cameras?
  – Same as in a classroom
  – We are a small group
  – Less isolation during a very isolating pandemic
  – Easier to approach others, make contacts
  – Leaving your camera off makes it harder for others to turn theirs on
  – Feedback for me is very helpful

• Please hold conversations outside of class

• Please silence phones

• Integrated Solid-State Circuits Conference (ISSCC)
  February 17–19
  — Quiz 2 and short guest lecture on Tue, Feb 18
Letter Grade Assignments

- I assign a letter grade only for the final course grade
- I look at the final exams and course record of the class and assign two key dividing points: the A/A+ and (probably B/B+) boundaries, and assign course grades from there using equally-sized intervals
  - No required numbers of any particular letter grades
  - Absolute scores are not important; the boundaries shift according to the difficulty of the exams in any quarter
  - Ignore any letter grades you might see on canvas

Example with hypothetical data:
Working With Others

• Collaboration
  – Asking questions and explaining principles produces better work and dramatically increases learning
  – Working with others
    • Do homework and prelabs with classmates nearby
    • Ask each other questions, help each other—regarding principles, and approaches to solving only
  – See Course Collaboration Policy on web page

• Dishonesty
  – Copying produces similar work, stunts learning, is not fair to honest students, and is not allowed in this course
    • Students engaged in dishonest work will be referred to Student Judicial Affairs
    • I will try to keep in-class exams honest
    • Steps will be taken to keep out of class work honest
Penalties for Violating the *Policy on Student Conduct and Discipline*

- **Penalties**
  - Minimum penalty: meetings with SJA officer, zero grade on work, record with SJA
  - Permanent F grade on your transcript, no credit for the class
  - One to three quarter suspension from the university
  - Permanent dismissal from all ten campuses of the University of California. Permanent notation on your transcript.
Penalties for Violating the *Policy on Student Conduct and Discipline*

- Several perspectives
  - Personal obvious reasons
  - ECE and UCD (especially for those inclined to share work with someone doing poorly in class)
    Cheating harms our major and university’s reputation among employers who interview our graduates.

- In summary: The purpose of the penalties and me mentioning them is so that no one will get one!!! Don’t do anything that violates the Policy on Student Conduct!
Penalties for Violating the *Policy on Student Conduct and Discipline*

- **Typical scenario:**
  - Someone shares code/design with another
  - They get caught
  - The “Copier” feels terrible guilt for causing a friend to get a zero
  - The “Sharer” deeply regrets sharing resulting in a zero when he/she should have had a full score
Cheating Websites
chegg, coursehero, etc.

- The university has recently taken a very strong stand against paying for work (2-quarter suspension for first offense last year)

- Key take-away messages:
  - Do not post assignments
  - Of course do not use any unpermitted outside material in work you submit
  - Of course do not post solutions
  - Two students did last year and got caught!!!
MOSS

• “Measure Of Software Similarity” tool
• Utilizes very sophisticated and fast algorithms
• Processes all $\text{Order}(N^2/2) = N(N-1)/2$ pairings
  – Ex: examination of 300 submissions includes 44,850 pairwise comparisons
• If needed, MOSS runs will be made with this year’s work combined with work from past years
MOSS Demonstration Case

• Added, deleted, changed all comments
• Changed all variable names
• Reordered modules
• Reordered lines of code within modules
• Changed equivalent logic

• 91% similarity for submission 1
• 91% similarity for submission 2
MOSS

• Key take-away messages:
  1) MOSS is amazingly good at spotting pairs of submissions that share a common design
     • This meshes very well with the course collaboration policy
  2) Follow the course collaboration policy and you have nothing to worry about
  3) Violate the course collaboration policy and you will have something to worry about
Advancing CMOS Technologies

- Moore’s “Law” (Observation) was made in 1965 and notes that transistor density ~doubles every year (every 1.5 years now)
Moore's Law – The number of transistors on integrated circuit chips (1971-2018)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.

GC2: 16 nm, 23.6 billion transistors
Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2015 by K. Rupp
New data added by B. Baas

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Future Fabrication Technologies

• Basic trends
  – Number of available devices: continually increasing
  – Energy dissipation per operation: decreasing too slowly

• There are a lot of ways to place and connect a billion transistors
• The most efficient implementations (throughput, energy, area) will have:
  – Processor sizes that capture computational kernels with few excess circuits
  – Optimized clock frequencies and supply voltages matched to dynamic workloads
Optimal Computational Tile Size

- The most efficient implementations (energy, throughput, chip area) have: **Processor sizes** that capture computational kernels with few excess circuits.

![Diagram showing energy efficiency, clock rate, and area efficiency versus tile size.](image)

Unused or low benefit-per-cost circuits