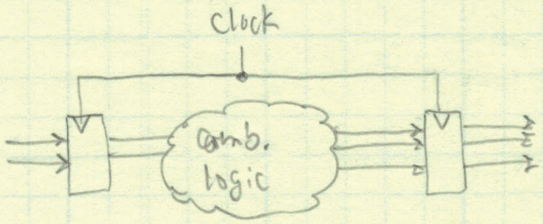
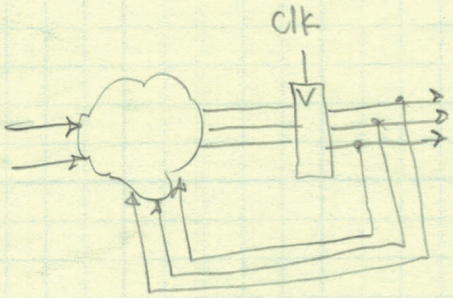
Critical Timing Relationships

If these are violated, the circuit will definitely fail under some circumstances.

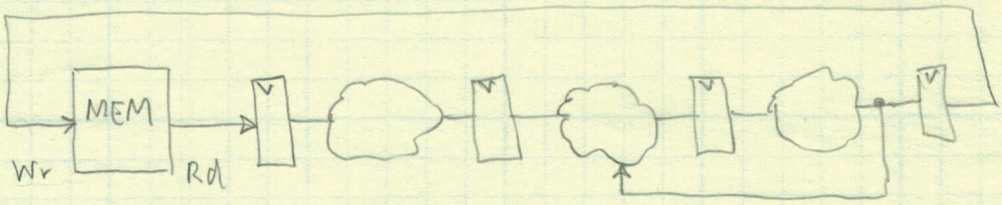
Fundamental block of every clocked digital system:



- FSM control, datapath, anything
- could also be latches, but we use FFs



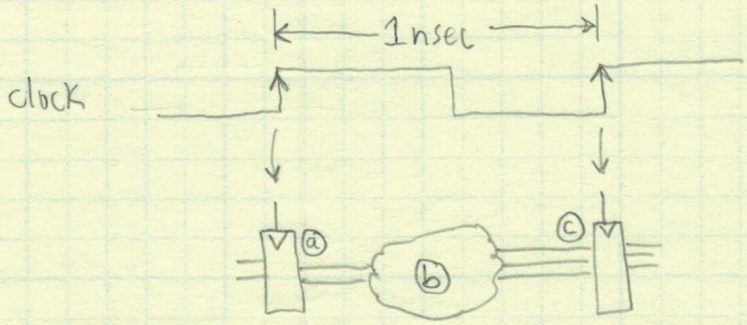
- could be the same register for both sides



Requirement #1 : Logic is not too slow (clock not too fast)

Ex: 1 GHz clock

clock period = $1/\text{freq} = 1/10^9\ \text{Hz} = 10^{-9}\ \text{sec} = 1\ \text{nsec}$



- There is one clock period for data to get from one register to the next one.

a) clock edge → Q output — $t_{clk\text{-}to\text{-}Q}$

b) time for the slowest path through the comb. logic — $t_{logic_{max}}$

c) time to arrive before the active clock edge — t_{setup}

∴ time circuit requires ≤ time allowed, for correct operation

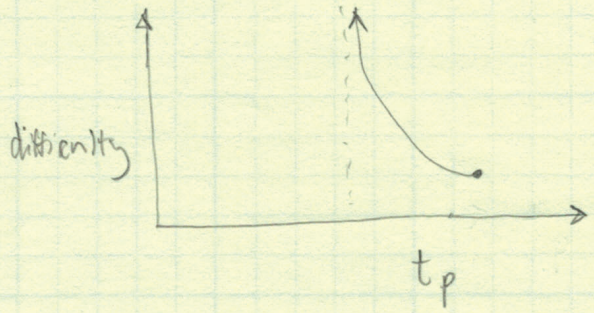
$$t_{clk\text{-}to\text{-}Q} + t_{logic_{max}} + t_{setup} \leq t_{cycle} \leq 1/\text{freq}$$

What if the requirement is violated?

A) Design time

- speed up logic

but...



B) After chip is built.

- only t_{cycle} is available

slow f_{clk} → longer t_{cycle}

i) product - maybe ok

1.9 GHz proc instead of 2.0 GHz ✓

59 frames per second vs. 60 fps ✗

ii) research - probably fine