Critical Timing Relationships

If these are violated, the circuit will definitely fail under some circumstances.

Fundamental block of every clocked digital system:

- FSM control, datapath, anything
- could also we latches, but we use FFs

- could be the same register for both sides
Requirement #1: Logic is not too slow (clock not too fast)

Ex: 1 GHz clock

\[
\text{clock period} = \frac{1}{\text{freq}} = \frac{1}{10^9 \text{ Hz}} = 10^{-9} \text{ sec} = 1 \text{ nsec}
\]

- There is one clock period for data to get from one register to the next one.

a) clock edge → Q output

b) time for the slowest path through the comb. logic

c) time to arrive before the active clock edge

\[ t_{\text{clk-to-Q}} + t_{\text{logic max}} + t_{\text{setup}} \leq t_{\text{cycle}} \]

\[ \leq \frac{1}{\text{freq}} \]

for correct operation
What if the requirement is violated?

A) Design time
   - speed up logic
   but...

B) After chip is built
   - only t_cycle is available
   slow t_clk → longer t_cycle

i) product – maybe ok
   1.9 GHz proc instead of 2.0 GHz ✓
   59 frames per second vs. 60 fps ✗

ii) research – probably fine